E158 Final Project Grading Sheet

Project:

Designers:

Checkoff

Proposed Project Difficulty	____ / 5
Project Meets Specifications	____ / 5
Implementation Quality	____ / 5
Project Fits Tiny Chip	____ / 2
DRC	____ / 2
ERC	____ / 2
NCC	____ / 3
Simulation	____ / 3
Total	**____ / 27**

Final Report

Color Chip Plot	____ / 1
attractive and legible	
Functional Overview	____ / 3
clear to other engineers	
Chip Pinout	____ / 1
padframe labeled with pin names, input/output/bidir	
Chip Floorplan	____ / 2
captions and dimensions of final design	
Area and Design Time Data	____ / 3
table listing area and design time for each cell in the design	
Simulation Results	____ / 3
description of simulations performed include a few pages of key waveforms convince reader design works	
Verification Results	____ / 1
DRC, ERC, NCC pass	
Postfabrication Test Plan	____ / 3
clear to other engineers	
Schematics / Verilog	____ / 3
complete set of drawn schematics and Verilog for synthesized blocks legible and well-commented	
Layout	____ / 3
complete set of layout clean and efficient	
PDF Submitted	
report submitted in electronic form	____ / 1
Total	**____ / 24**