Microprocessor-Based Systems (E155)

Final Project Requirements

Overview

The E155 Final Project is a chance for you to apply your new skills in digital design to a moderate sized problem as part of a two-person team. You should begin thinking about a project and teammate right away. Your project has the following milestones:

10/30:	Project Proposal Due
11/20-11/21:	Project Status Report & Demo Due
11/20-12/4:	Project Presentations
12/11-12/12:	Project Checkoffs
12/13:	Demo Day Party
12/13:	Final Report Due

Project Scope

Be creative when selecting your project. Your project should be bigger than a 1-week lab assignment, but small enough to be doable. If in doubt, err on the side of smaller. You will fail the class if you underake a project that is too big and produce no completed work.

I expect a typical project will use both the FPGA and ATSAM and will perform a function that is useful or interesting. You can find examples of past final projects on the class web page. Examples include games, electromechanical systems, prototypes for a startup company, or elements of a Clinic project (with your advisor's permission).

Budget

If your team needs parts that are not available in the stockroom, you may spend up to $50 to purchase them. You will need to save your receipts, fill out a reimbursement form in the department office, and have me sign the form. Of course, you can exceed this budget, but you must pay the remainder out of your own pocket.

Deliverables

Your team is responsible for the following deliverables at the dates described above:

Project Proposal

A 2-page proposal describing what you plan to build. *It must be specific enough that I can tell when you demonstrate your project that it meets the specs of the proposal.* Do not list stretch goals or wiggle words; simply state what you are committing to delivering. You may need to do some preliminary technical work to gain confidence you can deliver what you are promising. Include a budget for any supplies are not available in the stock room. Describe the main subsystems of the design and the features of the ATSAM that you plan to use. Explain the new piece(s) of hardware and show that both the FPGA and ATSAM are performing nontrivial functions appropriate to each. Include a block diagram showing the components and the interfaces between each.

Status Report

A 4-page report (plus appendices) documenting your design at the midpoint. The status should include schematics of anything on a breadboard, block diagrams of the logic on your FPGA, and an outline of the routines used on the ATSAM. You should include as an appendix either your Verilog code or software that is mostly complete (but do not have to have both ready). You must be ready to demonstrate some working hardware in the lab.

Problem Presentations

Your team will sign up for a 8-minute presentation on one of the days near the end of the class. Your presentation should include a 3-minute overview of your project followed by in-depth presentation of a specific technical problem your team is working on and has not yet solved. The goal of the presentation is to get input from other students who might have ideas of how to solve your problem so you must explain the problem clearly enough to get meaningful suggestions back.

Project Demonstration

Demonstrate a working project to the instructor in the lab during your lab section. There will be signups for demonstration periods, during which you will show that you meet your specificantions and be asked technical questions about the operation of your design. Come prepared with printouts of your schematics, software and Verilog. If your project is one day late, one letter grade will be deducted. Teams unable to demonstrate at least some functional system by Friday will fail the project.

Final Report

Turn in a final report documenting your design, not to exceed 12 pages plus appendices. Clearly explain how your design works. If you have developed techniques that would be useful for students in the future (e.g., how to interface to an LCD display), document these features well so that future students may build on your work. The appendices should include complete schematics, code, and Verilog for your design.

Late projects will not be accepted except in the case of unusual extenuating circumstances. Be careful to choose a project within a scope that you can reasonably expect to finish. If you realize your project is too large, contact me as soon as possible to renegotiate your project proposal. I will not accept revisions to the proposal after 11/26.

Grading

Your project will be graded as follows:

Proposal	10%
Status Report	20%
Presentation	10%
Demonstration	40%
Final Report	20%

If you feel there has been inequality between the work you and your teammate deliver, contact me personally.