Microprocessor-Based Systems (E155)

Lab 1: Utility Board Assembly

Introduction

In this lab you will assemble and test your µMudd Mark V.1 utility board containing an Altera Cyclone IV FPGA, Atmel SAM4S ARM Cortex-M4 microcontroller (MCU), Flash configuration memory, LEDs, switches, and a clock oscillator. You will be using the board for the remainder of the semester, so it is very important to assemble it properly. But don't panic! You'll quickly learn to troubleshoot and repair issues, and you are provided an automated test system to check that the microcontroller and FPGA are functional. If you totally cook your board, you may obtain parts for another one from the stock room.

Learning Objectives

By the end of this lab you will have…

- Learned how to solder
- Assembled and tested your µMudd Mark V.1 utility board
- Written a Verilog module to control LEDs and a 7-segment display
- Programed the FPGA with your Verilog code
- Gained confidence in building, assembling, testing, and debugging circuits
- Interfaced the 7-segment display to the utility board

Requirements

Follow the steps in this guide to test and assemble your µMudd Mark V.1 utility board. Write some Verilog code to exercise the FPGA using the switches, LEDs, and a 7-segment display to ensure your board is operational. Simulate and synthesize your code, then burn it onto the Flash memory and re-test the board. Hook up a 7-segment display and demonstrate that it works.

Background

In the 1980's and 1990's, digital design projects were built from a truckload of chips, each containing a few logic gates such as 74xx series logic gates or simple programmable array logic chips (PALs). Such projects involve placing and wiring together dozens of chips on a breadboard. It was easy to make a wiring mistake or burn out a chip and spend hours tracking down the problem. Now you can perform all of your digital logic on a single field-programmable gate array (FPGA) to greatly reduce the necessary wiring and number of chips. Later in the course, you will use the onboard Cortex-M4 microcontroller to write programs in assembly language and C that can interface with external hardware and the FPGA.

You will need to connect your FPGA to the real world to get inputs and outputs. In particular, you will often find it useful to have a clock oscillator, switches, and LEDs. Moreover, the FPGA comes in a 144-pin thin quad flatpack (TQFP) package. This is a surface mount (SMT) part so the pins of the chip do not go through the printed circuit board (as with the other through-hole parts you'll be working with). SMT components are mounted on pads on top of the PCB. Their pins are so small that special soldering skills and tools are needed to reliably attach them to the board. Your board comes with the FPGA, Flash memory, and the microcontroller already attached, but you will get to solder the rest, including a few easier SMT components.

The FPGA you will use in this course is the Altera Cyclone **EP4CE6**, which contains 6,272 Logic Elements. You can find the datasheet on the class web page. You will need to become familiar with the internals as you progress in this class.

The board was designed to maximize your access to the capabilities of the FPGA and MCU from a breadboard. Therefore, as you will notice, the board has a single row of 58 header pins (on one of the long sides of the board) that give you access to many of the FPGA and MCU pins. The other pins of the microcontroller and FPGA are power, ground, unused, or internally wired. Furthermore, the pins are labeled for your convenience. The other characteristics of the utility board will be explained later, in the Discussion section of this guide.

The µMudd Mark V.1 board schematic is at the end of this manual. Study this schematic to understand what goes on in the board because you will need this information to use and debug your board and are likely to be asked about some subsystem during your checkoff. The parts in the schematics are labeled using R for resistors, C for capacitors, and U for units (chips and other large parts).

To maximize your chances of building a functional board, we've created a test board which interfaces with the µMudd Mark V.1 through its edge card connector (the wide and exposed traces on the bottom of the board). The test board provides power and ground, programming interfaces, and a few LEDs for debugging. Aside from a few simple components, the test board allows you to test the FPGA and MCU with minimal assembly.

Component Discussion

The figures at the end of this document include both the bill of materials (BOM) and the utility board schematic. Major components include the power supply, header pins, clock generator, reset pushbuttons, the JTAG programmer connector, DIP switches, and LEDs. What follows is more information about several key components on the board.

Read through and understand this section that describes each of the board components. Identify the components in the schematic and think about how they operate. The subsequent section will guide you through the assembly process.

Power Supply

The utility board is supplied power by the header pins Vin and GND. The input supply should be at least 5 volts. The input is regulated down to 3.3 V, 2.5 V, and 1.2 V to serve various components on the board. The 3.3 V regulated voltage is also available at another header pin to serve other components you might want to connect to your board. Be sure not to connect this 3.3V output to another 3.3V supply: the two voltages will be subtly different and will cause contention and likely board damage. Also, as with any supply voltage lines, don't short the 3.3 V output to ground.

In the lab, the easiest way to supply power is from a 5 V benchtop power supply to the Vin header pin. If you do not have a power supply available, a DC transformer is an inexpensive alternative. For untethered applications such as robotics, you can also use a battery pack providing at least 5 V.

The FPGA I/O's will operate at 3.3 V, which we will call V_{CC}. The FPGA contains tiny logic transistors that would burn out at 3.3 V, so the 1.2 and 2.5 V supplies are needed to operate the digital logic and the analog circuitry within the FPGA.

Header Pins

The board provides one 58-pin row of male header pins that tap out signals from the FPGA, MCU, LEDs, switches, and power and ground. The header pins will be installed along the left side of the utility board.

Additionally, the board has a 18-pin edge card connector at the bottom of the board for debugging. This exposes power supplies as well as configuration interfaces, status pins, and some I/O for the MCU and FPGA. We've built test boards that interface through this connector and allow you to test that your microcontroller and FPGA are functional with minimal board assembly.

Clock Generation

In digital electronics, the term clock refers to a square wave that oscillates between GND and V_{CC}. Typically, clocks are used to sequence the action of a circuit. For instance, a flip-flop samples its input every time the controlling clock rises from logic 0 to logic 1. The clock signal is sent to the FPGA and MCU. The utility board has a 40 MHz clock signal provided by a crystal oscillator.

Reset Pushbutton

There is one reset pushbutton switch on the board which resets the FPGA. Upon reset, the FPGA, will have its memory cleared. If the PROM is programmed, the FPGA will immediately reprogram itself from the PROM. You will notice that these pushbuttons actually have 4 pins. However, only two pins are used, while the other two are left unconnected (and simply provide mechanical stability).

There are an additional two pushbuttons which reset and erase the MCU. When the reset pushbutton is pressed, the microcontroller resets its internal state, and begins executing program code from the base of its program memory. The erase pushbutton, however, erases all internal microcontroller memory - this includes any code which you've uploaded.

JTAG Programmer Jack

In the top right corner, the double row of header pins (marked JTAG) is for programming the FPGA.

The small 10-pin connector in the bottom right corner provides another JTAG interface for programming the MCU.

DIP Switches

The DIP switches provide a convenient source of inputs to circuits in your FPGA. When the switch is closed, it delivers a high output. When the switch is open, a pull-down resistor produces a low output.

LED array

There is a 10-segment, red light-emitting diode (LED) array on the board. The 'ON' LED (far left LED, with the pin header towards you) simply tells that the board is powered ON and receiving 3.3 V. The LED immediately to the right of the ON LED is used by the JTAG programmer. The other 8 red LEDs can be driven by the FPGA or MCU. Notice that there are 8 header pins labeled LED0 – LED7. These can be used in case you want the outputs of the LEDs for an external device. If a voltage is applied at one of the LED pins, the corresponding light is off for ground (GND) and on for voltage 3.3V (V_{cc}).

There are a few concerns that must be addressed whenever using LEDs. One is that LEDs glow nicely when given about 5 mA of current but may burn out when given more than about 20 mA. Therefore, it is important to include a current-limiting resistor to prevent LEDs from burning out, overheating the driver, or simply wasting power. A 330 Ω resistor does the job nicely, allowing $\sim \frac{3.3V}{330\Omega} = 10$ mA of current to flow. (In actuality, the current is about half of this. There is a voltage drop across the diode (about 1.7V for red), which makes the actual current $\frac{3.3V-1.7V}{330\Omega} = 4.8$ mA. This is still around the desired 5-20 mA range and so still works).

FPGA

The FPGA contains a large array of configurable logic blocks (CLBs) and programmable interconnections. The configuration information is stored in static random-access memory (SRAM) within the FPGA. Therefore, the information is lost when power is removed, and the device must be reconfigured each time it is powered up.

The FPGA can be configured via the Programmable Read Only Memory (PROM) on board. On powerup, the FPGA will serially configure itself from the PROM if the PROM has been programmed. It will also reprogram itself from the PROM when you push the reset button. Alternatively, designs can be programmed directly onto the FPGA in the Quartus software via the JTAG connection. This will overwrite the design already loaded from the PROM but will only last until the FPGA is reset or the power is disconnected.

Microcontroller

The board includes an Atmel SAM4S4B Cortex-M4 microcontroller. This is similar to the Cortex-M0 in the E85 Nucleo boards, albeit faster, with more powerful instruction set extensions, and with a larger peripheral set.

This microcontroller can be programmed through the small JTAG connection in the bottom-right corner of the board. As with the Cortex-M0, code will automatically execute when power is supplied. A reset after uploading new code ensures the most recently uploaded code is executing.

Assembling the Board

This section will give you tips on how to assemble the utility board. Following these tips will help you complete this lab quickly and in a logical way that places the flattest components first to make soldering easier.

□ Identify the Component Side of the Utility Board

The utility board has two sides. The component side, with the white silk screen markings indicating component placement, should go up. All components except the 58-pin header are placed on the component side. The through-hole parts (except the 58-pin header) are soldered on the reverse solder side. The surface-mount components are soldered using solder paste on the component side.

Using a multimeter, measure the resistance between the pins labeled Vin and GND on the board, and verify that the resistance is nearly infinite. If the resistance is low, you have a short circuit on your bare board and should get a new one. As you assemble your board, occasionally check the resistance between Vin and GND. If it is ever less than 10 Ω, you've introduced a short and should debug it before continuing.

Note: CMOS components such as the FPGA are sensitive to static electricity. Before you touch your board or solder anything, discharge your body by touching a large metal object. This is good practice when handling electronic components in any lab.

The FPGA should already be soldered to your board. These is a fine-pitch SMT component that requires practice to attach without creating solder bridges between pins. If your board malfunctions and you suspect a bridged or bad connection on one of the SMT chips, check the connections under a microscope. On the bottom side of the FPGA is a large ground pad that should be soldered to the ground plane of the board. There is a hole in the board underneath the FPGA for this purpose. Check that the pad on the back of the FPGA is soldered to the metal ring of the hole and add solder if the assembler neglected to make this joint. Make sure the iron is touching both the component and ring so the solder adheres to both.

Similarly, the MCU should already be soldered to the board. While the MCU has less than half of the pins of the FPGA, it is similarly fine-pitch, and may be the cause of board malfunctions. As with the FPGA, a good first debugging step is checking the MCU pin solder joints under a microscope.

When you begin soldering, moisten the sponge. When the iron first heats up, tin the tip by applying a generous amount of solder all over the tip, then wiping off the excess on the sponge. Periodically repeat as you work to keep the tip looking silvery rather than black and blistered.

For through-hole components, touch the tip of the iron to the pad on the board at the same time it touches the lead of the component. Apply the solder to the joint, not the tip of the iron. The solder should smoothly adhere to both the pad and the component pin rather than balling up on the component. The connection should appear shiny; a gray color indicates a possible unreliable "cold solder" joint.

For surface-mount components, apply a small drop of solder paste to each pad. Use tweezers to place the component into the desired placement. Use the tweezers to hold the component in place while you touch the tip of the iron to each pad.

If you are in doubt about the quality of your solder joints, ask early on rather than doing all of them first and discovering that your connections are intermittent or unreliable. Some of the components will be soldered close to vias (the small holes through the board used to connect between wiring layers on the printed circuit board). Be sure excess solder does not bridge to the via, creating a short circuit. When you are done, tin the iron one last time to protect the tip before turning it off.

A Safety Note: You may wish to use safety goggles while soldering, especially if you don't wear glasses. Also, be sure to hold the ends of leads as you cut them after soldering so they don't fly into the eye of the person working across the room. Solder contains lead, so wash your hands afterward.

□ Insert the Microcontroller Clock Inductor

Before you can test the microcontroller and FPGA with the test board, you need to build the minimum-viable microcontroller support circuity. For the µMudd Mark V.1 this is the 10 µH inductor L1. This is a simple through-hole component with no polarity.

□ Solder the Oscillator

Next, install the oscillator. This part is a surface mount (SMT) part. Soldering a surface mount device would be easiest if you had three hands: one to hold the part with tweezers, a second to hold the soldering iron, and a third to apply the solder. If you do not have three hands, solder paste is handy. Apply some paste to the pads, then place the part on the board and hold it with tweezers in one hand while using the soldering iron or hot air tool in the other hand to melt the paste., while a silvery appearance covering the pad and pin usually means a good connection. If you don't have solder paste, another option is to apply a blob of solder to one of the pads, then place the part on the pad, hold it with tweezers, and re-melt the solder with the iron.

Be mindful of how much solder you use while connecting surface mount parts. Using too much solder can bridge between pins, causing shorts. Use solder wick to remove the bridge. Excess solder can also bridge to nearby vias. Finally, extra solder will exert forces on your part as it cools, which makes it harder to position precisely.

Also be sure the notch on the crystal oscillator chip aligns with the notch on the board's silkscreen.

□ Test the oscillator

Insert the µMudd Mark V.1 into the test board edge card socket, such that the component side of the board faces the power plugs on the test board. Make sure you insert the µMudd completely into the test board socket: you should not be able to see traces outside the connector housing.

Once the board is inserted, connect the test board to 5V supplied from a lab power supply through the two banana plug sockets. Verify that the oscillator was installed correctly by using the oscilloscope to view the oscillator signal. You should use the analog side of the scope. The probes should be in the top right drawer of your lab station. Be sure your probe is in the 10x mode to have the bandwidth to view the fast signal. Make sure to attach the probe ground wire to your circuit ground. The clock signal is pin 3 of the oscillator chip (not P3 of the headers). Adjust the voltage and time scales so you can see a nice signal. Use either the cursors or the Quick Measure feature to verify that the correct frequency clock (40 MHz, which corresponds to a 25 ns period) is being produced.

□ Test the Microcontroller and FPGA

Once the board is inserted and oscillator tested, open projects fpga_boardtest and mcu_boardtest in Quartus Prime and Keil uVision. These are available from the course website in the Board_Testing.zip archive.

Begin by programming the MCU. Connect the Segger J-Link Mini programming adapter such that pin 1 on the programmer and pin 1 on the test board align, and in the Keil project mcu_boardtest, press the Load button, and then cycle power to the board. At this point the microcontroller will be executing test code.

Next, connect the FPGA JTAG programming cable, such that the ribbon points outward from the test board. Go to Tools -> Programmer, and if necessary, add the file 'fpga_boardtest.sof'. Press 'program' and wait for the progress bar in the upper right-hand corner of the window to reach 100%.

The LED marked 'blink_good' on the test board should be flashing. This illustrates that both the microcontroller and FPGA are functional. If the light is solid, then the microcontroller is not functioning. Check that the inductor is properly installed and the crystal oscillator is generating a 40 MHz square wave signal. If the light is completely off, then the FPGA is not functioning.

If you are unable to program the microcontroller or FPGA or find that the µMudd Mark V.1 fails the 'blink_good' test, then swap your µMudd with one from the stockroom.

□ Insert the Resistor Networks

Next you should install the resistor networks at R7, R8, and R9.

R7 and R8 are isolated resistor networks for the LEDs. 'Isolated' means that it contains a set of totally independent resistors. These particular resistor networks are sets of 5, 330 Ω resistors. Pins 1 & 2 are one resistor, pins 3 & 4 are another, and so on. Polarity does not matter. You may find it helpful to bend one pin at each end of the resistor network to hold it in place while soldering.

R9 is a Single-In-Line (SIL) resistor network. 'SIL' means that it contains resistors that are all connected to a single common pin. This particular one is a 5-pin component that has 4, 2.2 kΩ resistors. Pins 2, 3, 4, and 5 are terminals of the four resistors. Pin 1 is the common pin. On the board, this is connected to ground. Since R9 is not symmetric, **polarity matters**. Pin 1 is marked on the component with a square marking. Similarly, pin 1 on the board is marked with a square terminal instead of a round terminal. Make sure these are aligned or you may short circuit your board.

□ Insert the Resistors and Bypass Capacitors

Now install the resistors and bypass capacitors. For this board, all of these components are 0805 SMT components. The polarity of these components does not matter so you can insert them whichever way you'd like. However, some of the components have labels, and it is good practice to install labeled components in the same direction, making it easy to read them. See Table 1 for resistor and capacitor values.

The bypass capacitors are important to reduce noise on various voltage lines. Large capacitors near the voltage regulators are there to supplement the voltage regulator for spikes of current draw. Though the voltage regulators can supply current sufficient to meet the average demand of the circuits on the board, they cannot respond quickly enough to deliver high frequency spikes in current demand. Such spikes would cause the voltage to briefly droop, if the bypass capacitors were not there to supply the current.

A typical digital system uses several sizes of bypass capacitors. Larger capacitors store more charge and can deliver more current but react more slowly. Smaller capacitors can rapidly deliver charge to handle short spikes of demand. Large 10 μF capacitors are placed near the voltage regulators to supplement their current supply. Smaller 0.1 and 0.01 μF capacitors are placed near the digital components for the highest effectiveness at reducing noise at their voltage inputs. Overall, the bypass capacitors reduce the noise on the voltage supplies.

Note that the chips and board have some inherent capacitance as well, so the voltage might be stable enough even without bypass capacitors. However, noise-related problems are so difficult to reproduce and fix that it is always better practice to put a generous number of inexpensive bypass capacitors on the board than to skimp on bypassing and hope the board works anyway.

Part	**Reference Designations**
1 Ω resistor	R10
1 kΩ resistor	R2-3
10 kΩ resistor	R1, R4-6
100 kΩ resistor	R11-13
0.01 μF capacitor	C1, C2, C3, C10
0.1 μF capacitor	C4, C6, C8, C11, C12, C13, C15, C17[1]
2.2 μF capacitor	C14
4.7 μF capacitor	C16
10 μF capacitor	C5, C7, C9

Table 1: Resistor and capacitor component values.

[1] Note that C17 from the parts list and schematics is mislabeled on the actual board as C18.

□ Install the Pushbutton Switches

There are three small pushbutton switches that come with your kit, to be installed at FPGA_RESET, SAM_RESET, and SAM_ERASE. When installing these, you will have to align it in its holes and push until it snaps into location. Do not put your finger directly underneath the board because the sudden popping into position could stab your finger. A thin pair of pliers helps push the legs through. The switch will only align in two positions on the board; either alignment will work.

□ Insert the DIP Switches and LED array

The DIP switches are to be placed in the middle of the board above the LED array. Align the writing on the DIP switches with the silk screen writing on the board. When installing the LED array, make sure you align the notch on the part with the square solder pad on the board for correct alignment.

□ Install the JTAG connector

Install the JTAG connectors at JTAGFPGA and JTAGSAM. The connectors are symmetrical, so rotation does not matter. JTAGSAM is a relatively fine-pitch through-hole part: double check your solder joints to ensure no bridges have been formed.

□ Install the 58-pin Row of Header Pins

This is the *only* part that is installed on the bottom and soldered on the top (it will be inserted into the breadboard). Place the part so that the long pins extend below the board, with the black bumper up against the bottom of the board. The short pins go through the board and are soldered on top. You'll be sad if you install it differently and have to chop it out and remove it one pin at a time. Watch carefully that you do not use too much solder because it may bridge to one of the vias. When you place the header pins, try to keep all of them perpendicularly aligned so that placing the utility board in your breadboard isn't too much of a headache. As the header pins come in strips, you will need to use one long strip and cut one shorter strip.

Now hopefully you should be done with assembling your board. Before proceeding with the lab, you should check all of your solder joints. They should look reliable, filling their specific holes in the board. If some of your soldering looks more like a bubble on the top of the pin, you probably have a bad connection there. Also look for solder jumping across pins or to vias (solder bridges) and cold solder joints (gray, dull joints).

After you've checked your soldering and verified with a multimeter that there is no power to ground short on the board, your board is done!

□ Place the Utility Board on the Breadboard

Now you have to place your board on the breadboard. It should fit in the right-most side of the breadboard.

□ Test the Power Supply

After you've placed the utility board, connect a red wire from the red Vin banana plug connector to the upper power row. Then, from this row, connect a wire to the row of pins next to the Vin pin on the utility board. Then connect a black wire from the GND banana plug connector of the breadboard to the second power row (below the red wire). Connect this row to the Gnd pin of the utility board. Make sure these wires do not touch each other.

Without connecting the benchtop supply to your breadboard, turn it on and check that the 0-6 V scale indicates 5 V. Adjust it if necessary. Please keep the supply set to 5 V. It is good practice to check the supply before connecting it to your board because the knobs occasionally get bumped and you don't want to connect an incorrect voltage that damages your board or causes erratic operation.

When the power supply is set correctly, turn it off. Get a red and a black pair of banana plugs and connect the power supply to your breadboard (never connect power circuits while the supply is turned on). Turn the supply back on. The power LED should turn on. Feel your FPGA and make sure it does not get very warm. Also check your other components, especially the voltage regulators. The current from the supply should be around 100 mA. Check the 3.3 V output pin and confirm that the voltage regulator is producing the correct value. Also check that the capacitors C3 and C6 next to the 1.2 and 2.5 V regulators have 1.2 and 2.5 V on one of their leads.

□ Clean Up

Clean up your lab station. Discard the refuse you accumulated while soldering. Tin the iron and turn it off. Please keep the lab clean and neat as you work because you share it with many others.

FPGA Design

Your next goal is to write some Verilog modules to test the hardware on your board and operate a 7-segment display. By writing a module to control the LEDs based on the switches and clock, you will show that these components work and also that the FPGA, PROM, and power supply are functional. The system should have the following inputs and outputs:

clk	input	the 40 MHz clock
s[3:0]	input	the four DIP switches
led[7:0]	output	the 8 lights on the LED bar
seg[6:0]	output	the segments of a common-anode 7-segment display

The following tables define the relationship of the LEDs to the switches and clock:

S0	LED0	LED1
0	OFF	ON
1	ON	OFF
S1	**LED2**	**LED3**
0	OFF	ON
1	ON	OFF

S2	LED4	LED5
0	OFF	ON
1	ON	OFF

S3	S2	LED6
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

LED 7
Blink at ~2.4 Hz

Table 3 – I/O Requirements

The 7-segment display should display a single hexadecimal digit specified by s[3:0]. Be sure each digit can be distinguished from other digits (e.g. b and 8 should look different). Remember that you will be using a common anode display. The anode (positive terminal) of all of the LEDs is tied to 3.3 V through a single ("common") pin. Each segment's cathode (negative terminal) is connected to a pin. Therefore, you will need 7 separate control signals. Remember that a logic 0 applied to the cathode will turn on the segment. The segments are defined as shown below. Let seg[0] be A and seg[6] be G.

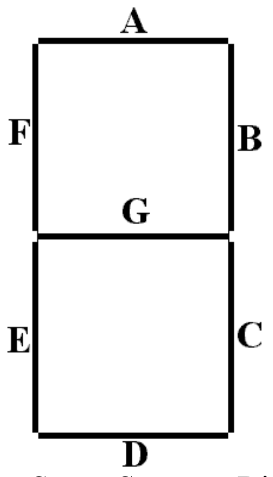


Figure 2 – Seven Segment Display layout

Launch the Quartus Prime software and start *New Project Wizard* from the File or startup menu.

Your first decision is where to keep your files. Ideally, they would go on your Charlie home directory. However, Quartus can be painfully slow accessing files on the file server over the network. An alternative is to keep your files on the local C drive while you are working and then to copy them back to your Charlie account before you log out. Please clean up after yourself by deleting the project from the C file when you are done, and remember that it is an honor code violation to refer to somebody else's code that was left on a computer. Note that some CAD tools have trouble with filenames having spaces and other special characters, exceeding 8 characters, or in paths not starting with a letter drive. The best way to avoid these problems is to choose short alphanumeric filenames.

Create a working directory for the project such as c:\e155\xx\lab1_xx where 'xx' area your initials. Name the project lab1_xx and click Next.

Click *Next* at the Add Files page, since we will not be adding any existing files to the new project. Now we will tell Quartus which FPGA we are using. Under Family, select **Cyclone IV**. Under Available Devices, select **EP4CE6E22C8**. If you ever forget which device to use, the part number is written on the FPGA.

On the next page, select Pick *ModelSim-Altera* as the Simulation tool and *SystemVerilog HDL* as the format. Click Next and verify the settings for the project. When you are satisfied, click Finish.

Choose *File* -> *New* and create a SystemVerilog HDL file. Save the file as lab1_xx.sv in your project directory and check the box to add the file to the current project. Create modules to perform the functions described above. The 7-segment display decoder should be combinational logic. Use a reasonable amount of hierarchy. Name the top-level module lab1_xx. The 7-segment display code, for example, will be reused in future labs, so it should be a module of its own. Every module should begin with a comment section that includes your name and email address, the date of creation, and a brief summary of its purpose, so that somebody else can understand what the module does and get ahold of you if they need help. Comment the modules as appropriate.

Logic Simulation

The next step is to simulate your logic with ModelSim.

Check that Altera has the correct path for ModelSim by invoking *Tools → Options*. Under EDA Tool Options, check that the ModelSim-Altera path is

f:\altera\13.0sp1\modelsim_ase\win32aloem

and set it if necessary. EDA stands for Electronic Design Automation and is the industry name for computer-aided design (CAD) tools for electronic design.

For unknown reasons, Quartus wants you to compile your code before simulating. To do this, select *Processing → Start Compilation* to compile your design. Ignore warnings about missing pin assignments or timing violations.

Invoke ModelSim by choosing *Tools → Run Simulation Tool → RTL Simulation*. RTL stands for Register Transfer Level code (your SystemVerilog code). The ModelSim window will open. Get in the habit of watching the transcript window to look for errors and to familiarize yourself with what a good run looks like. If you see errors, close ModelSim, correct your Verilog code in Quartus, and reopen ModelSim.

At this point it is possible that you will see the error "** Error: (vlog-19) Failed to access library 'work' at "work". In that case, open your SystemVerilog file in ModelSim, click the "Compile" button, find your file in the resulting dialog box, click compile, and click "yes" when prompted to create the library "work".

In ModelSim, simulate your design by choosing *Simulate → Start Simulation*. Click on the + symbol next to the work library and select your code (lab1_xx).

If the wave pane isn't open, open it by choosing *View → Wave*. View all of the inputs and outputs of your design by selecting them in the Objects window and dragging them to the Waves window. In a more complicated design, you may wish to examine internal signals as well.

Manually test your design by forcing the inputs to specific values. In the transcript window, type:

```
force s 0000
run 100
force s 0001
run 100
force s 0010
run 100
…
```

You should see the led and seg outputs displaying appropriate values. Note that the clock is not driven and you have not reset any registers so led[7] will be an x.

Check the outputs against your expectations. If you find any discrepancies, fix the code and resimulate. A helpful shortcut to avoid restarting ModelSim is that you can edit the module by finding it in under "work" in the library pane, right clicking, and choosing *Edit*. Make your fixes, then right click again and choose Recompile. Then type restart -f in the transcript window to restart simulation without having to set up the waveforms window again. When you return to Quartus, you'll find your corrected code.

Pin Assignment

Next, assign pins to relate the signal names in your Verilog code to physical pin numbers on the FPGA. Launch *Assignments → Pin Planner*. A table listing all inputs and outputs for the project should appear. Under Location, type the pin number to associate with the given signal. For example, SW0 is mapped to pin P76, so enter PIN_76 as the value for s[0].

The FPGA pinouts are shown in the Utility Board Schematic. Most of the user input/output (I/O) pins are tapped out to the headers and labeled on the board silk screen. Some have special functions; for example, FPGA pin P68 is connected to LED0. The clock is connected to pin P88 and not to a header pin because a 40 MHz clock would be degraded by the parasitic capacitance and inductance of the breadboard.

The pin numbers for the LEDs and switches are marked on the board's silkscreen. For the outputs for the 7-segment display, you may select any I/O pins you'd like. For example, you could use pins 51, 52, 53, 54, 55, 58, and 59 since they are contiguous on the board.

Note that the Pin Planner defaults to assuming that each bank of I/O pins receives 2.5 V and uses 2.5 V outputs. However, our system uses a 3.3 V I/O. Fortunately, leaving the voltages at their default value in Pin Planner works and generates 3.3 V outputs.

7-Segment Display Circuit

The 7-segment display will be used throughout the class for general output of numbers. In this lab assignment, though, it will be used to output the hexadecimal number entered by the user through the DIP switches.

Each segment of the display works as an independent LED. Therefore, the same current-limiting concern with the LEDs applies to the display as to the on-board bank of LEDs. You can limit the current into each segment of the display the same way you did for the LEDs on board, adding a suitable resistor to provide roughly 5-20 mA of current. You can find resistors and other such components in the supply cabinet or in the stockroom.

Consult the data sheet for the pinout of the common anode dual seven segment display. All seven segments share the same anode, which should be connected to VCC (3.3 V). Each of the segments has its own cathode, which can be pulled to 0 to turn on the segments.

Be sure to turn power off before wiring circuits on your board. You can choose either side of the display to use in this lab. After deciding on which side to use, you will need to connect the V_{DD} pin of that side (either $V_{DD}1$ or $V_{DD}2$) to 3.3 V. Then connect the input pins of the same side of the display to the header pins you chose. Remember to add suitable resistor between each of the inputs to the display and the header pins. These LEDs are common anode LEDs. That is, all the anodes from the LEDs are connected to a single V_{DD} ($V_{DD}1$ or $V_{DD}2$). You are driving the cathode of each LED. Given this information, you might need to modify your Verilog file. Do so in the simplest way possible.

Generating the FPGA Configuration Files

Now you will synthesize your HDL into a programming file to be transferred onto the FPGA. This outputs an SRAM Object File (.sof) in your project directory that can be used to program the FPGA directly over JTAG. Be sure your SystemVerilog files are saved, and choose *Processing → Start Compilation*. To help sort the many messages that the compilation process generates, click a tab under the Message area to see only that type of message. If compilation is successful but generates warnings, check the Warning and Critical Warning tabs for errors relevant to your design. Warnings about incomplete I/O assignments may be ignored if you have in fact assigned all relevant I/O pins. Missing Synopsis Design Constraints file warnings and timing analysis violations may also be ignored.

Note that Quartus seems to crash from time to time while compiling. If it does, restart and try again. If you find a consistent pattern of what causes the crashes, please let the instructor know.

Launch *Tools → Netlist Viewers → RTL Viewer* and examine the RTL schematic of your design. This shows the logic synthesized from your Verilog design. Ensure the hardware matches your expectations.

Look at the Compilation Report tab. In the Flow Summary, you should see a total number of registers and pins that match your expectations. Under Analysis & Synthesis, you can see how the logic blocks and registers are broken down in each module. Under Fitter, the Pin-Out File should match the pin assignments you intended.

Programming the FPGA via JTAG

Next, you will load your design onto the FPGA and PROM with an Altera USB Blaster programming device and the chip's JTAG[2] interface. Run *Tools → Programmer* to bring up the Programmer window. In the top left corner, check that *USB Blaster* is selected and use *Hardware Setup* to choose it if necessary. In the top-right corner, set *Mode* to JTAG. Your lab1_xx.sof file should appear already in the programmer window, and list EP3C5E144 as the associated device. If it does not appear, click the Add File… button and find the file by hand in your project directory. Be sure the Program/Configure box for your .sof file is checked.

You are now ready to program the FPGA. Connect the USB Blaster to the JTAG port with the ribbon cable leading off to the right of the board. Turn on the power supply. In the programmer window, press Start to begin the process. Check the Messages pane for programmer output, and verify that there were no errors. Look for "Configuration succeeded" and "Successfully performed operation(s)" messages.

At this point, with your design loaded, you should see the hexadecimal digit currently set on the switches displayed on the 7-segment display. Debug your design until it is fully functional. Good luck!

If you have problems, the following checklist may help:

1. Check the voltage outputs on each of the voltage regulators. Also check it on the adjacent capacitors (C3, C6, C9) to detect a bad connection between the regulator output and the PCB. This is one of the most common soldering problems.
2. Check that the power supply is hooked up correctly. Measure with the voltmeter that you have 5 volts between the V_{in} and GND pins on your FPGA board. Check that the current out of the power supply is less than 200 mA. If the current is high, look for power/ground shorts on your board. Otherwise, if the voltage is incorrect, adjust the power supply to produce the correct output.
3. If the JTAG programmer indicates "Program Failed," first, make sure your board is powered, close the Programmer window and try again. Sometimes programming fails if you power on your board after you open the Programmer window. If programming still fails the problem could be in your board or in the programmer. If programming works on a classmate's board using the same programmer, you may have a bad solder joint or other board error. If the programmer doesn't work on multiple boards, please report it to the instructor.
4. If your power is good but the FPGA still refuses to respond, check the NCONFIG signal (on the RESET button). It should be 1 when the button is not pressed.
5. If the LEDs flicker on and off when you tap on the board or toggle switches, you probably have a loose connection or marginal solder joint somewhere. Two common problems in the past are poor banana plugs that are too small for the receptacles and inadequate solder joints on the voltage regulators.

[2] JTAG stands for the *Joint Test Access Group.* The JTAG interface is a serial interface used to communicate with chips on a board using a few pins during testing and configuration. JTAG is also called Boundary Scan.

6. If the LEDs do something but do not function correctly, the problem is likely in your Quartus schematics or implementation. Check the implementation report file that the pin mapping is what you want. Check for any logic bugs.
7. When exiting the programmer window, don't save anything. That way the design programmed to the PROM or FPGA is always the most recent build.

Programming the PROM with the Serial Flash Loader

Programming over JTAG only changes the volatile SRAM of the FPGA itself and does not write to the non-volatile PROM. The design will only stay on the FPGA until it is reset or power is disconnected (try it!). Programming the PROM directly would require adding an additional programmer port to the board, connected to the Active Serial (AS) interface between the PROM and the FPGA. Instead, it can be programmed over JTAG through the FPGA, using the Serial Flash Loader function in Quartus. JTAG is used to write a temporary design to the FPGA that effectively bridges the JTAG and AS interfaces, allowing the USB Blaster to talk to the PROM without being physically connected to it.

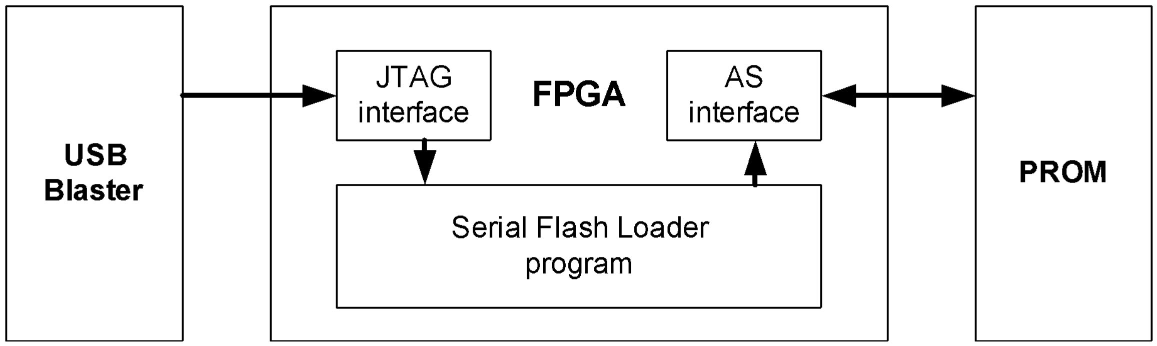


Figure 3 – Serial Flash Loader block diagram. A program bridges the JTAG and Active Serial interfaces to let the USB Blaster talk to the PROM.

When debugging your design, simple JTAG programming has advantages, namely that it is a much faster process. Losing the contents of the FPGA with every reset is less important if your design is being changed with every test. The Serial Flash Loader is much slower than JTAG programming and requires extra steps to complete, but should be used whenever the design is unlikely to be changed in the short term.

Always write your finished labs to the PROM before checkoff. Also remember that whatever design you last programmed to the PROM will be loaded immediately when the FPGA turns on. Forgetting this could cause you massive confusion when debugging, especially in Labs 5-7 when old code on the FPGA might interfere with pins you are trying to use with your ATSAM.

Compile your project to generate an up-to-date .sof file. Next, you will convert the .sof to a JTAG Indirect Configuration (.jic) file for use with the Serial Flash Loader. Choose *File → Convert Programming File*s. Set the programming file type to *JTAG Indirect Configuration File* and the configuration device to *EPCQ16*. Click Advanced and enable the "Disable EPCS ID check" option. Pick a simple file name, such as lab1_xx.jic.

Under Input Files to Convert, select SOF Data and click Add File. Find your lab1_xx.sof. It is in the output_files directory. Press OK. Now highlight Flash Loader and click Add Device. Select Cyclone IV E in the left pane, then EP4CE6 in the right pane, and click OK. Click *Generate* and verify the .jic was generated successfully, then close the window.

Launch the Programmer and remove your old lab1_xx.sof from the programming file list. Now add the lab1_xx.jic file you just generated. Check both Program / Configure boxes and click Start. Watch the Messages pane for any errors. When the process completes, your design is loaded on the PROM. It will automatically be loaded onto the FPGA after reset or power-on until the Serial Flash Loader is used again to replace it. If you choose Tools -> Options -> Initiate Configuration after Programming, you won't have to hit reset after the first programming.

If you want to erase the EPROM, change the EPCQ16 option from Program/Configure to Erase and click Start again.

When you are finished, save you files somewhere (such as your network drive or a USB key) and remove the files from the local machine. Good luck!

What to Turn In

For this lab and all subsequent ones, turn in a lab report. The report should not exceed one page of text, plus schematics, code, and anything else appropriate, such as diagrams, simulation results, or calculations. The report typically has the following sections:

- **Introduction**: Briefly explain what was done.
- **Design and Testing Methodology**: Explain how you approached the design of this assignment from both a software and a hardware standpoint (as appropriate). Include how you tested your design. These tests should convince the reader that the requirements of the assignment have been met.
- **Technical Documentation**: Include your Verilog code and schematics of your circuits.
  - Quality and clarity of your code is important. Make sure it is adequately commented. Succinct code using standard idioms is best.
  - Schematics of your breadboarded circuits should be sufficient for another engineer to understand and reconstruct the circuit on the breadboard. Always use standard symbols for standard components such as resistors, switches, transistors, diodes, etc. Give the component name or part number such that the reader could order parts and replicate your circuit, or look up components in a datasheet where necessary. The reader shouldn't have to open Quartus to relate your Verilog code to the schematic, and shouldn't need to refer to a data sheet to wire external components or understand what the connections are. Don't assume that the reader has memorized the pinouts of any chips. Therefore, you'll need to label both the pin number and pin name for each pin you use from the FPGA board or other component (e.g., 7-segment display). There is no need to draw any of the circuitry on the board; just refer to it by the pins number and name.
- **Results and Discussion**: Did you accomplish all of the prescribed tasks? If not, what are the shortcomings? How might you address them given more time? As appropriate,

how did the design perform (ex. How fast/accurate/reliable was it?). Is there anything you would do differently if you were to redo the lab? Is there anything else interesting worth mentioning?

- **Conclusions**: Briefly summarize what was done and how it performed.
  - How many hours did you spend on the lab? Any comments, suggestions, or complaints about the assignment? This will not count toward your grade, but will help refine the lab for the future.

The report does not need to be long but should be complete. Some individual questions may not apply to this particular lab but are listed to give you a general idea of what is desired. Future reports will follow a similar format and the questions may be more applicable in these instances.

Have your lab checked off by the instructor. You will need to demonstrate that the board and 7-segment display operate correctly. You will also be asked a question about some part of the lab or your board. You should be thoroughly familiar with all of the lab and the components of your board to be able to answer the question. The oral exam is typically in the form of a "Fault-Tolerance Question." What would happen if a particular wire is broken or a pin is shorted to V_{CC} or GND? Be prepared for any other questions about your lab, however.

Acknowledgments:

This lab manual and previous utility boards have been developed by Profs. Matthew Watkins, David Money Harris, and Sarah Harris, Alex Alves '16, Gourav Khadge '15, Leo Altmann '11, Christian Jolivet '11, Elizabeth Reynolds '02, Marty Weiner '02, Fernando Mattos '00, and Eliot Gerstner '99.

Appendix: FPGA Initialization Sequence

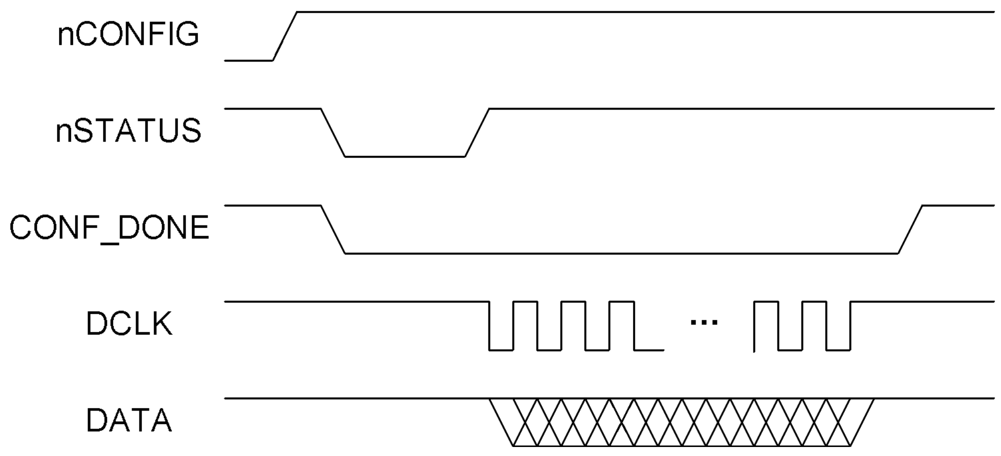
If your FPGA board is assembled incorrectly or your PROM is programmed wrong, you may find that your FPGA fails to initialize. This sheet documents the initialization process to help you track down your problem. The initialization sequence is described in more detail in pages 8-6 through 8-10 of the Cyclone 4 Device Handbook (vol. 1).

The MSEL[2:0] pins on the FPGA are used to select a configuration scheme. They are connected to GND, VCC and GND respectively to indicate Active Serial configuration at 3.3V levels.

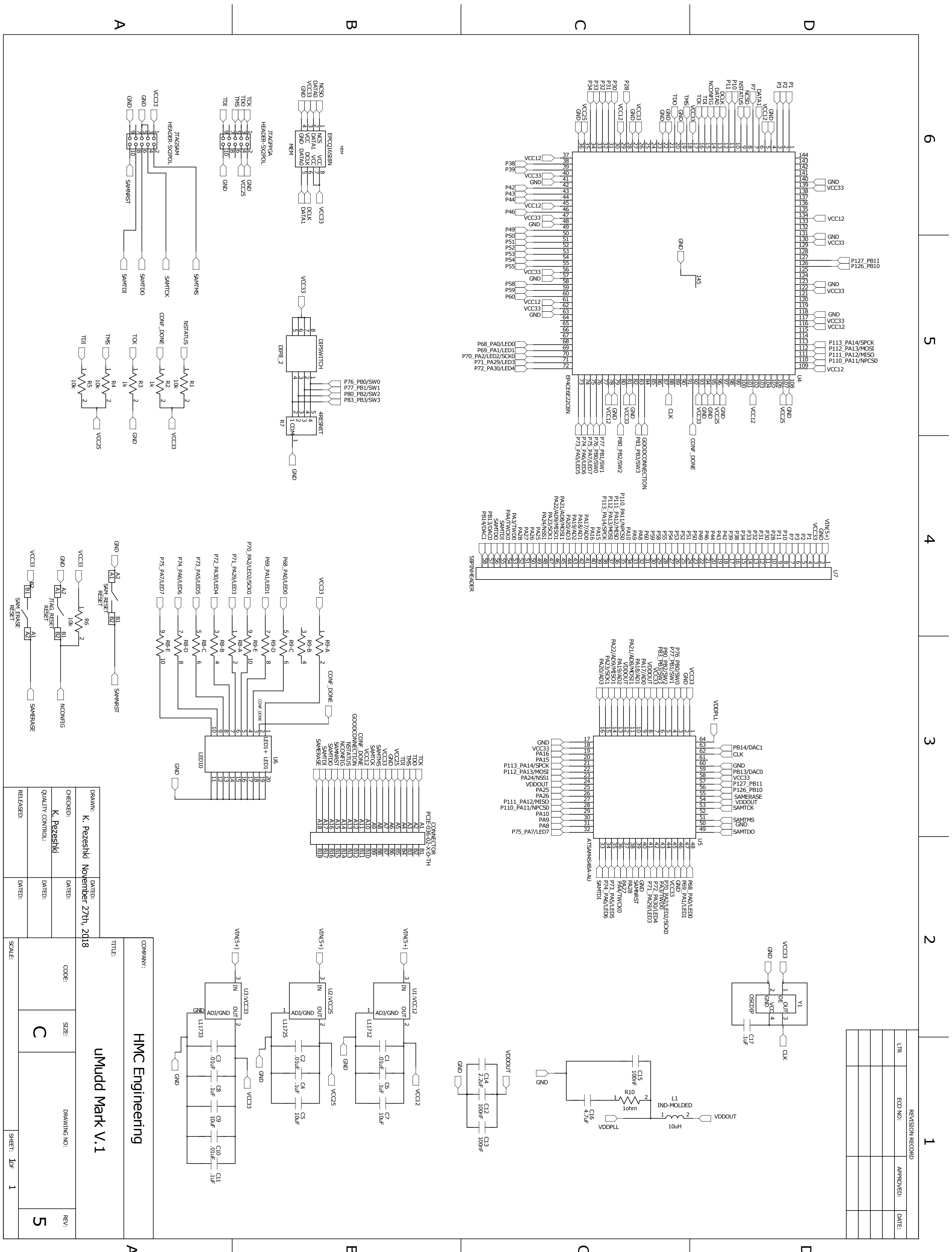
When the FPGA powers on or you release the reset switch (pulling nCONFIG from low to high), the device begins initialization, pulling nSTATUS and CONF_DONE low while clearing internal memory and preparing for configuration. In < 200ms, nSTATUS is then pulled high to indicate the start of configuration.

During configuration, the FPGA generates a 40 MHz clock via an internal oscillator and transmits the signal via DCLK to the EPCQ16 PROM. The PROM responds by sending serial configuration data back over the DATA connection. The FPGA has 3,000,000 bits of internal state, so serial configuration via PROM should complete in about 100ms. When configuration is complete, CONF_DONE is pulled high again, and the device enters user mode < 0.5ms later. If CONF_DONE is never asserted or nSTATUS is pulled low after initialization completes, a configuration error has occurred. Check the soldering on the FPGA and PROM. CONF_DONE is also output to the second LED on the 10LED array.

The configuration waveforms are shown below:



Part Description	Part Identifier	Manufacturer	Manufacturer P/N	Supplier	Supplier P/N	Quantity	Unit Price	Total Price
PCB		Advanced Circuits				1	$ 15.03	$ 15.03
Cyclone IV FPGA	U6	Altera	EP4CE6E22C8N	Digikey	544-2746-ND	1	$ 11.95	$ 11.95
FPGA flash	U5	Altera	EPCQ16ASI8N	Digikey	544-3440-ND	1	$ 7.35	$ 7.35
Atmel SAM4S4B	U8	Microchip technology	ATSAM4S4BA-AU	Digikey	ATSAM4S4BA-AU-ND	1	$ 3.93	$ 3.93
Quad DIP switch	U9	Grayhill	76SB04	Digikey	GH7170-ND	1	$ 0.92	$ 0.92
1.2 V low-dropout regulator	U1	ST	LD117DT12TRI	Digikey	497-1231-1-ND	1	$ 1.16	$ 1.16
2.5 V low-dropout regulator	U2	ST	LD117DT25CTR	Digikey	497-1233-1-ND	1	$ 1.16	$ 1.16
3.3 V low-dropout regulator	U3	ST	LD117DT33CTR	Digikey	497-1235-1-ND	1	$ 1.16	$ 1.16
SPST pushbutton switch	PB1, PB2, PB3	Panasonic	EVQ-PAE04M	Digikey	P8008S-ND	3	$ 0.29	$ 0.87
10-segment LED array	U10	Lumex	SSA-LXB10IW-GF/LP	Digikey	67-1010-ND	1	$ 2.85	$ 2.85
330 Ω 5 resistor network	R8, R9	Bournes	4610X-2-331LF	Digikey	4610X-2-331LF-ND	2	$ 0.29	$ 0.57
FPGA download connector	JTAGFPGA	Tyco	5103309-1	Digikey	A33160-ND	1	$ 0.76	$ 0.76
36-pin header	U11	3M	929400-01-36-RK	Digikey	929400E-01-36-ND	2	$ 1.32	$ 2.65
2.2 KΩ 4 resistor network	R7	Bourns Inc.	4605X-101-222LF	Digikey	4605X-101-222LF-ND	1	$ 0.51	$ 0.51
1 KΩ resistor	R2, R3	Panasonic Electronic Components	ERJ-6GEYJ102V	Digikey	P1.0KACT-ND	2	$ 0.10	$ 0.20
10 KΩ resistor	R1, R4, R5, R6	Panasonic Electronic Components	ERJ-6GEYJ103V	Digikey	P10KACT-ND	4	$ 0.10	$ 0.40
1 Ω resistor	R10	Bourns Inc.	CRS0805-FW-1R00ELF	Digikey	CRS0805-FW-1R00ELFCT-ND	1	$ 0.39	$ 0.39
100 KΩ resistors	R11, R12, R13	Panasonic Electronic Components	ERJ-6GEYJ104V	Digikey	P100KACT-ND	3	$ 0.10	$ 0.30
0.1 μF capacitor	C4, C6, C8, C11, C12, C13, C15, C17	Samsung Electro-Mechanics America, Inc	CL21F104ZBCNNNC	Digikey	1276-1007-1-ND	8	$ 0.10	$ 0.80
0.01 μF capacitor	C1, C2, C3, C10	Murata Electronics North America	GRM216R71H103KA01D	Digikey	490-1664-1-ND	4	$ 0.10	$ 0.40
10 μF capacitor	C5, C7, C9	Samsung Electro-Mechanics America, Inc	CL21A106KPFNNNG	Digikey	1276-6456-1-ND	3	$ 0.14	$ 0.42
2.2 μF capacitor	C14	AVX Corporation	0805ZG225ZAT4A	Digikey	478-12511-1-ND	1	$ 0.41	$ 0.41
4.7 μF capacitor	C16	Murata Electronics North America	GRT21BC8YA475KE13L	Digikey	490-12361-1-ND	1	$ 0.45	$ 0.45
10 μH inductor	L1	Bourns Inc.	77F100K-TR-RC	Digikey	77F100K-TR-RCTR-ND	1	$ 0.10	$ 0.10
SAM download connector	JTAGSAM	Samtec	FTSH-105-01-F-D-K	Digikey	SAM8909-ND	1	$ 2.74	$ 2.74
40 MHz oscillator	Y1	TXC Corporation	9B-40.000MAAJ-B	Digikey	887-2030-ND	1	$ 0.39	$ 0.39
Total								**$ 57.86**



COMPANY: HMC Engineering

TITLE: uMudd Mark V.1

DRAWN: K. Pezeshki DATED: November 27th, 2018

CHECKED: DATED:

QUALITY CONTROL: K. Pezeshki DATED:

RELEASED: DATED:

CODE: SIZE: C DRAWING NO: REV: 5

SCALE: SHEET: 1 OF 1

REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE: