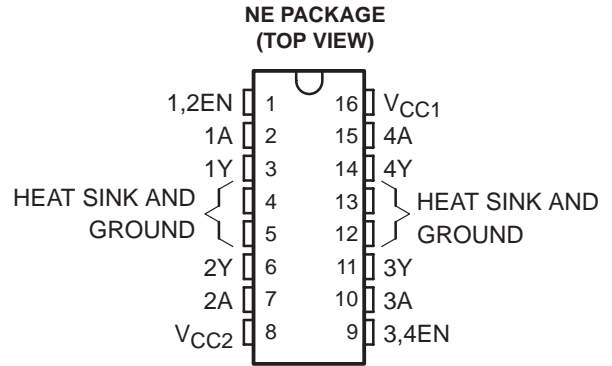


SN754410 QUADRUPLE HALF-H DRIVER

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- 1-A Output-Current Capability Per Driver
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- Designed for Positive-Supply Applications
- Wide Supply-Voltage Range of 4.5 V to 36 V
- TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- Input Hysteresis Improves Noise Immunity
- 3-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- No Output Glitch During Power Up or Power Down
- Improved Functional Replacement for the SGS L293



FUNCTION TABLE
(each driver)

INPUTS [†]		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level, L = low-level
X = irrelevant
Z = high-impedance (off)
[†] In the thermal shutdown mode, the output is in a high-impedance state regardless of the input levels.

description

The SN754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents up to 1 A at voltages from 4.5 V to 36 V. The device is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL-and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

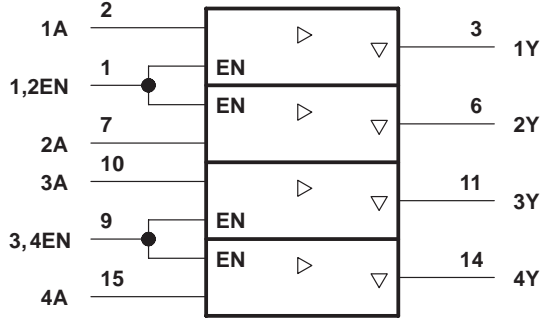
A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage V_{CC2} is used for the output circuits.

The SN754410 is designed for operation from -40°C to 85°C .

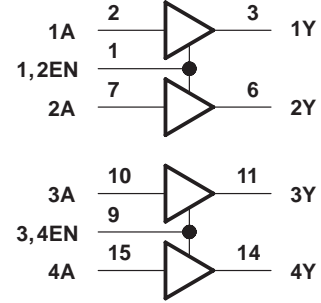
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logic symbol†

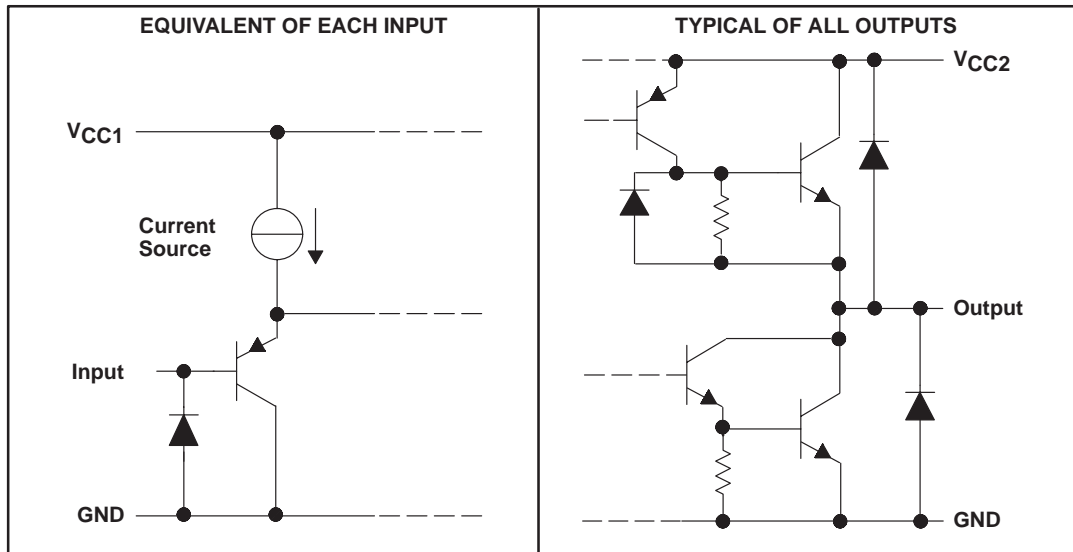


logic diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Output supply voltage range, V_{CC1} (see Note 1)	–0.5 V to 36 V
Output supply voltage range, V_{CC2}	–0.5 V to 36 V
Input voltage, V_I	36 V
Output voltage range, V_O	–3 V to $V_{CC2} + 3$ V
Peak output current (nonrepetitive, $t_w \leq 5$ ms)	± 2 A
Continuous output current, I_O	± 1.1 A
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075 mW
Operating free-air temperature range, T_A	–40°C to 85°C
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network GND.
 2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

	MIN	MAX	UNIT
Output supply voltage, V_{CC1}	4.5	5.5	V
Output supply voltage, V_{CC2}	4.5	36	V
High-level input voltage, V_{IH}	2	5.5	V
Low-level input voltage, V_{IL}	–0.3‡	0.8	V
Operating virtual junction temperature, T_J	–40	125	°C
Operating free-air temperature, T_A	–40	85	°C

‡ The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.



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electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -12 \text{ mA}$		-0.9	-1.5	V
V_{OH} High-level output voltage	$I_{OH} = -0.5 \text{ A}$	$V_{CC2} - 1.5$	$V_{CC2} - 1.1$		V
	$I_{OH} = -1 \text{ A}$	$V_{CC2} - 2$			
	$I_{OH} = -1 \text{ A}, T_J = 25^\circ\text{C}$	$V_{CC2} - 1.8$	$V_{CC2} - 1.4$		
V_{OL} Low-level output voltage	$I_{OL} = 0.5 \text{ A}$		1	1.4	V
	$I_{OL} = 1 \text{ A}$			2	
	$I_{OL} = 1 \text{ A}, T_J = 25^\circ\text{C}$		1.2	1.8	
V_{OKH} High-level output clamp voltage	$I_{OK} = -0.5 \text{ A}$		$V_{CC2} + 1.4$	$V_{CC2} + 2$	V
	$I_{OK} = 1 \text{ A}$		$V_{CC2} + 1.9$	$V_{CC2} + 2.5$	
V_{OKL} Low-level output clamp voltage	$I_{OK} = 0.5 \text{ A}$		-1.1	-2	V
	$I_{OK} = -1 \text{ A}$		-1.3	-2.5	
$I_{OZ(off)}$ Off-state high-impedance-state output current	$V_O = V_{CC2}$			500	μA
	$V_O = 0$			-500	
I_{IH} High-level input current	$V_I = 5.5 \text{ V}$			10	μA
I_{IL} Low-level input current	$V_I = 0$			-10	μA
I_{CC1} Output supply current	$I_O = 0$	All outputs at high level		38	mA
		All outputs at low level		70	
		All outputs at high impedance		25	
I_{CC2} Output supply current	$I_O = 0$	All outputs at high level		33	mA
		All outputs at low level		20	
		All outputs at high impedance		5	

† All typical values are at $V_{CC1} = 5 \text{ V}$, $V_{CC2} = 24 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC1} = 5 \text{ V}$, $V_{CC2} = 24 \text{ V}$, $C_L = 30 \text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{d1} Delay time, high-to-low-level output from A input	See Figure 1		400		ns	
t_{d2} Delay time, low-to-high-level output from A input			800		ns	
t_{TLH} Transition time, low-to-high-level output				300		ns
t_{THL} Transition time, high-to-low-level output				300		ns
t_r Rise time, pulse input						
t_f Fall time, pulse input						
t_w Pulse duration						
t_{en1} Enable time to the high level	See Figure 2		700		ns	
t_{en2} Enable time to the low level			400		ns	
t_{dis1} Disable time from the high level				900		ns
t_{dis2} Disable time from the low level				600		ns



PARAMETER MEASUREMENT INFORMATION

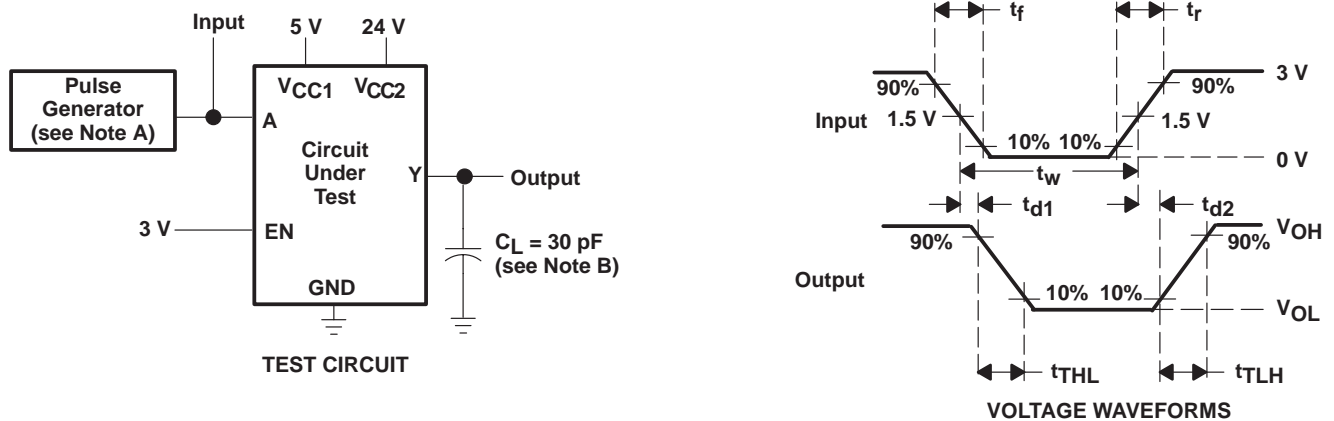


Figure 1. Test Circuit and Switching Times From Data Inputs

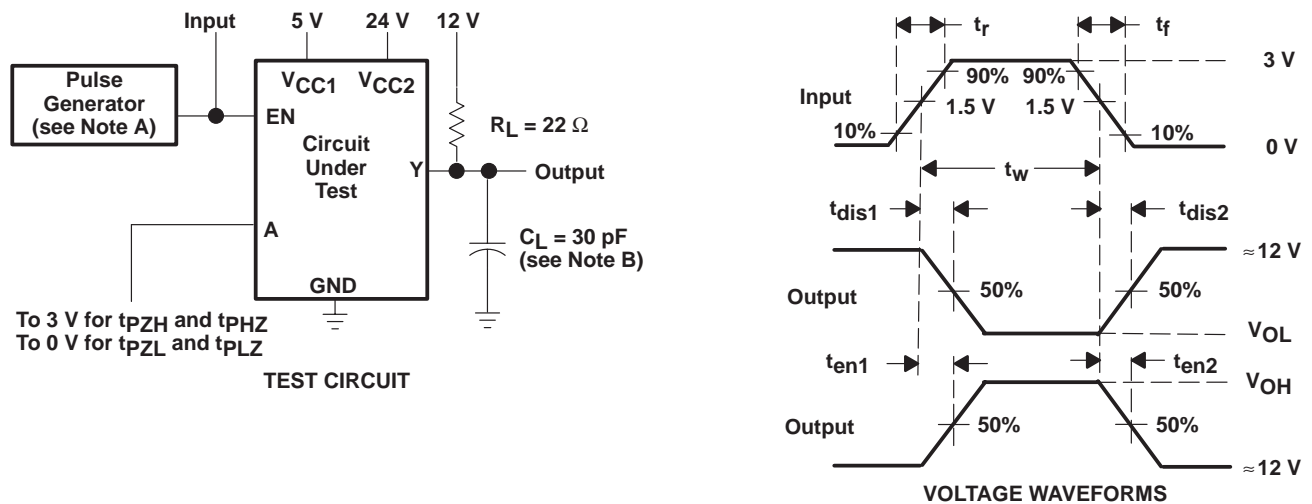


Figure 2. Test Circuit and Switching Times From Enable Inputs

- NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $t_w = 10 \mu\text{s}$, $\text{PRR} = 5 \text{ kHz}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

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APPLICATION INFORMATION

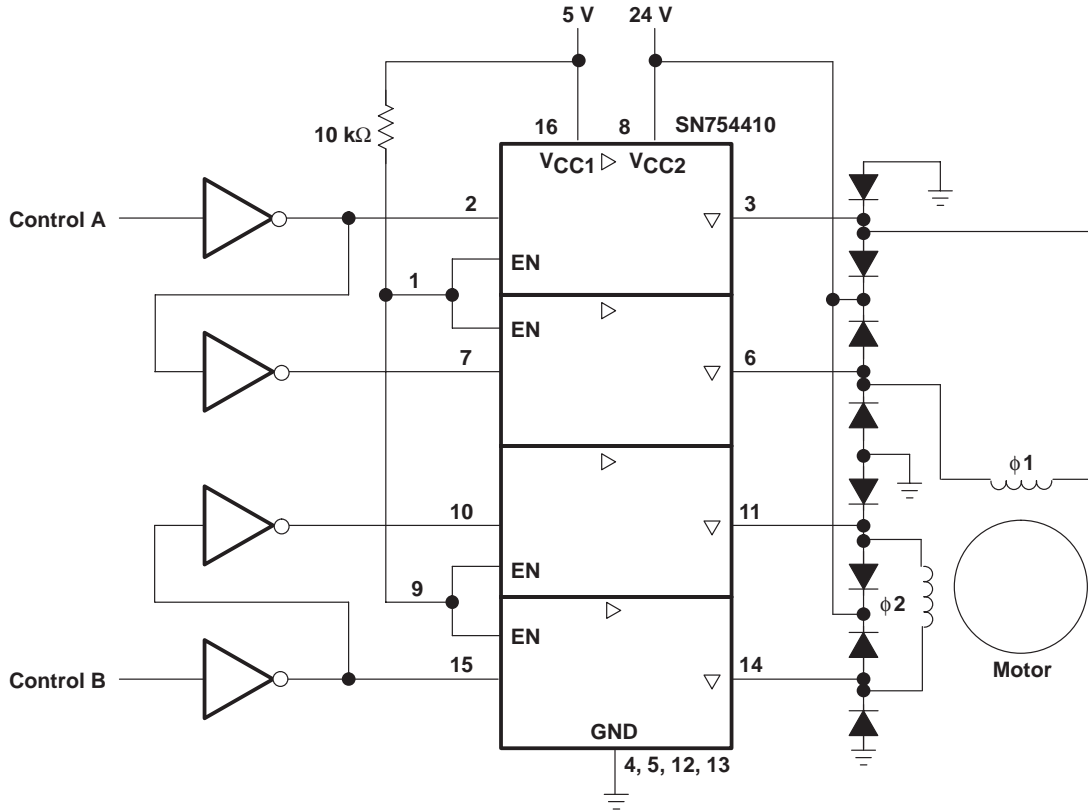


Figure 3. Two-Phase Motor Driver