RISC-V

System-on-Chip Design

Harris, Stine, Thompson, & Harris

Chapter 6:

Logic Synthesis

Chapter 6 :: Topics

Logic Synthesis

6.1 Performance, Power, and Area (PPA)
6.2 Fabrication Technologies
6.3 Running Synthesis
6.4 Reviewing Log Files
6.5 Wally Synthesis Results

Logic Synthesis

- **Converts RTL (Verilog) to hardware**
  - Maps it onto a library of cells
  - Attempts to minimize area and power while meeting timing constraints

Logic Synthesis

- **Process**
  - **Reads** RTL, constraints, standard cell libraries (i.e., registers, adders, etc.), and technology file (i.e., # metal layers, width and spacing of metal and vias, etc.)
  - **Analyzes** design for syntax errors
  - **Elaborates** design to map to generic library
  - **Compiles** to map to actual cell library
  - **Physical synthesis:** approximate cell placement
  - **Place & route:** places and wires together cells

Chapter 6: Logic Synthesis

Performance, Power, and Area (PPA)

Performance, Power, Area (PPA)

Figures of merit in synthesis:

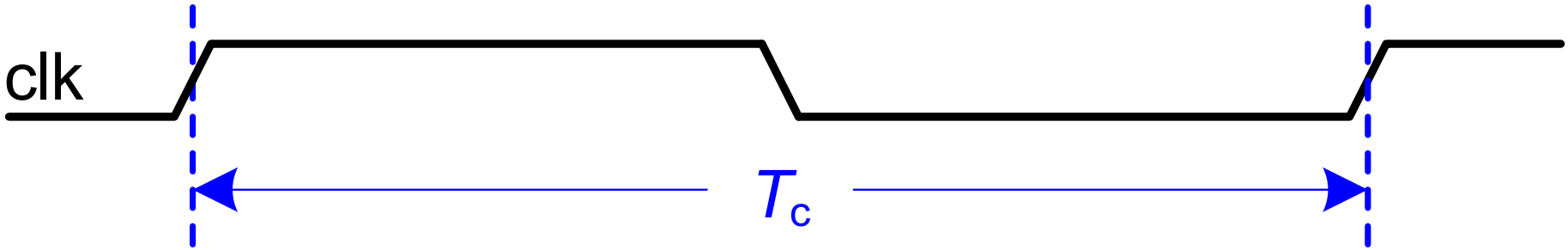
- **Performance:** clock frequency
- **Power:** power drawn (watts)
- **Area:** chip space (also indicates cost)

Chapter 6: Logic Synthesis

Performance

Performance

- **Performance is determined by frequency**
  - **T_c = cycle time (clock period)**
  - **F = frequency. F = $1/T_c$**
- **Example:**
  - T_c = 0.25 ns
  - F = $1/T_c$ = 1/(0.25 ns) = 4 GHz

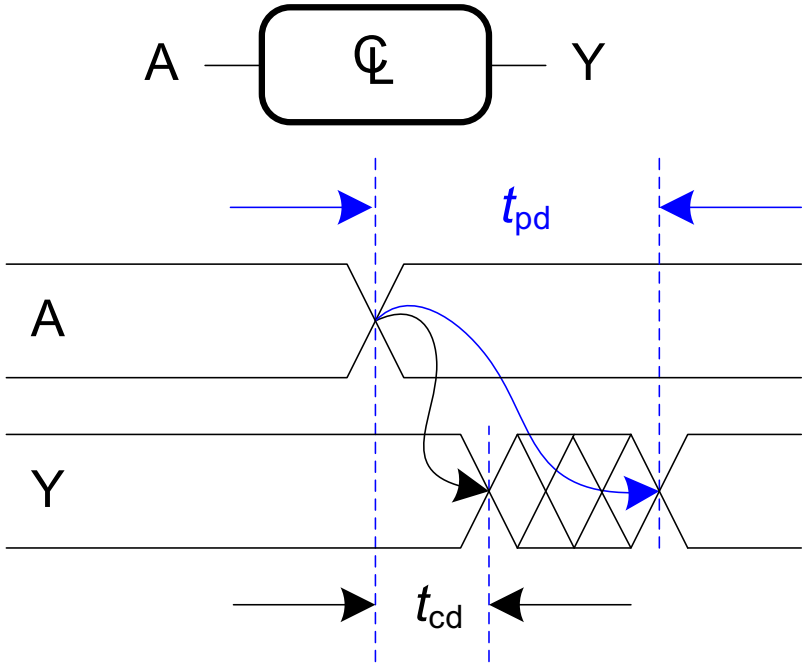


T_c is determined by:

- **Combinational logic delays**
- **Flip-flop timing**

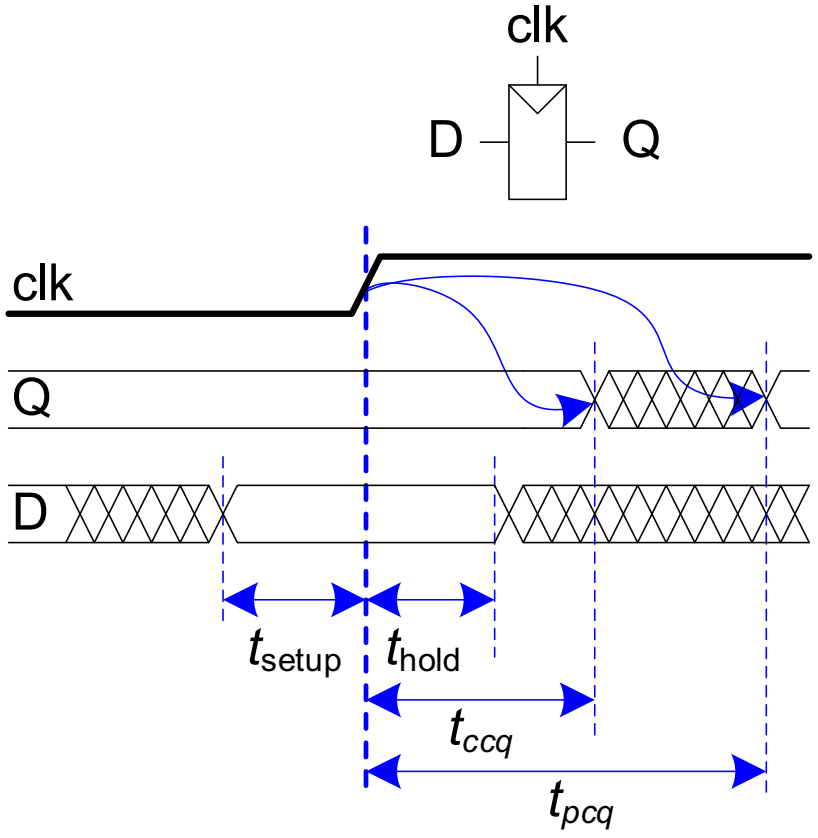
Timing Constraints

- **Combinational Logic (CL) timing:**
  - **Minimum delay** from input changing to output changing: contamination delay (t_{cd})
  - **Maximum delay** from input changing to output changing: propagation delay (t_{pd})



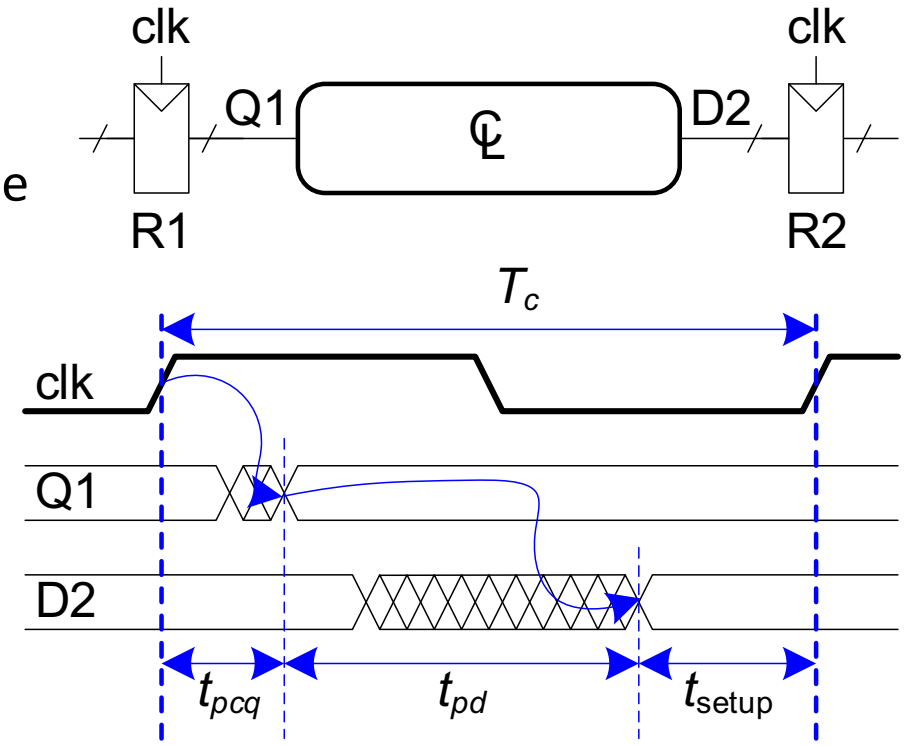
Timing Constraints

- **Flip-flop timing:**
  - **Input constraint:**
    - Input D must be stable:
      - a setup time (t_{setup}) before clock edge and
      - a hold time (t_{hold}) after the clock edge
  - **Output constraint:**
    - Output Q changes:
      - at a minimum of t_{ccq} (contamination clock-to-q) after clock edge
      - at a maximum of t_{pcq} (propagation clock-to-q) after clock edge



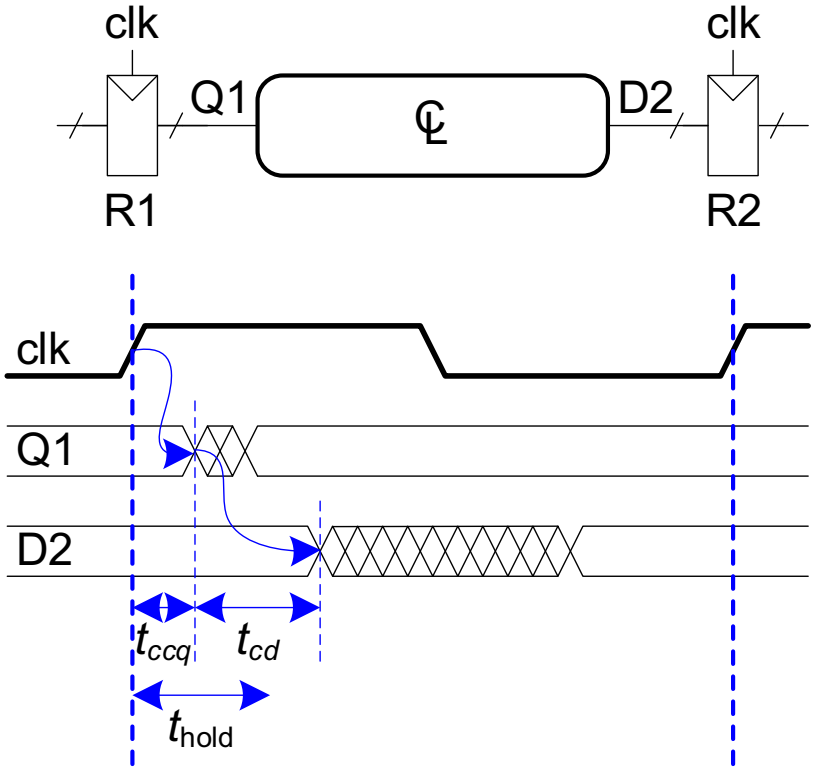
Timing Analysis: Setup Constraint

- **Cycle time (T_c):**
  - Must be long enough for:
    - R1 to produce **Q1** (t_{pcq})
    - Combinational logic to produce **D2** (t_{pd})
    - D2 to setup into **R2** (t_{setup})
  - Thus,
    - $T_c \geq t_{pcq} + t_{pd} + t_{setup}$



Timing Analysis: Hold Time Constraint

- **Hold time (t_{hold}):**
  - Must be shorter than the fast path from R1 to R2:
    - Min delay for R1 to produce **Q1** (t_{ccq})
    - Min delay for combinational logic to produce **D2** (t_{cd})
  - Thus,
    - $t_{hold} < t_{ccq} + t_{cd}$



Timing Analysis Summary

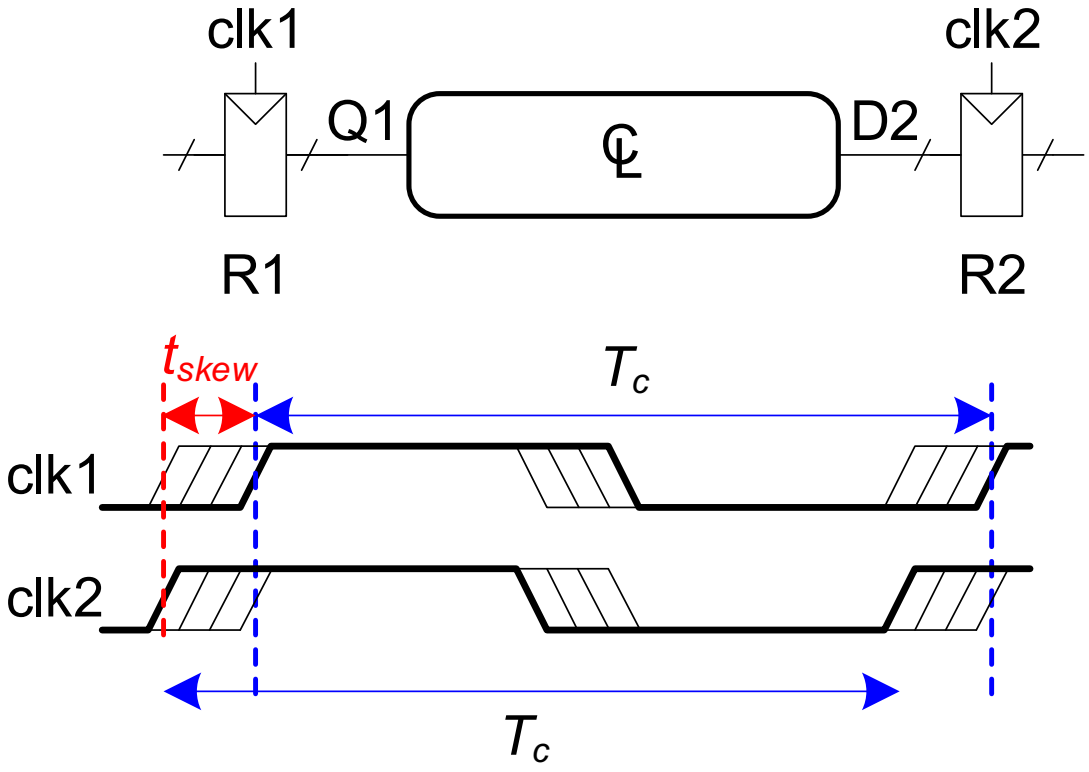
- Timing analysis requires that both the **setup and hold time constraints are met**:
  - Setup time constraint:

    $T_c \geq t_{pcq} + t_{pd} + t_{setup}$
  - Hold time constraint:

    $t_{hold} < t_{ccq} + t_{cd}$

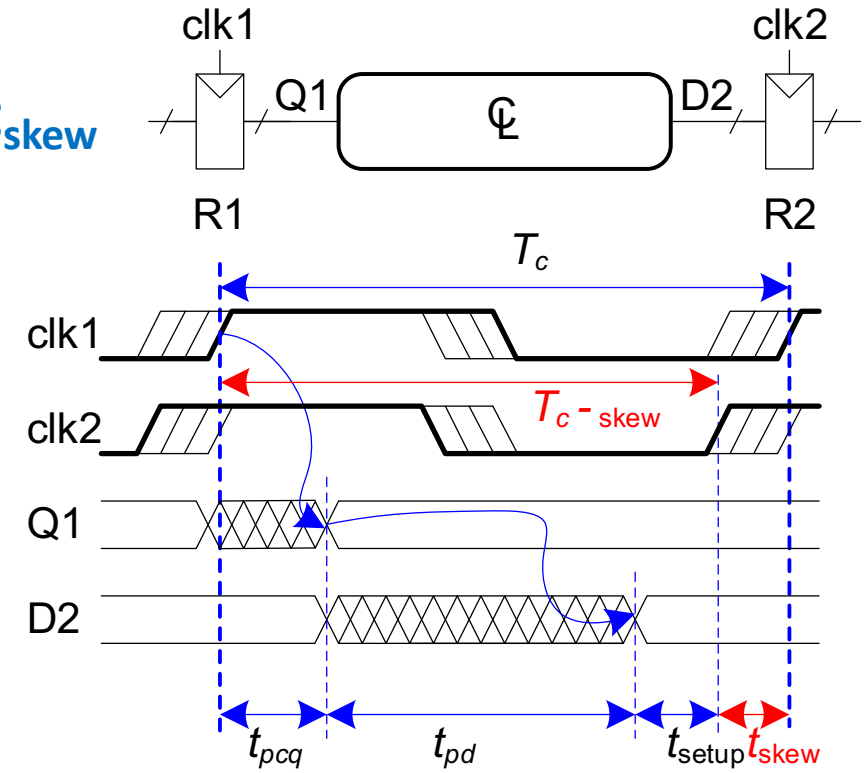
Timing Analysis with Skew

- **Skew:** delay between adjacent clock edges
  - clk1 and clk2 have the **same cycle time** (T_c)
  - **t_{skew} is the maximum delay** between adjacent clocks



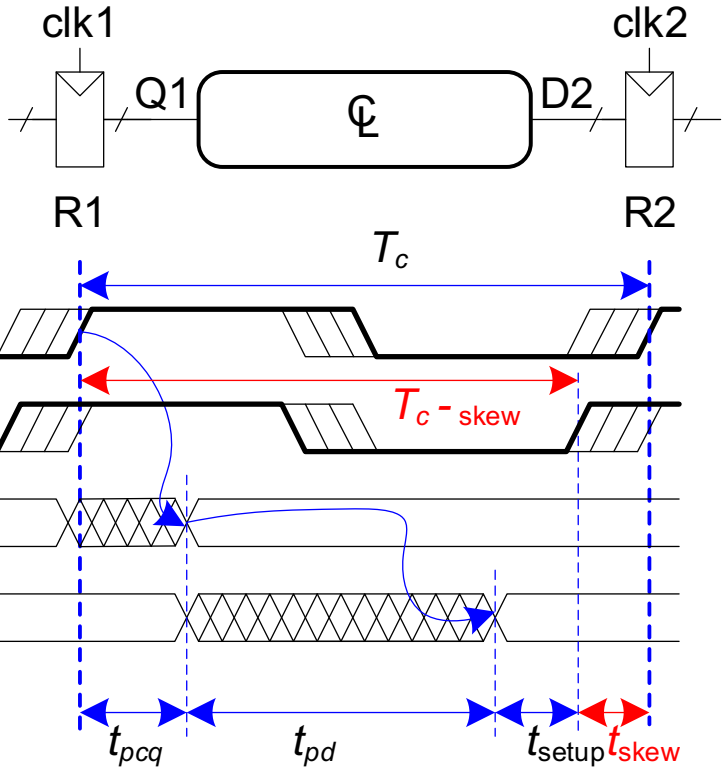
Setup Constraint with Skew

- **Now have less time to do work**
  - clk1 edge to clk2 edge = $T_c - t_{skew}$
- Thus,
  - $T_c - t_{skew} \geq t_{pcq} + t_{pd} + t_{setup}$
  - $T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$



Setup Constraint with Skew

- **Now there is less time to do the work**
  - clk1 edge to clk2 edge = $T_c - t_{skew}$
- Thus,
  - $T_c - t_{skew} \geq t_{pcq} + t_{pd} + t_{setup}$
  - $T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$



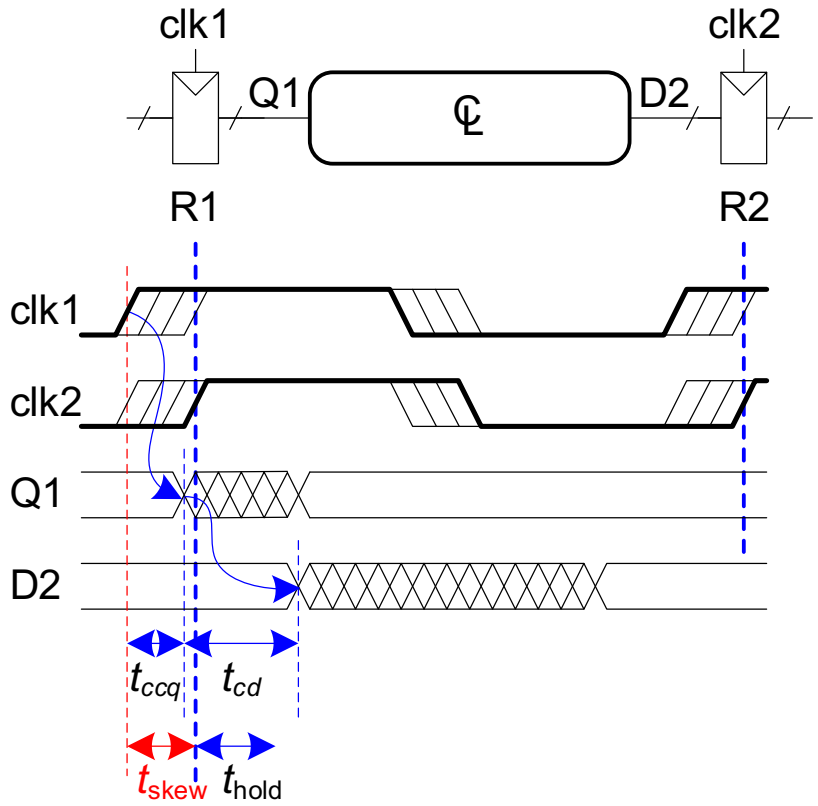
Skew **increases cycle time** (T_c) by t_{skew} – thus decreasing frequency / performance.

Hold Time Constraint with Skew

- **Now, R2's hold time doesn't start till t_{skew} later:**
  - So, D2 must now be held stable for $\mathbf{t_{hold} + t_{skew}}$ after clk1's rising edge.
- Thus,
  - $\mathbf{t_{hold} + t_{skew}} < t_{ccq} + t_{cd}$
  - $\mathbf{t_{hold}} \quad\quad\quad\quad\quad\quad < \mathbf{t_{ccq} + t_{cd} - t_{skew}}$

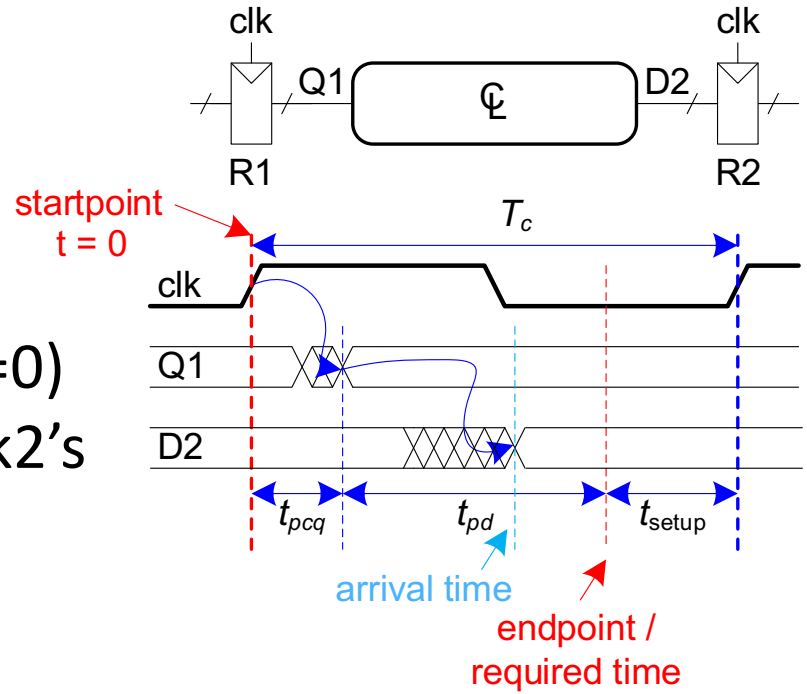
This is a **harder constraint to meet** than without skew:

$$t_{hold} < t_{ccq} + t_{cd}$$



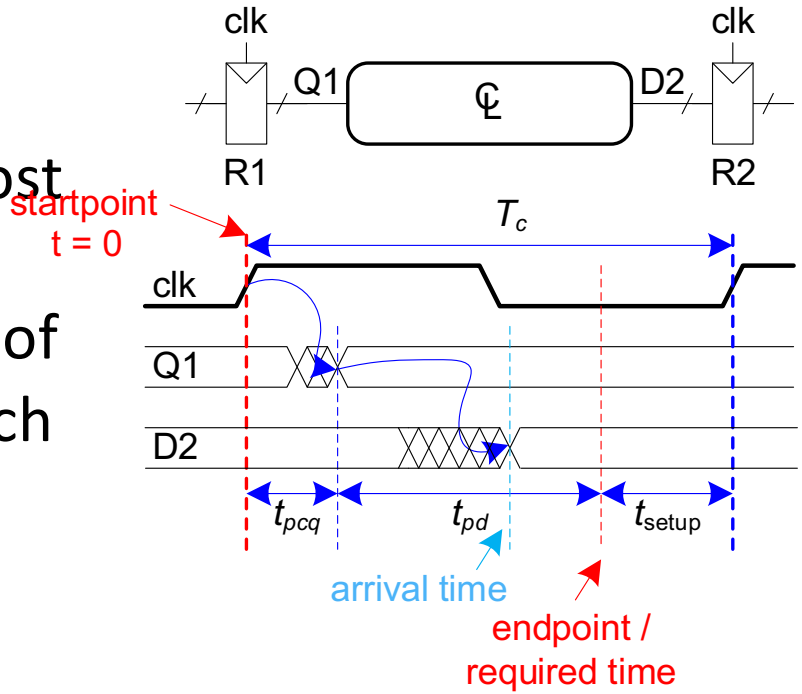
Static Timing Analysis

- Calculates **worst-case delay (t_{pcq} + t_{pd}) between clocked elements**
- **Definitions:**
  - **startpoint:** clk1's rising edge (t=0)
  - **endpoint:** setup time before clk2's next rising edge
  - **required time:** $T_c - t_{setup}$
  - **arrival time:** $t_{pcq} + t_{pd}$
  - **slack:** required time – arrival time
    - Positive slack: circuit works
    - Negative slack: circuit doesn't work



Static Timing Analysis, cont'd

- **slack:** required time – arrival time
  - **WNS** = worst negative slack: most negative slack of all paths
  - **TNS** = total negative slack: sum of negative slack of all paths at each endpoint
  - **Critical path** = path with WNS



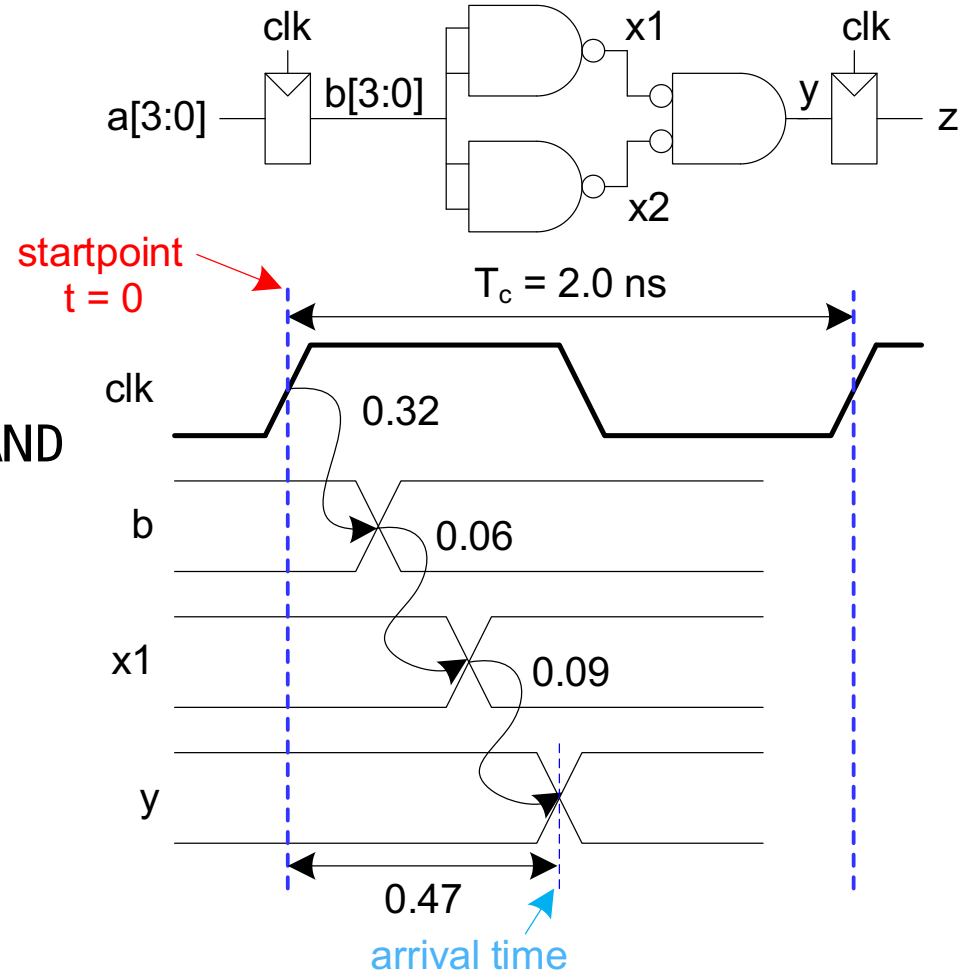
Static Timing Analysis, cont'd

- Synthesis tool tries to **meet target clock period** by:
  - **Decreasing delay of critical path** (path with WNS)
    - By using faster cells, etc.
- If the synthesis tool cannot meet the target clock period, the **designer can try to redesign the RTL:**
  - Simplify logic
  - Move logic between pipeline stages
  - Etc.

Example Timing Analysis

```
module example (
  input  logic        clk,
  input  logic [3:0] a,
  output logic        q);

  flop #(4) f1(clk, a, b);
  assign y = &b; // 4-input AND
  flop #(1) f2(clk, y, q);
endmodule
```



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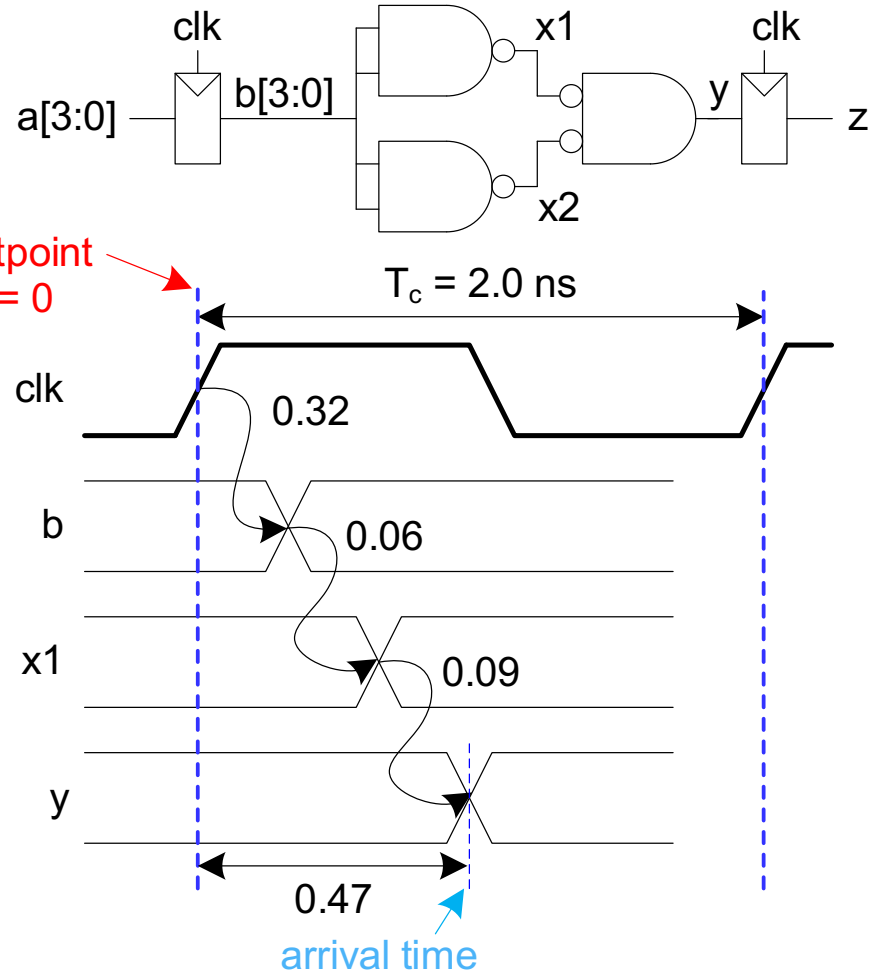


- Target clock period: $\mathbf{T_c}$ = 2 ns
- $\mathbf{t_{pcq}}$ = 0.32 ns
- $\mathbf{t_{setup}}$ = 0.13 ns
- **required time** = $T_c - t_{setup}$ = (2 – 0.13) ns = 1.87 ns
- **arrival time** = 0.47 ns
- **slack** = required time – arrival time = (1.87 – 0.47) ns = **1.4 ns**

Slack is **positive**, so this circuit functions correctly.

Chapter 6: Logic Synthesis

Power

Power

- **Dynamic power:** toggling between 1 and 0 (charging/discharging capacitance)
- **Static power:** some leakage current

Power is Proportional to frequency

- **Power consumption: $P = E/T_c = Ef$**
  - ***E*: Energy consumed per clock period**
  - **T_c: Clock period**
  - ***f*: frequency (= $1/T_c$)**

Dynamic power

- **Dynamic power:** toggling between 1 and 0 (charging/discharging capacitance)
  - All transistors and wires have some capacitance (on the order of fF = 10^{-15} F)
  - Energy to charge a capacitor to V_{dd}: $\boldsymbol{E_{dyn} = CV_{dd}^2}$
  - A signal that rises and falls every clock cycle consumes power: $\boldsymbol{P_{dyn} = CV_{dd}^2 f}$
  - α = **activity factor:** how often a circuit switches. A signal that rises or falls every cycle has $\alpha = ½$
    - $\boldsymbol{P_{dyn} = \alpha CV_{dd}^2 f}$
  - Dynamic power is computed for each component and then summed.

Static Power

- **Static power:** some leakage current
  - Transistors that are supposed to be off actually draw a small amount of current (leakage current).
  - $P_{leak} = I_{leak} V_{dd}$

Power and Area

- Energy depends on number and size of components.
- So, **minimizing area is a rough proxy for minimizing power.**
- **Example:**
  - Wally's floating-point divide/square root unit:
  - Consumes: **0.28 fJ/μm²/cycle** on average (TSMC 28hpm process under typical conditions)

Chapter 6: Logic Synthesis

Area

Area

- Synthesis makes **design trade-offs**:
  - May choose different **algorithms** for implementation:
    - **Example:** ripple-carry adder is slow but small, prefix adder is fast but large.
  - May choose cell with different **drive strength**.
    - **Example:** choosing between different flavors of cells:
      - An AND gate that is slow but small, or
      - An AND gate that is fast but large (wider transistors – so, higher drive strength and faster – but also more area and power)

Chapter 6: Logic Synthesis

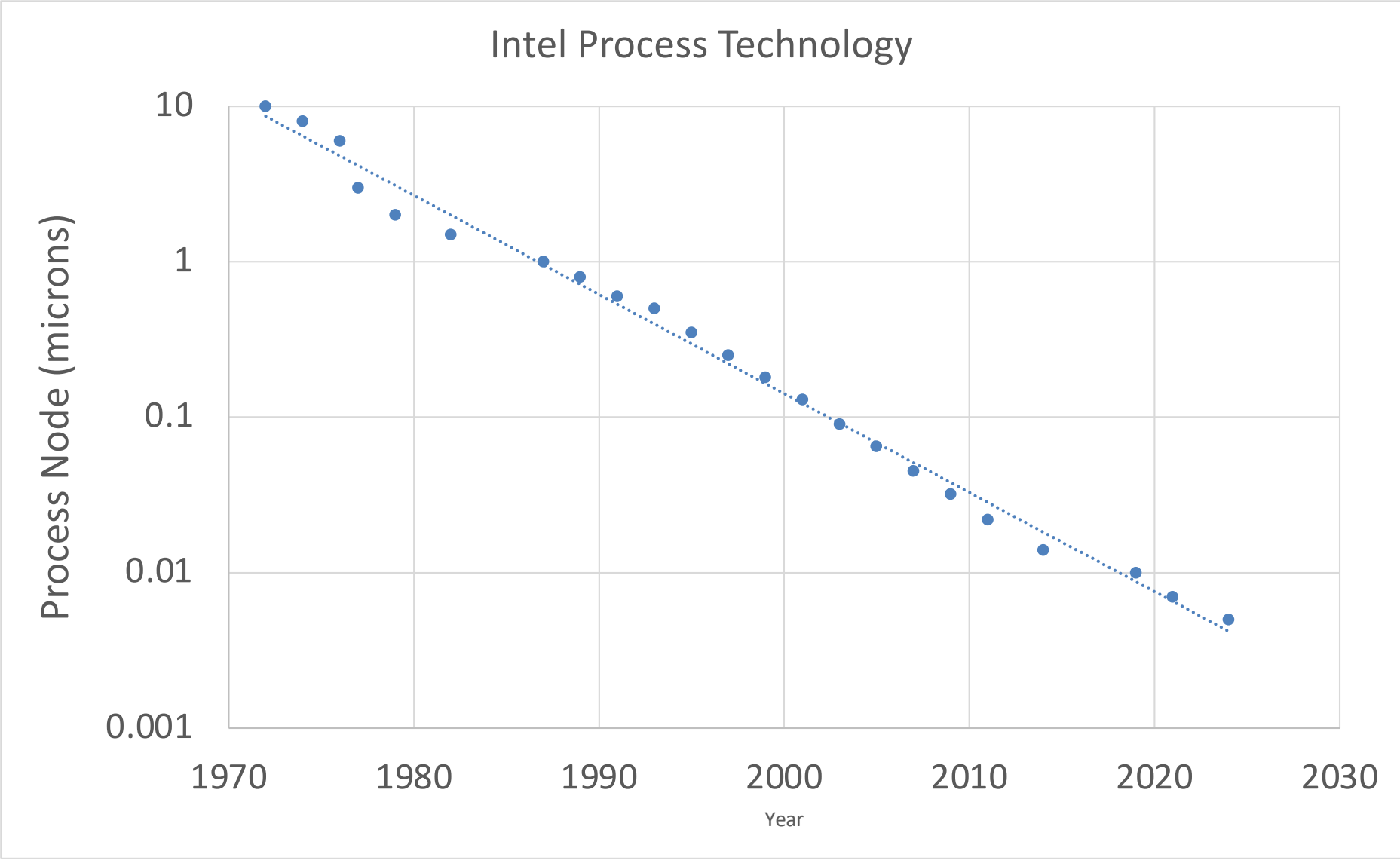
Fabrication Technologies

Fabrication Technologies

- Process node or feature size:
  - Used to be transistor gate length
  - **Planar process:** 1972-2009
    - Process node/feature size was the gate length
    - Smaller gate length = lower power, faster, smaller
    - Smaller process node # = smaller gate length (i.e., 28 nm = gate length of 28 nm)
  - **FinFET:** 2009+
    - Turned transistor on side to reduce leakage current
    - Lower number corresponds to higher performance, but no longer gate length
    - **Example:** Compared to TSMC 5-nm process, TSMC 3-nm is:
      - 33% more dense
      - 10% - 15% faster at the same power or
      - 25% to 30% lower power at the same speed

https://www.techradar.com/news/the-future-of-leading-edge-chips-according-to-tsmc-5nm-4nm-3nm-and-beyond

Planar Process Progression



Example Process Technologies

- **Sky130:** Skywater 130-nm process
  - Process design kit (PDK) available here: github.com/google/skywater-pdk
  - Open-source access and free chip fabrication for universities (partnership between Skywater, Google, and Efabless)
- **Sky90:** Skywater 90-nm process
  - Process design kit (PDK) no longer available publicly
- **TSMC28:** Taiwan Semiconductor Manufacturing Company 28-nm process

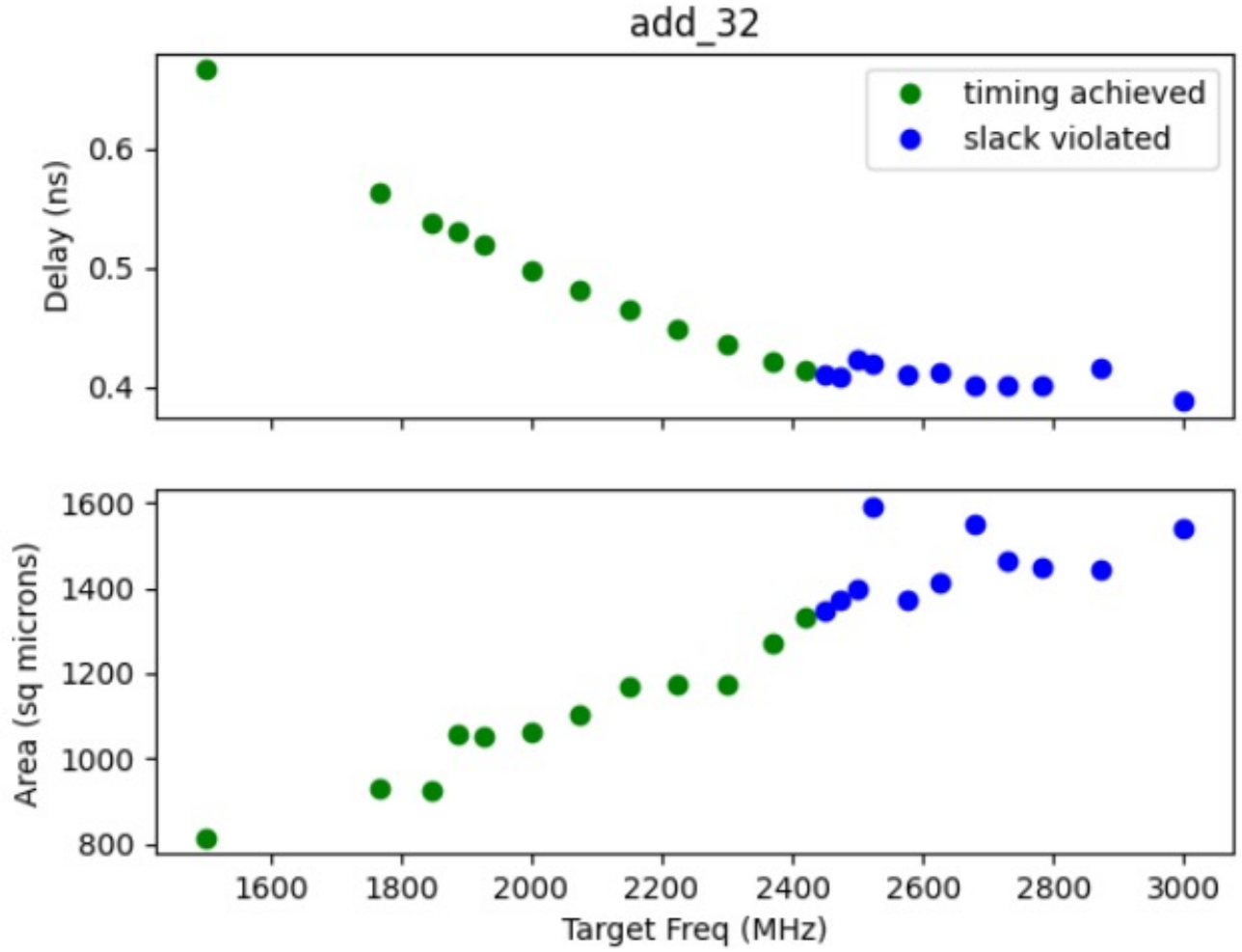
Inverter Characteristics

Fanout-of-4 inverter delay is the time for one inverter to drive four identical inverters. Representative of a typical gate delay.

Characteristic	Units	Skywater130	Skywater90	TSCM28hpc+
Nominal Supply Voltage	V	1.8	1.2	0.9
Track Pitch	mm	0.37	0.35	0.090
Cell Height	tracks	12	8	9
INVX1 FO4 Delay	ps	99.5	43.3	11.6
INVX1 Area	mm^2	4.4	1.96	0.252
INVX1 Leakage	nW	0.13	2.0	1.1
INVX1 Input Capacitance	fF	2.8	3.49	0.54

Delay and Area Tradeoffs

Power and area tend to increase with performance

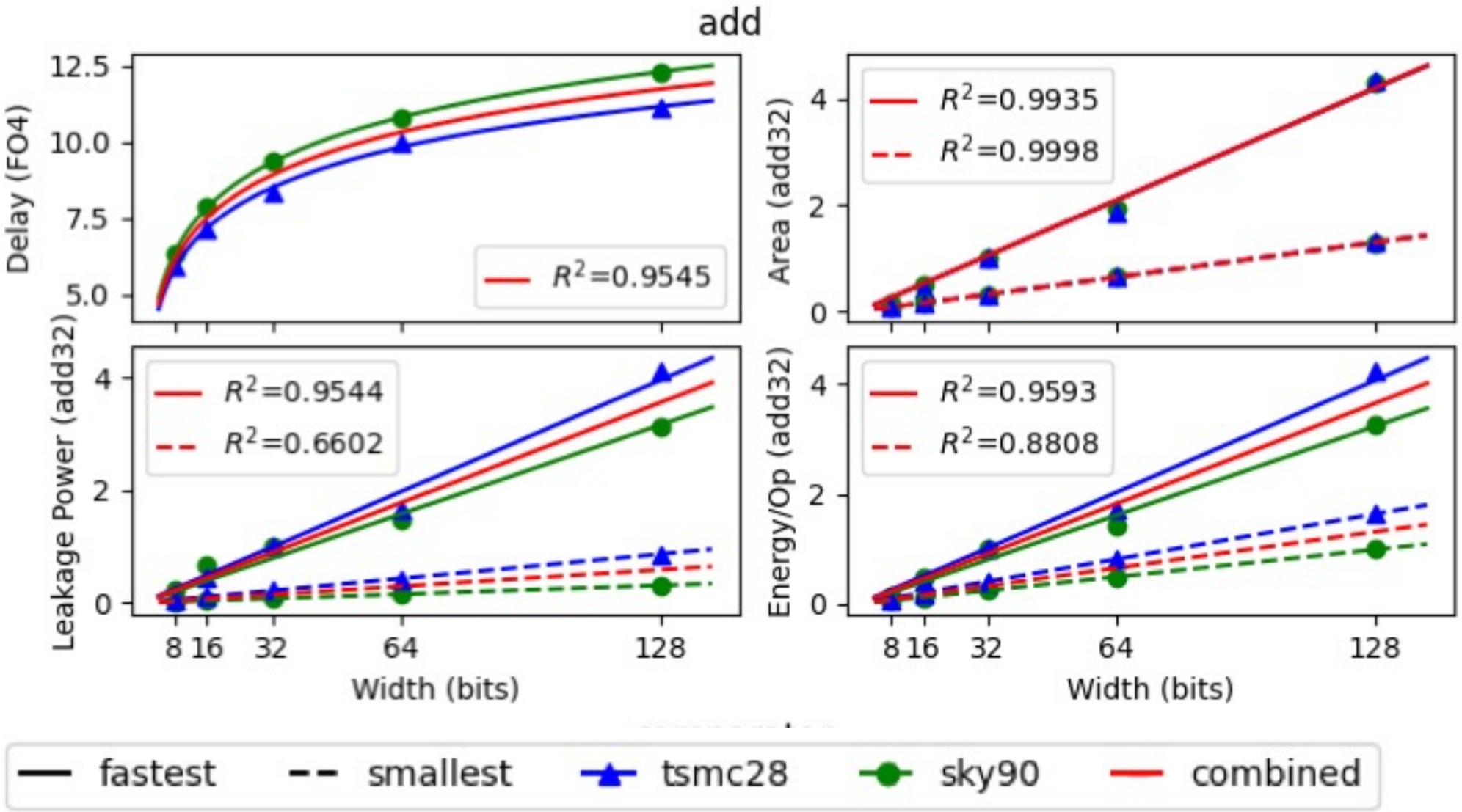


Skywater 90

Fast Adders

Characteristic	Units	Sky130	Sky90	TSCM28hpc+
Delay	ps	891	449	100
	FO4	9.0	10.4	8.6
Area	μm^2	2,581	1,441	209
Leakage Power	nW	18	714	1,060
Dynamic Energy	fJ / op	685	658	82

Datapath PPA Example: Adder



Datapath PPA

Element	Best Delay (FO4)	At Best Delay Relative to Fast add32			At Lowest Area Relative to Fast add32		
		Area	Leakage	Energy	Area	Leakage	Energy
add	1.9 + 1.4 $\log_2 N$	1.0S	0.89S	0.91S	0.32S	0.15S	0.33S
comparator	2.1 + 0.91 $\log_2 N$	0.58S	0.44S	0.27S	0.33S	0.15S	0.12S
priorityencoder	0.0 + 0.98 $\log_2 N$	0.32S	0.22S	0.087S	0.14S	0.044S	0.033S
shiftleft	0.46 + 1.60 $\log_2 N$	1.9S	2.1S	1.4S	0.77S	0.28S	0.48S
mult	0.0 + 6.0 $\log_2 N$	$13S^2$	$13S^2$	$33S^2$	$7.8S^2$	$3.5S^2$	$14S^2$
mux2	2.6 + 0.41 $\log_2 N$	0.21S	0.23S	0.16S	0.14S	0.11S	0.14S
mux4	3.1 + 0.50 $\log_2 N$	0.35S	0.31S	0.26S	0.27S	0.11S	0.19S
mux8	4.9 + 0.46 $\log_2 N$	0.80S	0.66S	0.43S	0.53S	0.23S	0.24S
csa	3.6	0.87S	1.3S	0.95S	0.33S	0.15S	0.31S
flop	3.3	0.33S	0.33S	1.3S	0.33S	0.33S	1.3S

Normalized to 32-bit adders

$S = N / 32$

Chapter 6: Logic Synthesis

Wally Synthesis Results

Output Files

- **DESIGN.sdc:** Synopsys Design Constraints file: provides constraints, including target clock period, driver and load cells, delays from primary inputs and outputs, and maximum fanout
- **DESIGN.sdf:** Standard Delay Format file; design timing for timing further analysis using Synopsys tools
- **DESIGN.ddc:** an encrypted binary database file; contains the synthesis results that Synopsys tools load for further analysis
- **DESIGN.sv:** synthesized Verilog netlist

Quality of Results (QOR) Files

Example: qor.rep for Wally rv32e in Skywater 130 nm

Timing Path Group 'clk'

Levels of Logic:	37.000000
Critical Path Length:	**3.030967**
Critical Path Slack:	**-0.152755**
Critical Path Clk Period:	3.030303
Total Negative Slack:	-57.774506
No. of Violating Paths:	710.000000
Worst Hold Violation:	0.000000
Total Hold Violation:	0.000000
No. of Hold Violations:	0.000000

Cell Count

Hierarchical Cell Count:	78
Hierarchical Port Count:	6697
Leaf Cell Count:	8226
Buf/Inv Cell Count:	2069
Buf Cell Count:	335
Inv Cell Count:	1734
CT Buf/Inv Cell Count:	0
Combinational Cell Count:	7053
Sequential Cell Count:	1173
Macro Count:	0

Quality of Results (QOR) Files, cont'd

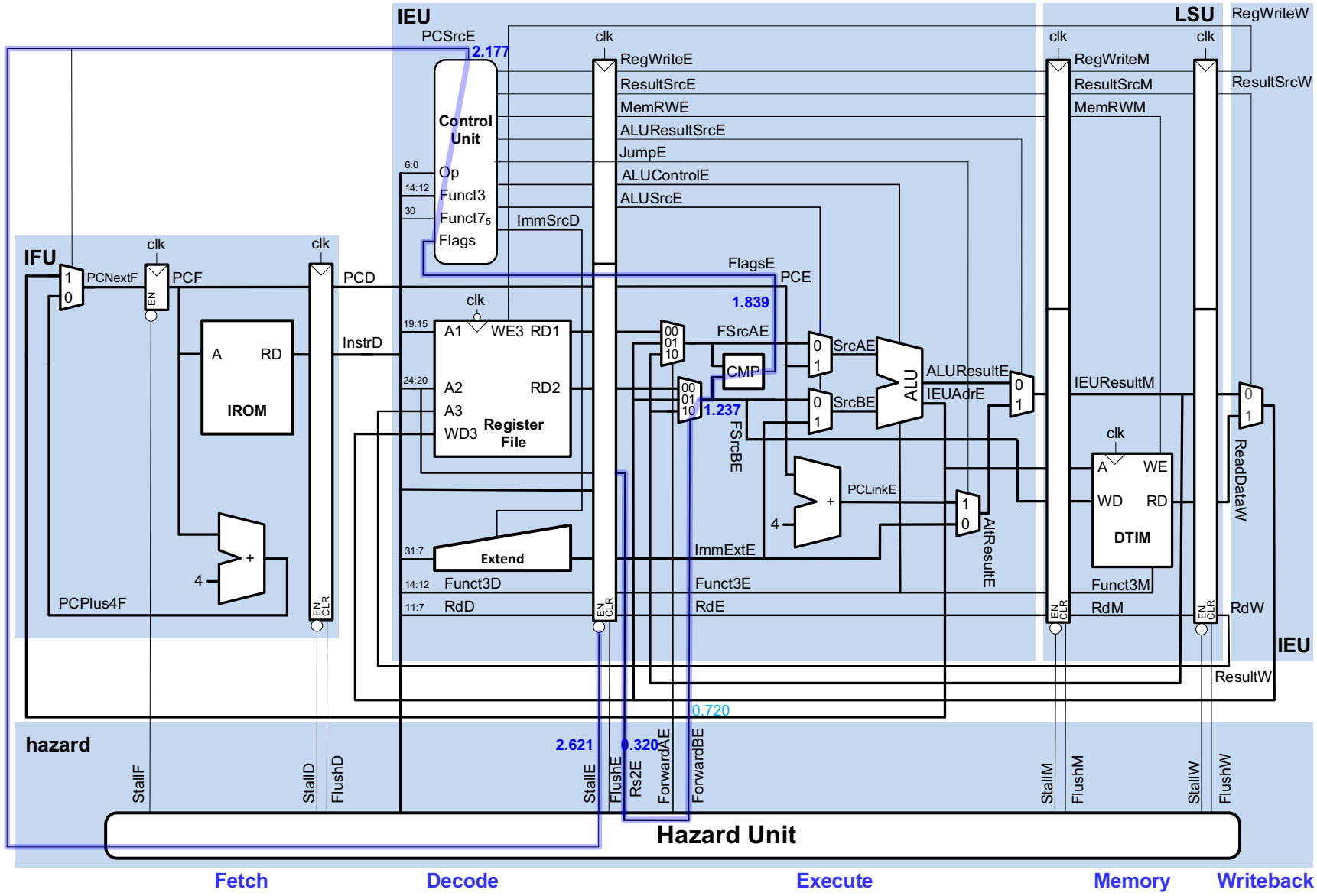
Example: qor.rep for Wally rv32e in Skywater 130 nm

```
Area
  ---------------------------------
  Combinational Area:      52579.678278
  Noncombinational Area:   42734.023876
  Buf/Inv Area:            10614.396889
  Total Buffer Area:       2400.485956
  Total Inverter Area:     8213.910933
  Macro/Black Box Area:    0.000000
  Net Area:                0.000000
  ---------------------------------

  Cell Area:               95313.702154
  Design Area:             95313.702154
  Design Rules
  ---------------------------------
  Total Number of Nets:    8614
  Nets With Violations:    0
  Max Trans Violations:    0
  Max Cap Violations:      0
  ---------------------------------

  ----------------------------------------------------------------
  Design  WNS: 0.152755  TNS: 57.774506  Number of Violating Paths: 710
  Design (Hold)  WNS: 0.000000  TNS: 0.000000  Number of Violating Paths: 0
  ----------------------------------------------------------------
```

Performance (Timing) Reports

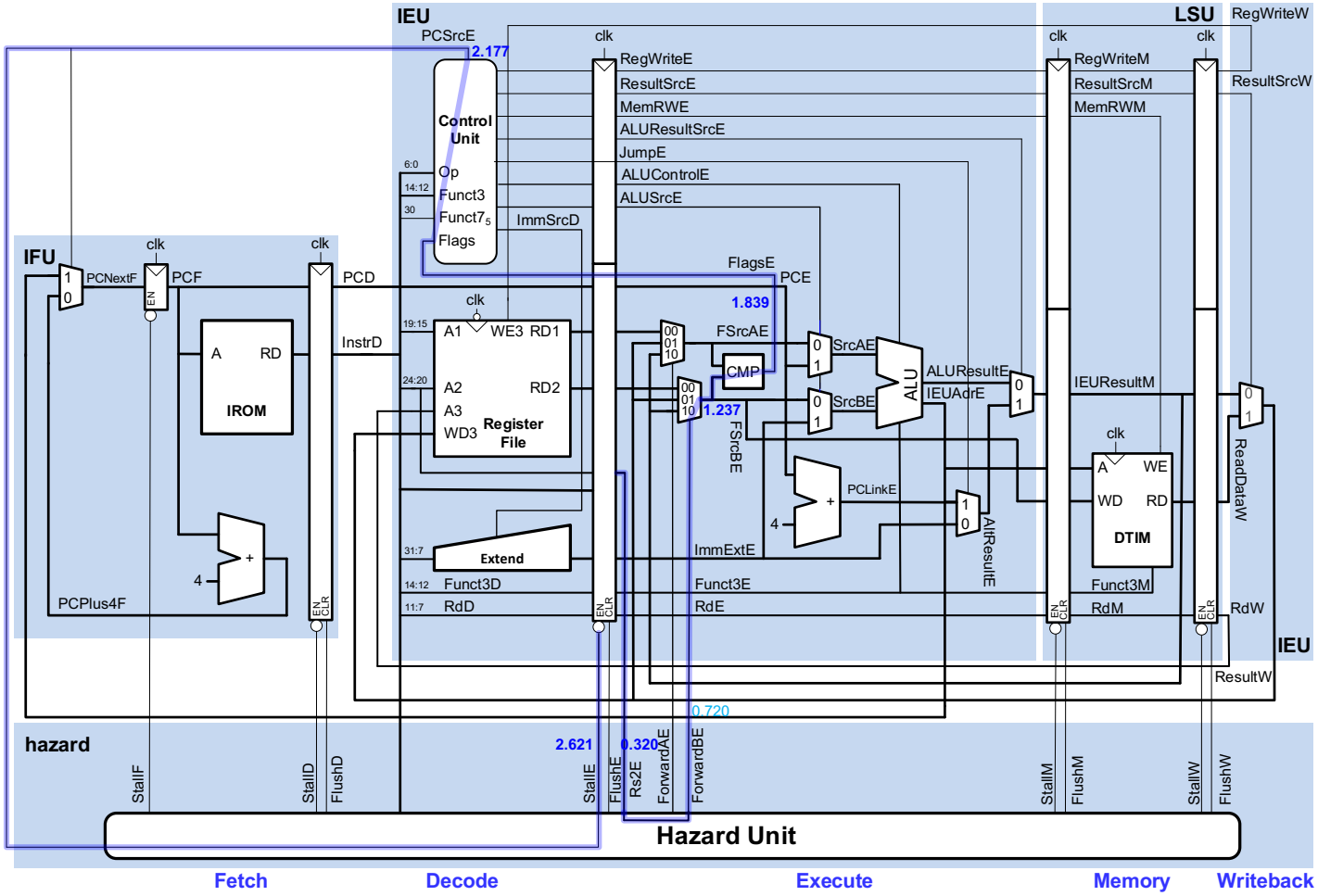
- **timing.rep:** Worst case overall timing
- **per_module_timing.rep:** Worst case timing through modules

Wally Critical Path



Wally Critical Path

- RS2E
- Comparator
- Flags
- StallE
- Pipeline register enable



Wally Timing Report: timing.rep

```
Point                                                Fanout       Cap      Trans      Incr       Path
-------------------------------------------------------------------------------------------------------
clock clk (rise edge)                                                                0.000000   0.000000
clock network delay (ideal)                                                          0.000000   0.000000
ieu/dp/Rs2EReg/q_reg[0]/CK (sky130_osu_sc_12T_ms__dff_1)                0.000000     0.000000 # 0.000000 r
ieu/dp/Rs2EReg/q_reg[0]/Q (sky130_osu_sc_12T_ms__dff_1)                 0.080838     0.320341   0.320341 f
ieu/dp/Rs2EReg/q[0] (net)                            4     0.013949              0.000000   0.320341 f
ieu/dp/Rs2EReg/q[0] (flopenrc_WIDTH5_3)                                              0.000000   0.320341 f
ieu/dp/Rs2E[0] (net)                                       0.013949              0.000000   0.320341 f
ieu/dp/Rs2E[0] (datapath__395949)                                                    0.000000   0.320341 f
ieu/Rs2E[0] (net)                                          0.013949              0.000000   0.320341 f
ieu/fw/Rs2E[0] (forward)                                                             0.000000   0.320341 f
ieu/fw/Rs2E[0] (net)                                       0.013949              0.000000   0.320341 f
ieu/fw/U36/Y (sky130_osu_sc_12T_ms__xnor2_l)                            0.089581     0.111006   0.431348 r
ieu/fw/n19 (net)                                     1     0.002578              0.000000   0.431348 r
ieu/fw/U35/Y (sky130_osu_sc_12T_ms__nand2_1)                            0.056313     0.070386   0.501734 f
ieu/fw/n54 (net)                                     2     0.004396              0.000000   0.501734 f
ieu/fw/U34/Y (sky130_osu_sc_12T_ms__inv_1)                              0.038368     0.051942   0.553675 r
ieu/fw/n21 (net)                                     1     0.002665              0.000000   0.553675 r
ieu/fw/U10/Y (sky130_osu_sc_12T_ms__nand2_1)                            0.035893     0.048400   0.602075 f
ieu/fw/n4 (net)                                      1     0.002499              0.000000   0.602075 f
ieu/fw/U9/Y (sky130_osu_sc_12T_ms__nor2_1)                              0.119280     0.118555   0.720630 r
ieu/fw/ForwardBE[1] (net)                            2     0.005788              0.000000   0.720630 r
ieu/fw/ForwardBE[1] (forward)                                                        0.000000   0.720630 r
ieu/ForwardBE[1] (net)                                     0.005788              0.000000   0.720630 r
ieu/dp/ForwardBE[1] (datapath__395949)                                               0.000000   0.720630 r
ieu/dp/ForwardBE[1] (net)                                  0.005788              0.000000   0.720630 r
```

Wally Timing Report: timing.rep, contd

```
 Point                                              Fanout       Cap     Trans      Incr       Path
 ------------------------------------------------------------------------------------------------------
ieu/dp/fbemux/s[1] (mux3_WIDTH32_0)                                                0.000000   0.720630 r
  ieu/dp/fbemux/s[1] (net)                                    0.005788                0.000000   0.720630 r
  ieu/dp/fbemux/U64/Y (sky130_osu_sc_12T_ms__buf_2)                       0.043860  0.113264   0.833893 r
  ieu/dp/fbemux/n27 (net)                                2    0.007730                0.000000   0.833893 r
  ieu/dp/fbemux/U21/Y (sky130_osu_sc_12T_ms__inv_2)                       0.020679  0.033514   0.867408 f
  ieu/dp/fbemux/n6 (net)                                 2    0.004983                0.000000   0.867408 f
  ieu/dp/fbemux/U6/Y (sky130_osu_sc_12T_ms__nand2_1)                      0.091524  0.079013   0.946421 r
  ieu/dp/fbemux/n7 (net)                                 1    0.009288                0.000000   0.946421 r
  ieu/dp/fbemux/U2/Y (sky130_osu_sc_12T_ms__inv_4)                        0.065229  0.081017   1.027438 f
  ieu/dp/fbemux/n86 (net)                               15    0.038532                0.000000   1.027438 f
  ieu/dp/fbemux/U23/Y (sky130_osu_sc_12T_ms__aoi22_l)                     0.111244  0.101017   1.128455 r
  ieu/dp/fbemux/n85 (net)                                1    0.002578                0.000000   1.128455 r
  ieu/dp/fbemux/U121/Y (sky130_osu_sc_12T_ms__nand2_1)                    0.096501  0.108888   1.237343 f
  ieu/dp/fbemux/y[26] (net)                              3    0.009574                0.000000   1.237343 f
  ieu/dp/fbemux/y[26] (mux3_WIDTH32_0)                                               0.000000   1.237343 f
  ieu/dp/n126 (net)                                           0.009574                0.000000   1.237343 f
  ieu/dp/comp/b[26] (comparator_WIDTH32)                                             0.000000   1.237343 f
  ieu/dp/comp/b[26] (net)                                     0.009574                0.000000   1.237343 f
  ieu/dp/comp/U95/Y (sky130_osu_sc_12T_ms__inv_2)                         0.042916  0.061810   1.299153 r
  ieu/dp/comp/n160 (net)                                 2    0.005376                0.000000   1.299153 r
  ieu/dp/comp/U92/Y (sky130_osu_sc_12T_ms__aoi22_l)                       0.065065  0.048621   1.347774 f
  ieu/dp/comp/n29 (net)                                  1    0.002488                0.000000   1.347774 f
  ieu/dp/comp/U43/Y (sky130_osu_sc_12T_ms__nand2_1)                       0.064032  0.074407   1.422181 r
  ieu/dp/comp/n183 (net)                                 2    0.005462                0.000000   1.422181 r
  ieu/dp/comp/U240/Y (sky130_osu_sc_12T_ms__inv_1)                        0.026098  0.038457   1.460638 f
  ieu/dp/comp/n159 (net)                                 1    0.002488                0.000000   1.460638 f
```

Wally Timing Report: timing.rep, contd

```
Point                                                  Fanout       Cap      Trans      Incr       Path
-------------------------------------------------------------------------------------------------------
...
hzu/U13/Y (sky130_osu_sc_12T_ms__buf_2)                                    0.054383   0.144729   2.621394 f
hzu/StallE (net)                                          4      0.016288             0.000000   2.621394 f
hzu/StallE (hazard__395949) <-                                                        0.000000   2.621394 f
StallE (net)                                                     0.016288             0.000000   2.621394 f
ifu/StallE (ifu__395949)                                                              0.000000   2.621394 f
ifu/StallE (net)                                                 0.016288             0.000000   2.621394 f
ifu/U6/Y (sky130_osu_sc_12T_ms__inv_2)                                     0.073454   0.077434   2.698829 r
ifu/n256 (net)                                            6      0.015610             0.000000   2.698829 r
ifu/InstrEReg/en (flopenr_WIDTH32_1)                                                  0.000000   2.698829 r
ifu/InstrEReg/en (net)                                           0.015610             0.000000   2.698829 r
...
ifu/InstrEReg/q_reg[31]/D (sky130_osu_sc_12T_ms__dff_1)                    0.120045   0.000000   3.055580 r
data arrival time                                                                                 3.055580

clock clk (rise edge)                                                                 3.030303   3.030303
clock network delay (ideal)                                                           0.000000   3.030303
ifu/InstrEReg/q_reg[31]/CK (sky130_osu_sc_12T_ms__dff_1)                              0.000000   3.030303 r
library setup time                                                                   -0.152149   2.878155
data required time                                                                                2.878155
-------------------------------------------------------------------------------------------------------
data required time                                                                                2.878155
data arrival time                                                                                -3.055580
-------------------------------------------------------------------------------------------------------
slack (VIOLATED)                                                                                 -0.177425
```

Wally Critical Path

```
Point                                                Fanout       Cap      Trans      Incr       Path
-------------------------------------------------------------------------------------------------------
...
hzu/U13/Y (sky130_osu_sc_12T_ms__buf_2)                                   0.054383   0.144729   2.621394 f
hzu/StallE (net)                                        4     0.016288              0.000000   2.621394 f
hzu/StallE (hazard__395949) <-                                                    0.000000   2.621394 f
StallE (net)                                                  0.016288            0.000000   2.621394 f
ifu/StallE (ifu__395949)                                                          0.000000   2.621394 f
ifu/StallE (net)                                              0.016288            0.000000   2.621394 f
ifu/U6/Y (sky130_osu_sc_12T_ms__inv_2)                                    0.073454   0.077434   2.698829 r
ifu/n256 (net)                                          6     0.015610            0.000000   2.698829 r
ifu/InstrEReg/en (flopenr_WIDTH32_1)                                              0.000000   2.698829 r
ifu/InstrEReg/en (net)                                        0.015610            0.000000   2.698829 r
...
ifu/InstrEReg/q_reg[31]/D (sky130_osu_sc_12T_ms__dff_1)                   0.120045   0.000000   3.055580 r
data arrival time                                                                             3.055580

clock clk (rise edge)                                                             3.030303   3.030303
clock network delay (ideal)                                                       0.000000   3.030303
ifu/InstrEReg/q_reg[31]/CK (sky130_osu_sc_12T_ms__dff_1)                          0.000000   3.030303 r
library setup time                                                               -0.152149   2.878155
data required time                                                                            2.878155
-------------------------------------------------------------------------------------------------------
data required time                                                                            2.878155
data arrival time                                                                            -3.055580
-------------------------------------------------------------------------------------------------------
slack (VIOLATED)                                                                             -0.177425
```

Power Reports

- **power.rep:** shows power in each module
- **Example:** Using Sky130

```
Global Operating Voltage = 1.8
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW
-------------------------------------------------------------------------------
                                        Switch   Int      Leak     Total
Hierarchy                               Power    Power    Power    Power    %
-------------------------------------------------------------------------------
wallypipelinedcore__395949                 0.820    5.302  715.939    6.122 100.0
  hzu (hazard__395949)                  7.04e-03 1.90e-03    1.674 8.95e-03   0.1
  ebu.ebu (ebu_XLEN32_PA_BITS34_AHBW32)
                                        3.79e-02    0.177   10.097    0.215   3.5
  lsu (lsu__395949)                     5.16e-02    0.609   32.021    0.661  10.8
  ieu (ieu__395949)                        0.458    3.299  602.129    3.758  61.4
  ifu (ifu__395949)                        0.264    1.213   69.435    1.477  24.1
```

Leakage power = **715 nW**. **Dynamic power** = (5.302 + 0.820) = **6.122** mW. Dynamic power dominates when it is operating – but leakage power affects battery life when quiescent.

Area Reports

- **area.rep:** shows area of each module
- **Example:** Using Sky130

```
Number of ports:                         6891
Number of nets:                         13479
Number of cells:                         8265
Number of combinational cells:           7014
Number of sequential cells:              1173
Number of macros/black boxes:               0
Number of buf/inv:                       2060
Number of references:                      11

Combinational area:              52330.105886
Buf/Inv area:                    10525.996487
Noncombinational area:           42734.023876
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 95064.129763
```

Total area:

95,064 µm²

(~0.1 mm²)

Chapter 6: Logic Synthesis

Wally Configurations

Wally Derived Configs. for Synth.

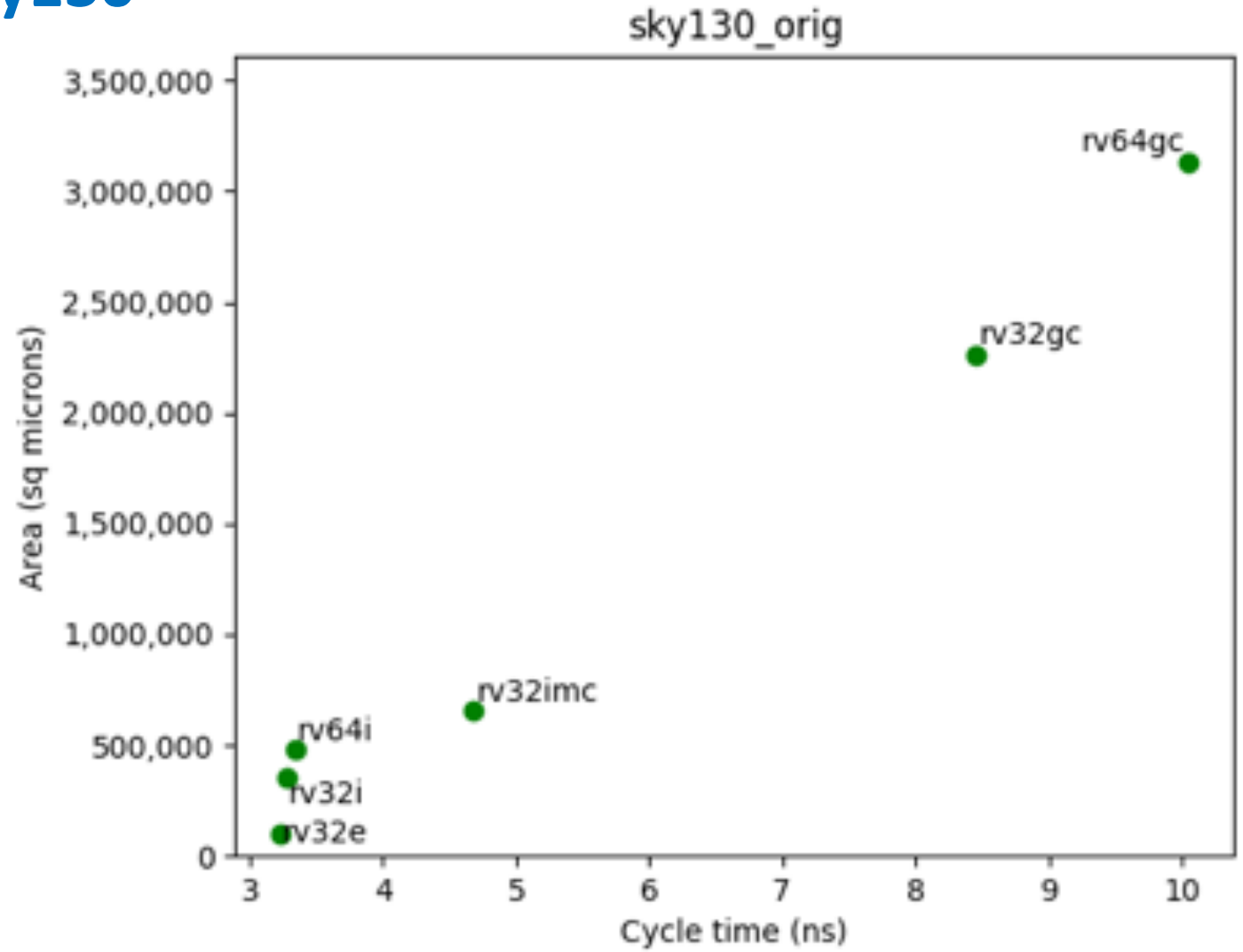
Derived Config	Base Config	Tweaks
syn_rv32e	rv32e	Reduced memory size to keep runtime and memory reasonable for processes without SRAM
syn_rv32i	rv32i	
syn_rv32imc	rv32imc	
syn_rv32gc	rv32gc	
syn_rv64i	rv64i	
syn_rv64gc	rv64gc	
syn_sram_rv32e	rv32e	Use SRAM library for TSMC28hpm
syn_sram_rv32i	rv32i	
syn_sram_rv32imc	rv32imc	
syn_sram_rv32gc	rv32gc	
syn_sram_rv64i	rv64i	
syn_sram_rv64gc	rv64gc	
syn_rv64gc_pmp0	rv64gc	Gradually disable features to explore critical paths
syn_rv64gc_noPriv	syn_rv64gc_pmp0	
syn_rv64gc_noFPU	syn_rv64gc_noPriv	
syn_rv64gc_noMulDiv	syn_rv64gc_noFPU	
syn_rv64gc_noAtomic	syn_rv64gc_noMulDiv	
syn_sram_rv64gc_pmp0	syn_sram_rv64gc	Gradually disable features to explore critical paths while using SRAM library
syn_ sram_rv64gc_noPriv	syn_sram_rv64gc_pmp0	
syn_ sram_rv64gc_noFPU	syn_ sram_rv64gc_noPriv	
syn_ sram_rv64gc_noMulDiv	syn_ sram_rv64gc_noFPU	
syn_ sram_rv64gc_noAtomic	syn_ sram_rv64gc_noMulDiv	

Area & Performance vs. Process

Config: rv64gc	Sky130	Sky90	TSMC28
Area (mm2)	3.2	1.3	0.5
Tc (ns)	10	4	1.3

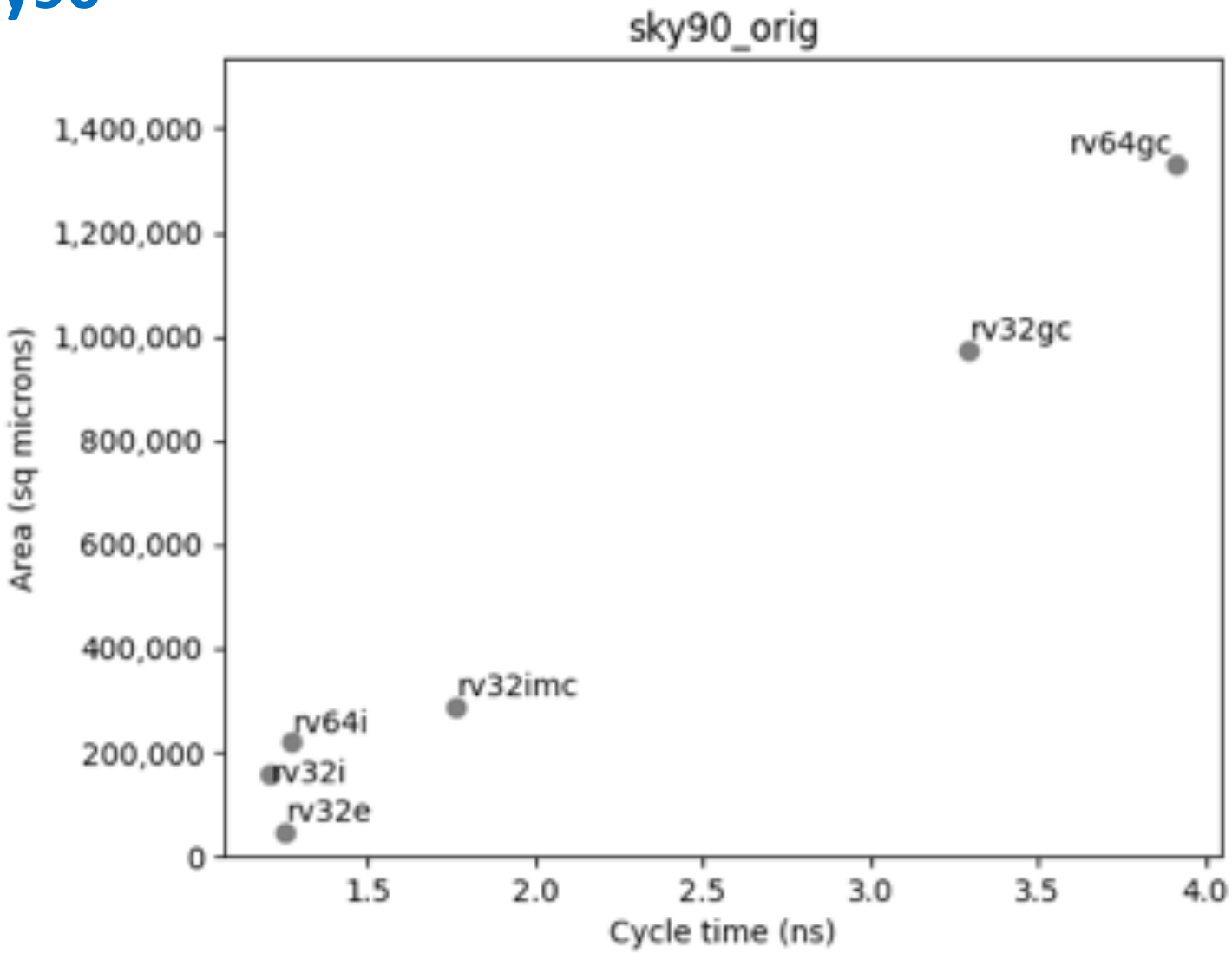
Area & Performance vs. Config.

Sky130



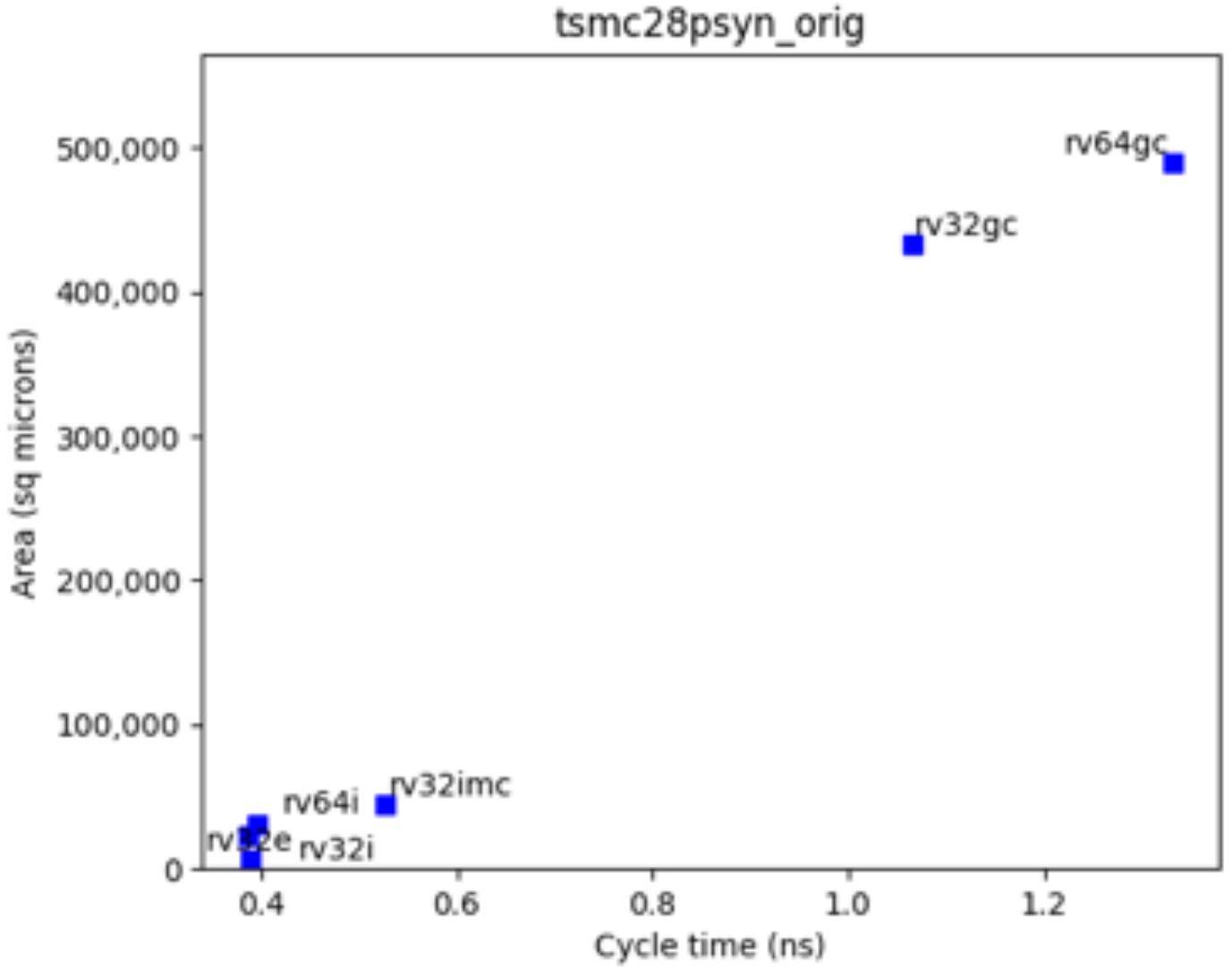
Area & Performance vs. Config.

Sky90



Area & Performance vs. Config.

TSMC28



Area & Performance vs. Features

Feature	PMP Entries	Privileged Unit	FPU	MDU	Atomic Ops
orig	16	Y	Y	Y	Y
PMP0	0	Y	Y	Y	Y
noPriv	0	N	Y	Y	Y
noFPU	0	N	N	Y	Y
noMulDiv	0	N	N	N	Y
noAtomic	0	N	N	N	N

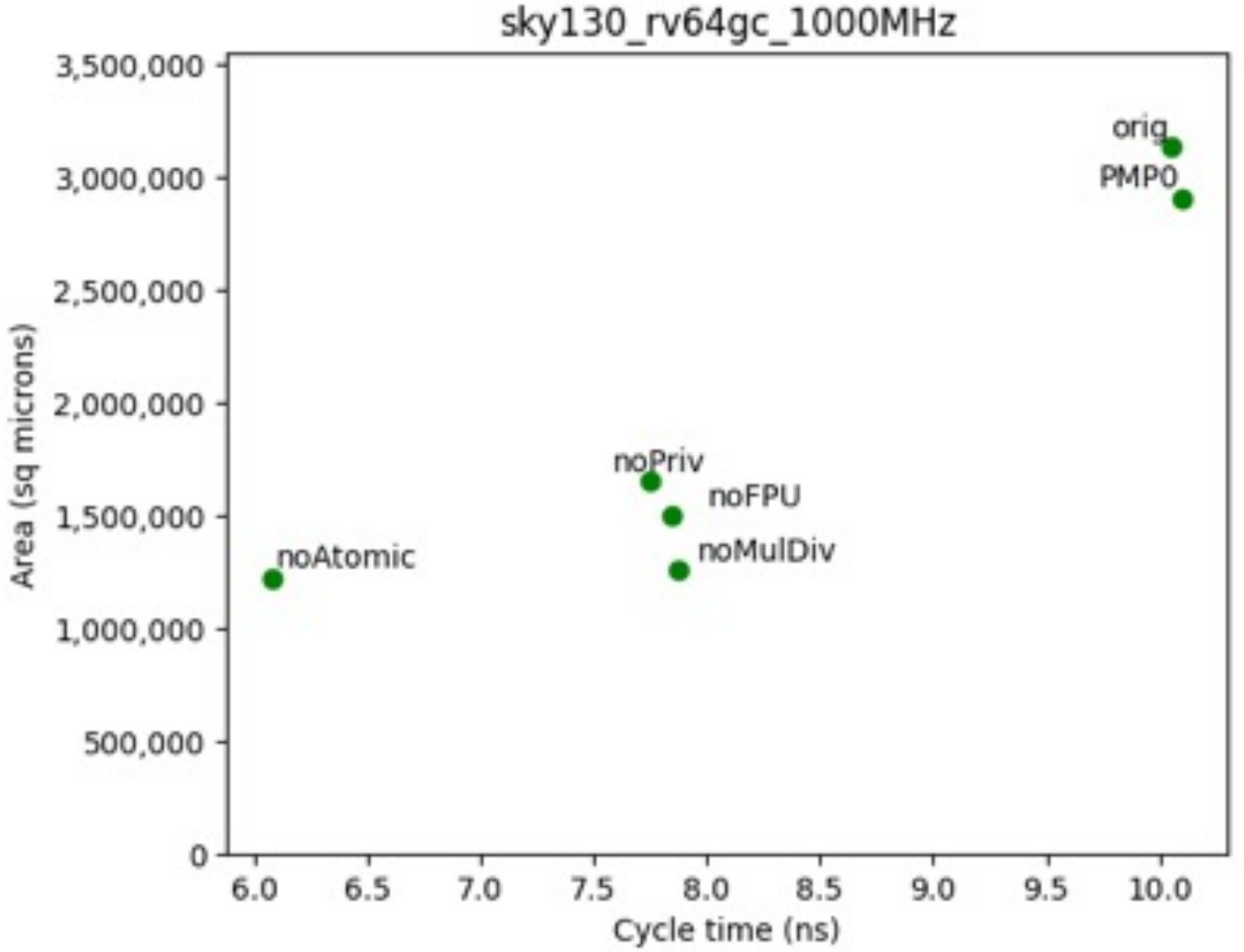
Area & Performance vs. Features

Feature	PMP Entries	Privileged Unit	FPU	MDU	Atomic Ops
orig	16	Y	Y	Y	Y
PMP0	0	Y	Y	Y	Y
noPriv	0	N	Y	Y	Y
noFPU	0	N	N	Y	Y
noMulDiv	0	N	N	N	Y
noAtomic	0	N	N	N	N

Little difference: orig vs. PMP0
Big difference: orig vs. noPriv/noFPU/noMulDiv
Biggest difference: orig vs. noAtomic

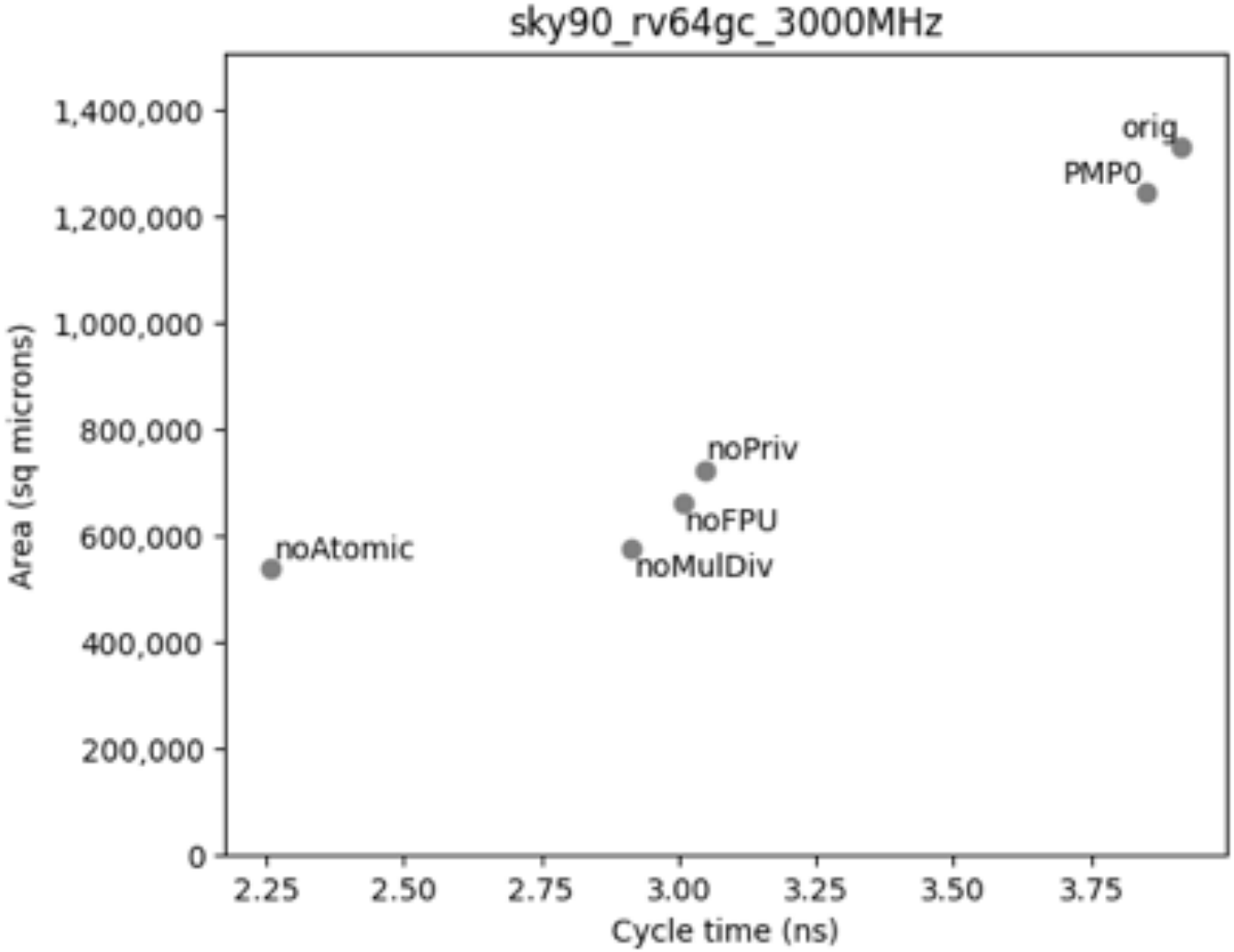
Area & Performance vs. Features

Sky130



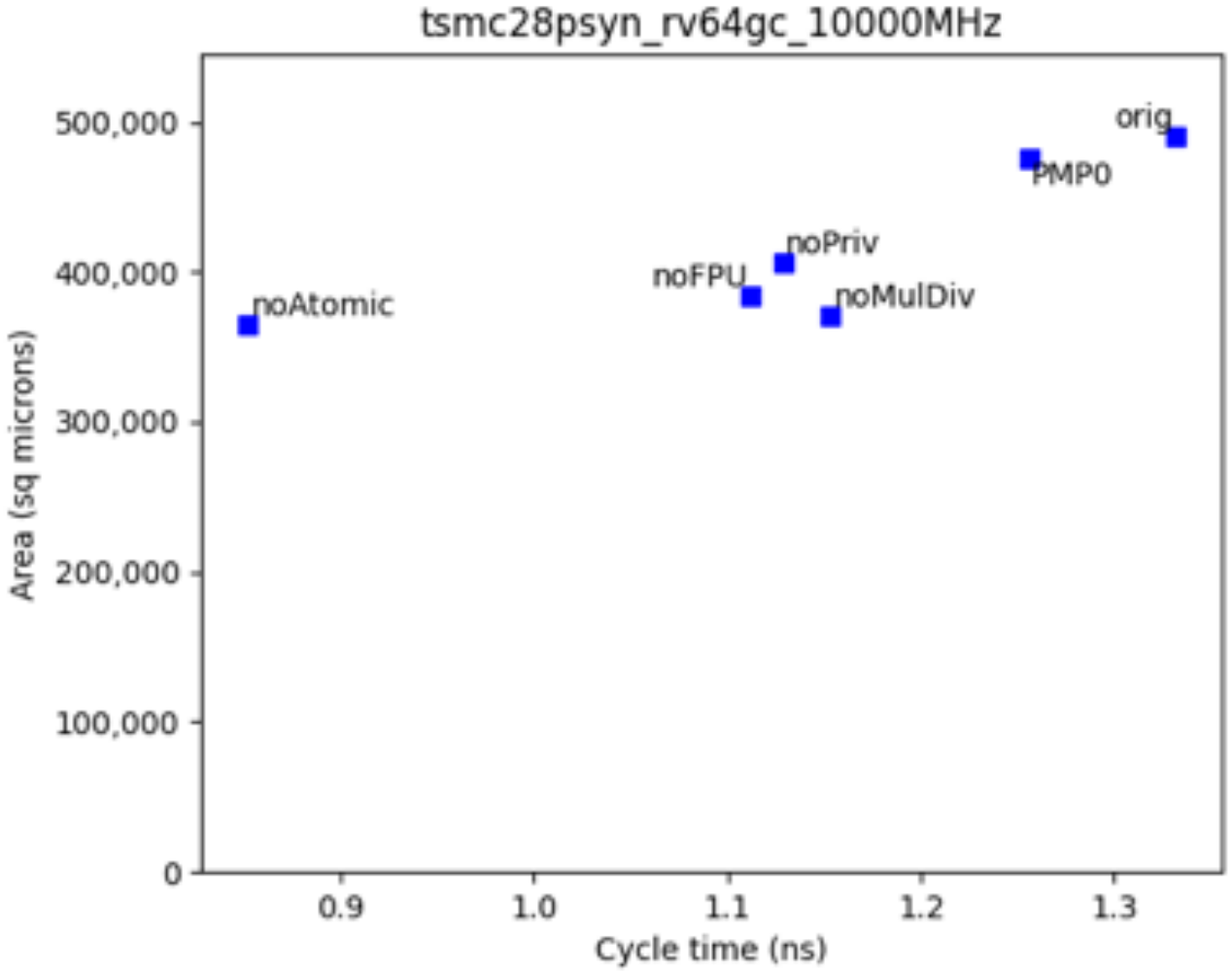
Area & Performance vs. Features

Sky90



Area & Performance vs. Features

TSMC28



About these Notes

RISC-V System-on-Chip Design Lecture Notes