RISC-V

System-on-Chip Design

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Chapter 1

A Brief History of Computer Design

RISC-V SoC Design Table of Contents

Intro & Tools	1-2.	Intro: Computer Design & RISC-V
		Appendix B. Hitchhikers Guide to Linux
		Appendix C. Git
	3.	Tool Flow
	4.	HDL Design Practices
	5-6.	Design Verification, Logic Synthesis
Wally RISC-V Processor	7.	Wally: RISC-V Pipelined Processor
	8.	Privileged Operations
	9.	Buses
	10.	Caches
	11.	Memory Management Unit (MMU)
	12.	Load/Store Unit (LSU)
	13.	Instruction Fetch Unit (IFU)
Extensions	14.	Compressed Extension
	15.	Multiply/Divide Extension
	16.	Floating-Point Extension
	17.	Atomic Extension
	18.	Bit manipulation & Cryptography Extension
	19.	Other Extensions

RISC-V SoC Design Table of Contents

Peripherals, Benchmarking, Linux & FPGA

20. Peripherals
21. Benchmarking
22. Linux
23. FPGA Implementation

Other Appendices

A. Wally Synopsis
C. Tcl
F. Floating-Point Implementation
I. Instruction Summary

Course & Textbook Overview

- System-on-Chip (SoC)
- RISC-V
- RISC-V SoC

Systems-on-Chip

- **System-on-Chip (SoC)**
  - Integrates microprocessors, memories, peripherals
  - More than 10 billion transistors/cm^2 in 2025
  - Transistors switch between 0 and 1 in picoseconds
  - Consume < 1 femtojoule each time
  - Modern integrated circuits are usually called SoCs
- **Applications**
  - Low-cost battery-powered mobile devices
  - Medical devices
  - Consumer gadgets
  - Education
  - Warfare
- **Central to prosperity and national security**

RISC-V

First major non-proprietary computer architecture

- 5th generation Reduced Instruction Set Computer (RISC)
- Developed at **Berkeley in 2010**
- **Simple instructions**
  - Avoids many "cute tricks" that proved overly clever in older architectures
- **No patents or licensing** agreements required
- Driven by non-profit **RISC-V International**

Huge momentum

- Likely to displace all architectures besides x86 and ARM
- **12 billion cores shipped by 2022**, with expected 40% annual compound growth through 2030

RISC-V SoC Design

This course will take you through building a **real full-featured SoC** containing a RISC-V processor, memories, and peripherals.

- Most architecture courses focus on high-level principles
- This course will show you both principles and detailed implementation

Wally configurable SoC

- 32 or 64 bit
- Bus, cache, memory management, branch prediction
- Floating-point unit
- Other standard extensions
- Peripherals
- Boots Linux on an FPGA

Chapter 1

A Brief History of Computer Design

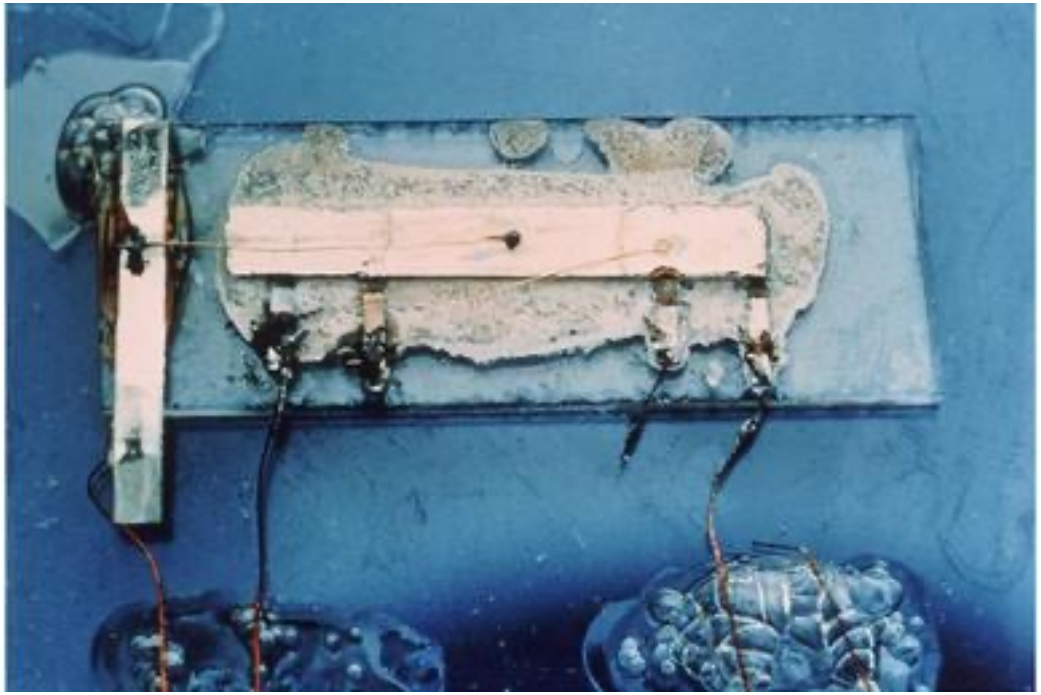
Chapter 1 :: Topics

A Brief History of Computer Design

1.1 Moore's Law & Beyond
1.2 System-on-Chip
1.3 Birth of Computing
1.4 Mainframes & Minicomputers
1.5 Microprocessors
1.6 CISC & RISC
1.7 RISC-V
1.8 International Economic & Security Competition

Integrated Circuits

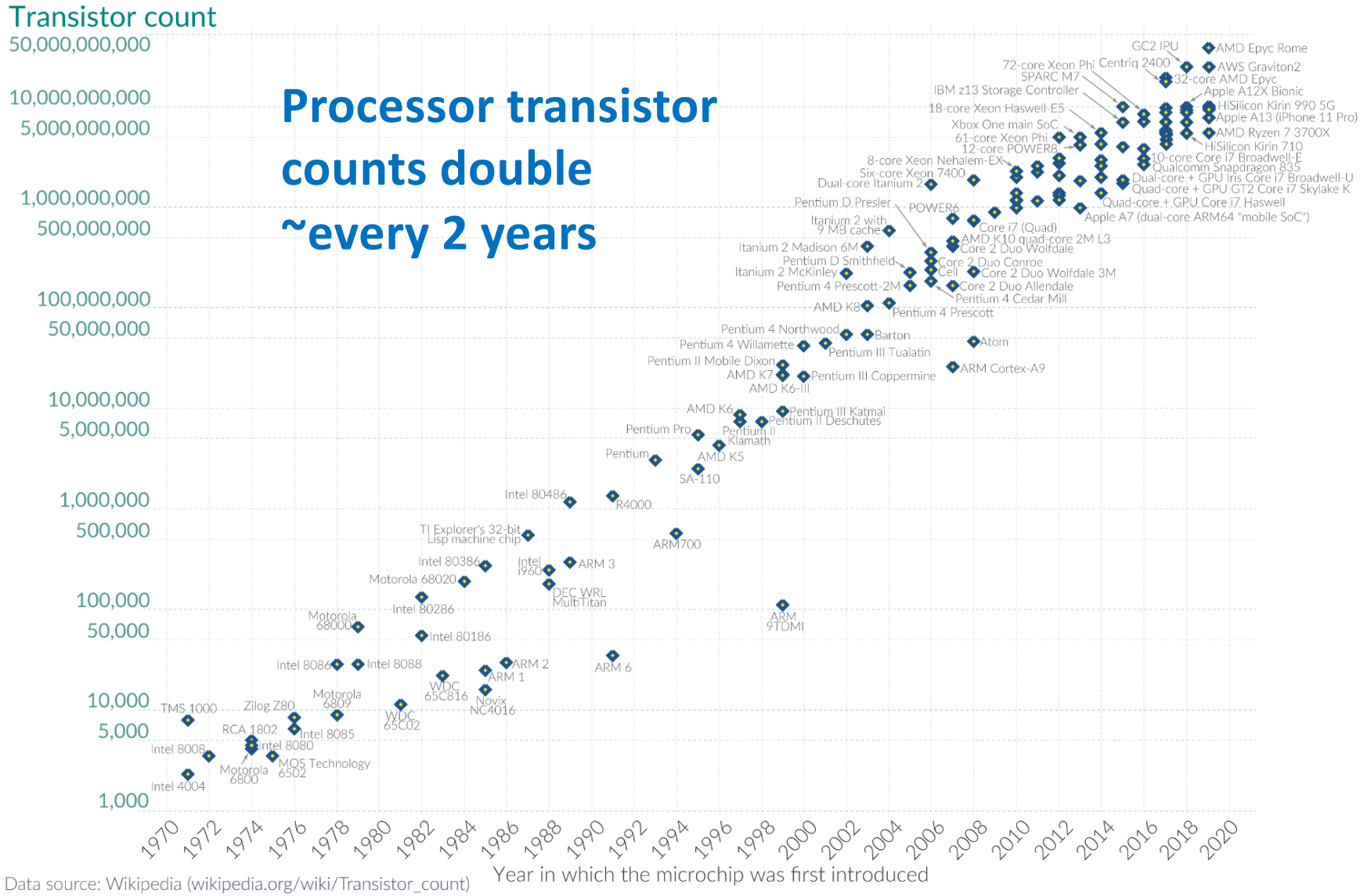
- Jack Kilby & Robert Noyce coinvented **first integrated circuit in 1958**.
- **Moore's Law:** Observation that the number of transistors on a chip grows exponentially.



First Integrated Circuit

https://en.wikipedia.org/wiki/Jack_Kilby

Moore's Law



Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)
OurWorldinData.org – Research and data to make progress against the world's largest problems.

Transistor/Chip Evolution

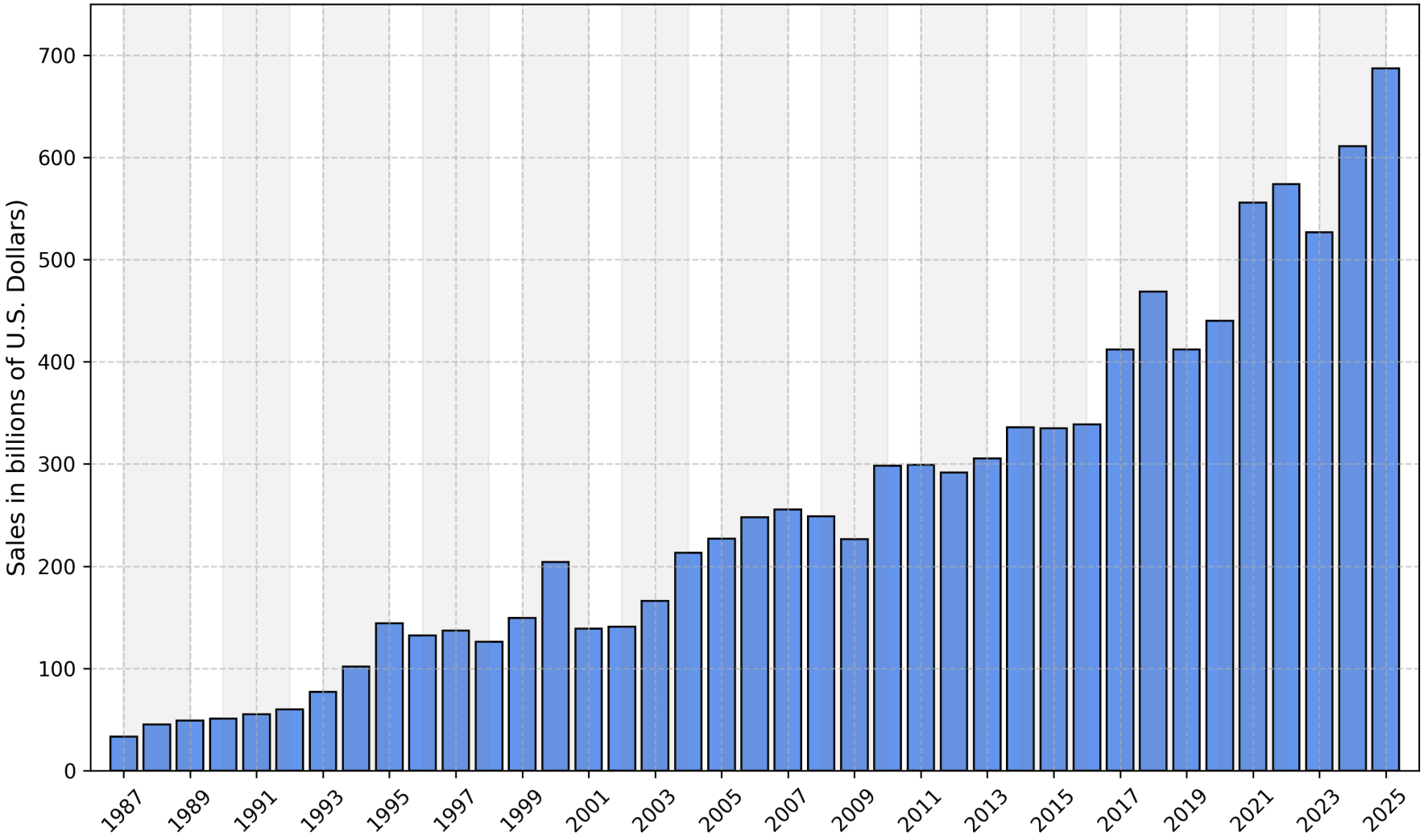
Process Node	16 nm	10 nm	7 nm	5 nm	3 nm
Initial production	2014	2016	2018	2020	2022
Chip area (mm^2)	125	88	83	85	85
Billions of transistors	3.3	4.3	6.9	10.5	14.1
Gross dice / wafer	478	686	721	707	707
Net dice / wafer	360	512	546	530	510
Wafer cost ($)	5912	8389	9965	12500	15500
Die cost ($)	16.43	16.37	18.26	23.57	30.45
Transistor cost (nanobucks)	4.98	3.81	2.65	2.25	2.16

Dennard's Law and Scaling

- **Dennard's Law:** Transistor speed and power consumption improve as transistors shrink.
- **Dennard Scaling:**
  - If new process node reduces these by 30%:
    - Transistor dimensions
    - Supply voltage
    - Threshold voltage
  - Then it results in:
    - 1.4x the speed
    - ½ the power per transistor

Dennard scaling tapered off around 2004. Now transistor power and performance gradually improve due to innovation (i.e., strained silicon, high-k metal gates, FinFETs, gate-all-around transistors, etc.)

Global Semiconductor Sales



http://www.statista.com/statistics/266973/global-semiconductor-sales-since-1988

Design Cost

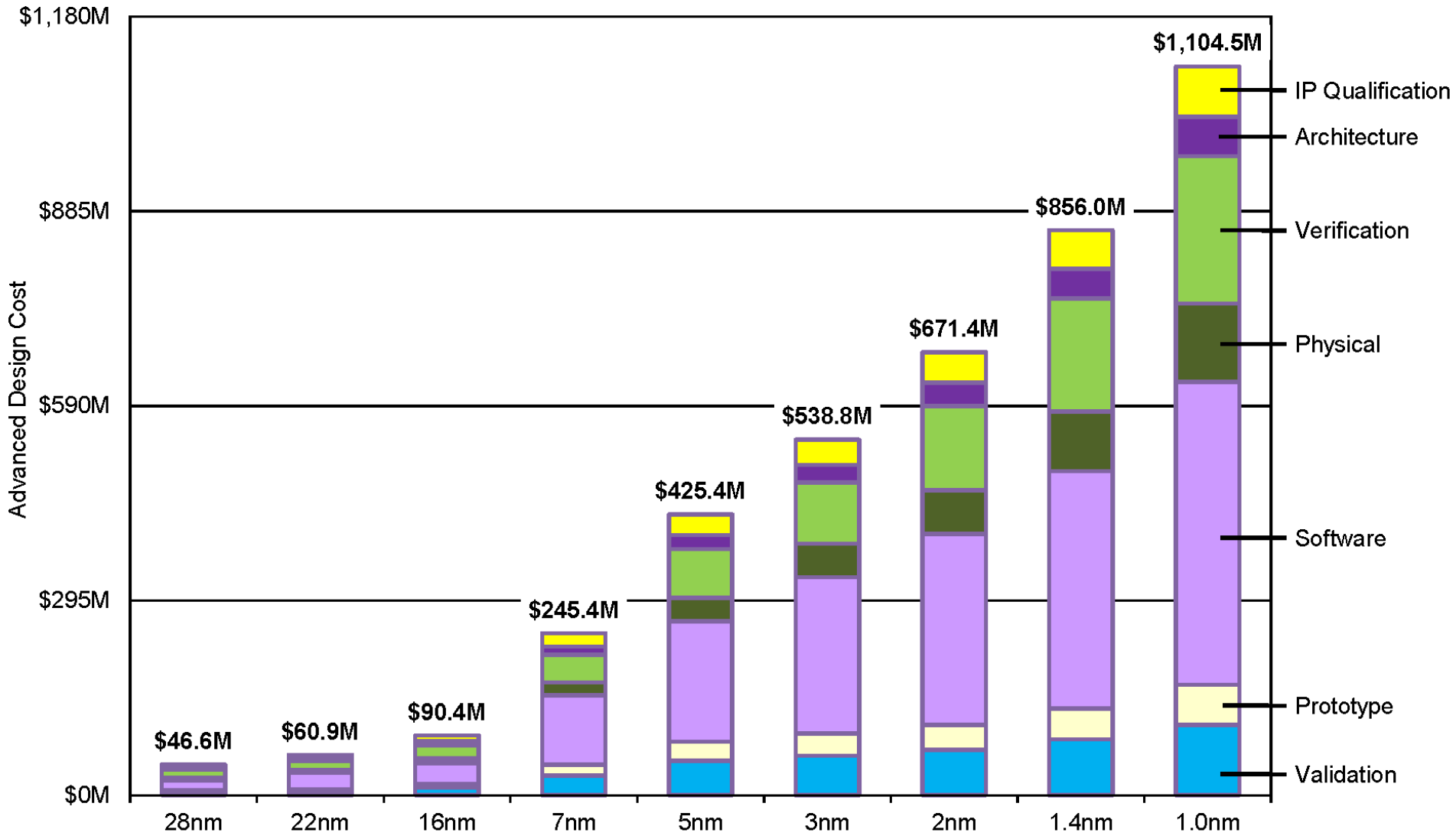


Image courtesy of International Business Strategies, Inc., September 2024.

Processor Timeline

1830-1871	**Analytical Engine**	First digital computer (*Charles Babbage*)
1941	**Z3**	First general-purpose computer (*Conrad Zuse*)
1942	**ABC**	First electronic computer (*Atanasoff, Berry*)
1943	**Colossus**	First programmable computer (*Bletchley Park*)
1944	**Mark I**	Separate program and data (*Harvard*)
1945	**ENIAC**	Digital electronic, gp & programmable (*U. Penn*)
1948	**Baby**	First to have a stored program (*Manchester U.*)
1951	**EDVAC**	Follow on to ENIAC, added a stored program (*U. Penn*)
1961	**Stretch**	First to use transistors (*Gene Amdahl*)
1960	**System/360**	First commercial success (*IBM*)

1969	**4004**	First 4-bit microprocessor, on a single chip (*Intel*)
1970	**PDP-11**	Leading minicomputer (*DEC*: *Digital Equip. Corp.*)
1977	**Apple II**	Low-cost 6502 makes computers widely available
1981	**IBM PC**	Competitor to Apple II, based on Intel's 8088
1982-1986	**RISC**	RISC-I (*Berkeley*), MIPS I (*Stanford*), ARM I, SPARC
1992	**Alpha 21064**	200 MHz RISC processor 3x speed of Pentium (*DEC*)
1993	**Pentium**	66 MHz CISC: RISC wins RISC vs. CISC debate (*Intel*)
1994-2006	**MHz Wars**	Super-pipelining, high power
2006	**Core**	Multi-core (*Intel*)
2010	**RISC-V**	First popular open-source architecture (*Berkeley*)

The Analytical Engine

- Designed by Charles Babbage from 1834-1871
- Considered to be the first digital computer
- Built from mechanical gears, where each gear represented a discrete value (0-9)
- Babbage died before finishing it

Image courtesy Wellcome Collection:
Stipple engraving by R. Roffe, 1833.

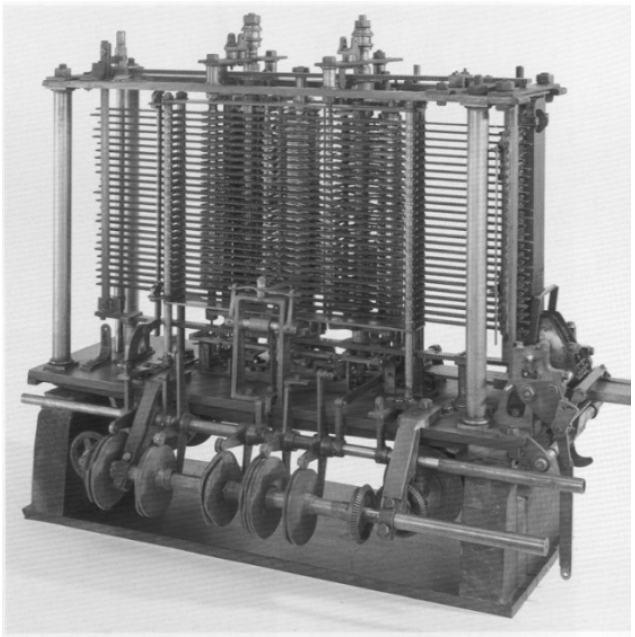


Image courtesy of Science Museum / Science and Society Picture Library.

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1940s

- Spurred on by need for computation in World War II
  - 1941: Z3 computer (Zuse, Berlin) – first general-purpose computer
  - 1942: ABC computer – first electronic computer
  - Etc.

Harvard Mark I

http://www.cs.kent.edu/~rothstei/10051/HistoryPt3.htm

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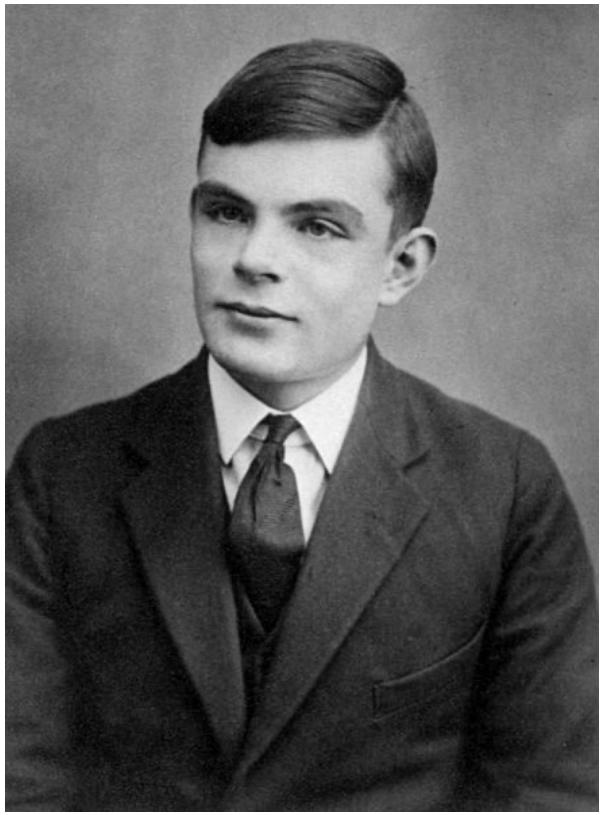
John Von Neumann, 1903-1957

- By age 8, was learning calculus and spoke six languages
- Faculty member at Princeton
- One of founding figures of computer architecture
- Published idea of a stored program architecture
- His other contributions include:
  - Establishing mathematical framework for quantum mechanics
  - Founding the field of game theory

Alan Turing, 1912 - 1954

- British mathematician and computer scientist
- Founder of computer science and AI
- Developed the Turing machine: a universal computing machine capable of carrying out any algorithm
- Published seminal proof that not all problems are computable
- In 1952, was prosecuted for homosexual acts. Two years later, he died of cyanide poisoning.
- The Turing Award was named in his honor, which is the highest honor in computing.



https://commons.wikimedia.org/wiki/File:Alan_Turing_Aged_16.jpg

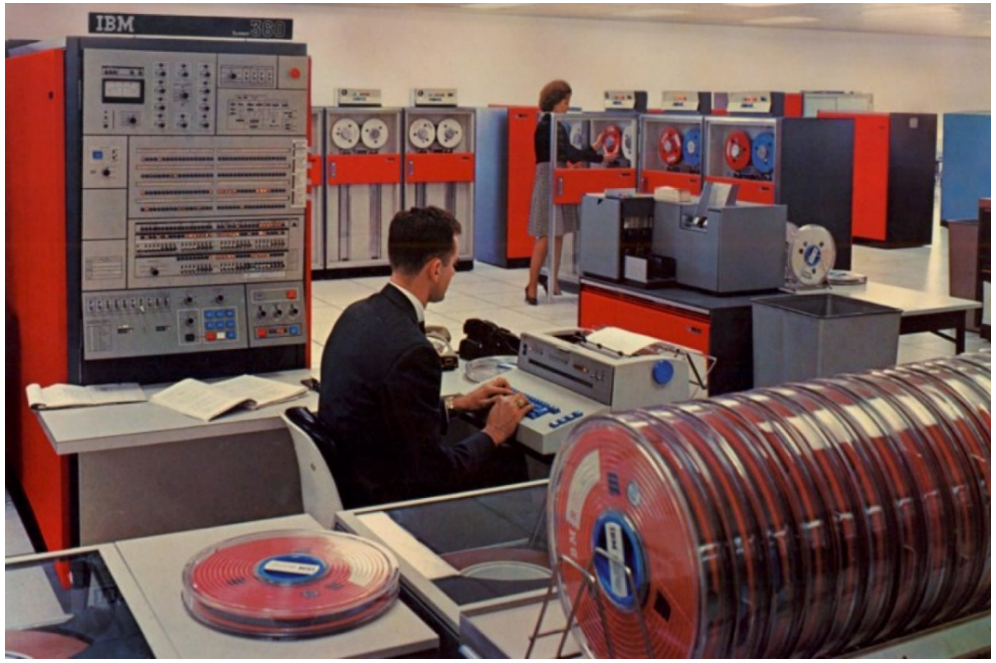
Grace Hopper, 1906 - 1992

- Graduated from Yale University with a Ph.D. in mathematics
- Programmed Mark I computer
- Helped develop the COBOL programming language & compiler
- Highly awarded naval officer
- Received World War II Victory Medal and National Defense Service Medal, among others

Image courtesy United States Navy DN-SC-84-05971.

IBM's System 360

- First commercial success
  - IBM invested $5B in its development
  - Production delays nearly bankrupted IBM
  - Spanned wide range of performances
    - Model 30: 8 KiB memory, 34.5 Kinstructions/second
    - Model 91: 6 MiB memory, 16.6 Minstructions/second



https://www.ibm.com/history/system-360

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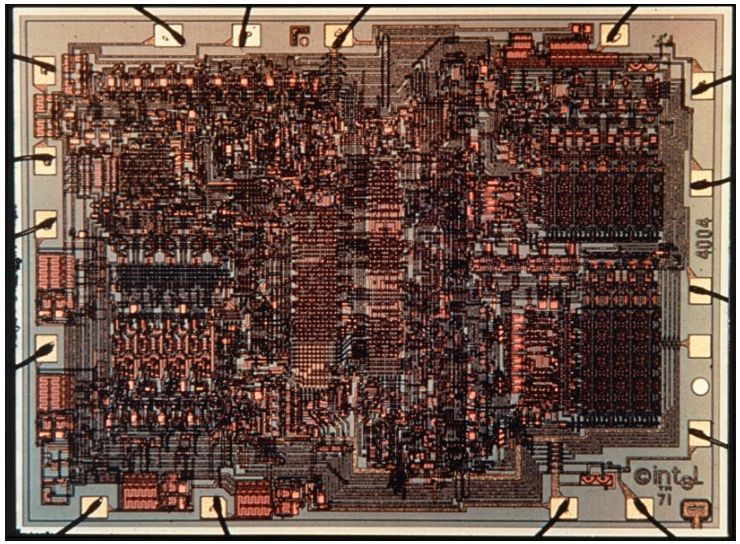
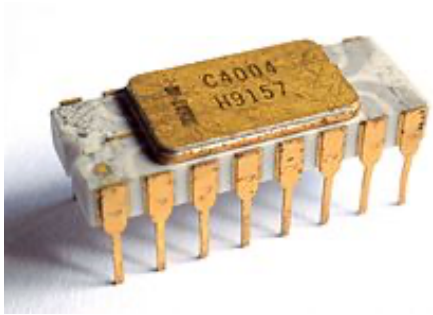
Intel's 4004

- First commercial microprocessor (processor built on a single chip):
  - 4-bit
  - Programmable
  - 2300 transistors
  - 10 μm silicon gate pMOS process
  - Layout done by hand



https://www.intel.com/content/www/us/en/history/virtual-vault/articles/the-intel-4004.html



https://spectrum.ieee.org/the-surprising-story-of-the-first-microprocessors

1969	4004
1970	PDP-11
1977	Apple II
1981	IBM PC
1982-1986	RISC
1992	Alpha 21064
1993	Pentium
1994-2006	MHz Wars
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Wider Availability of Computers

- **Apple II** (1977, cost: $1300): Low-cost 6502 makes computers widely available
- **IBM's Personal Computer (PC)** (1981, cost: $1565): Based on Intel's 8088, competitor to Apple II

Apple II

IBM PC

https://www.ibm.com/history/personal-computer

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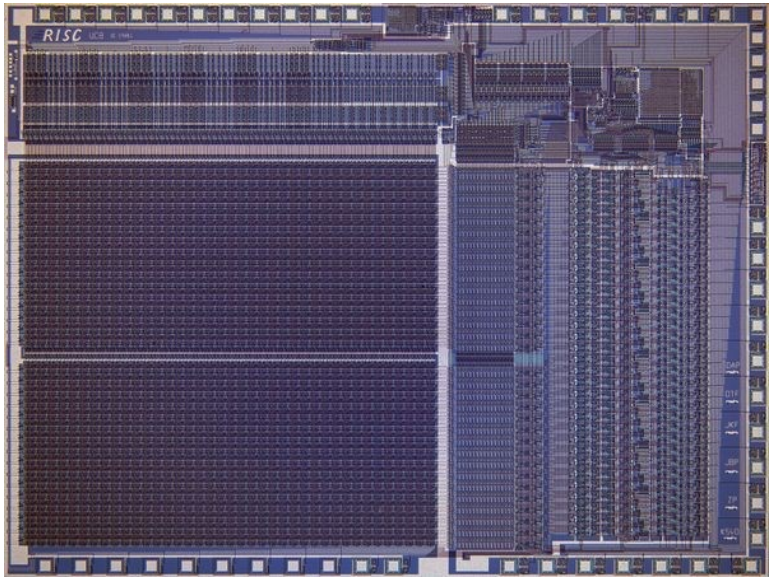
RISC

Reduced Instruction Set Computer (RISC):

- Co-invented by David Patterson and John Hennessy
- MIPS, SPARC, ARM



MIPS I die

Photo courtesy of David Patterson.

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2010	RISC-V

David Patterson

- Professor of Computer Science at the University of California, Berkeley since 1976
- Coinvented the Reduced Instruction Set Computer (RISC) with John Hennessy in the 1980s
- Founding member of RISC-V team.
- Was given the Turing Award (with John Hennessy) for pioneering a quantitative approach to the design and evaluation of computer architectures.

Photo used with permission.

John Hennessy

- President of Stanford University from 2000 - 2016
- Professor of Electrical Engineering and Computer Science at Stanford since 1977
- Coinvented the Reduced Instruction Set Computer (RISC) with David Patterson in the 1980s
- Was given the Turing Award (with David Patterson) for pioneering a quantitative approach to the design and evaluation of computer architectures.

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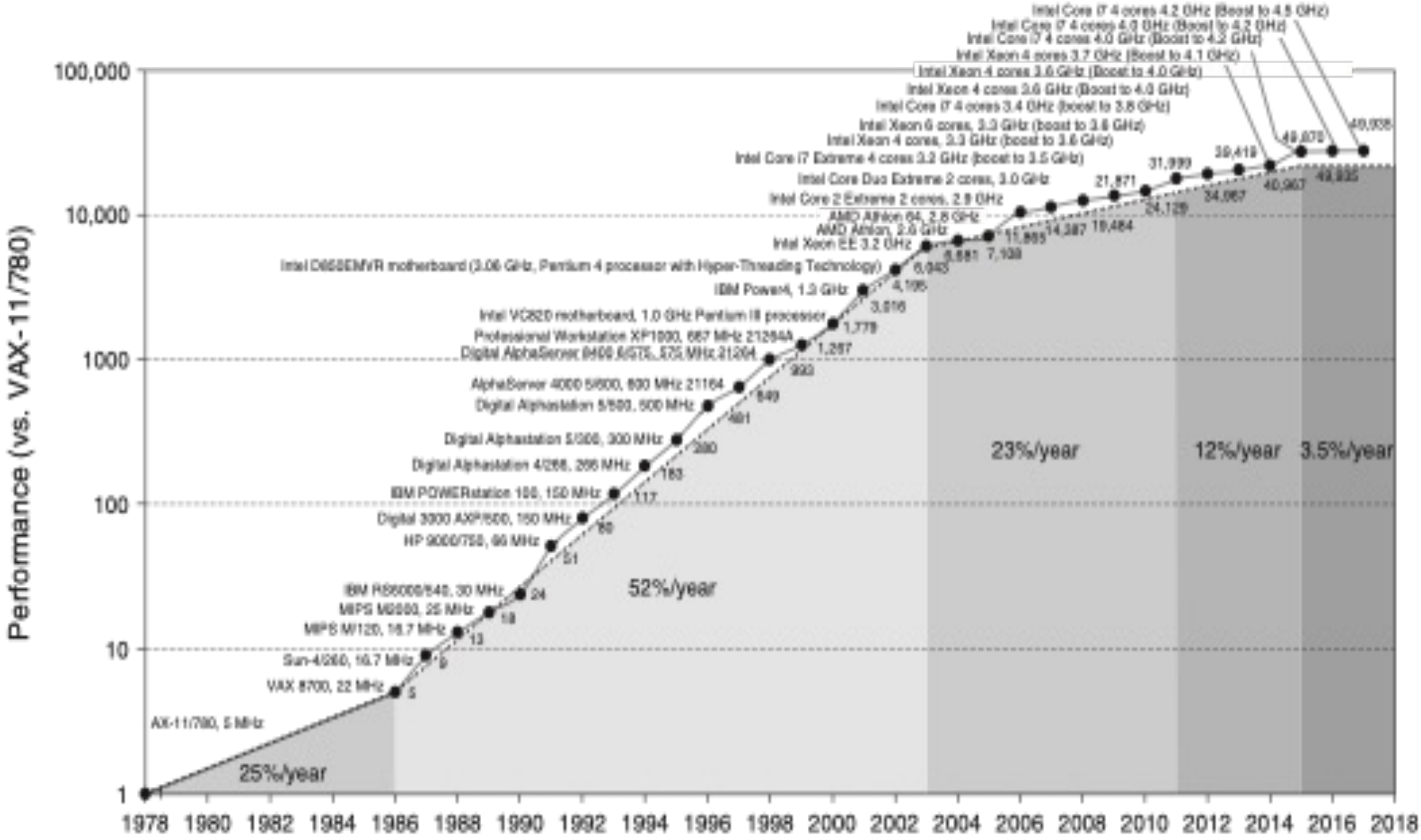
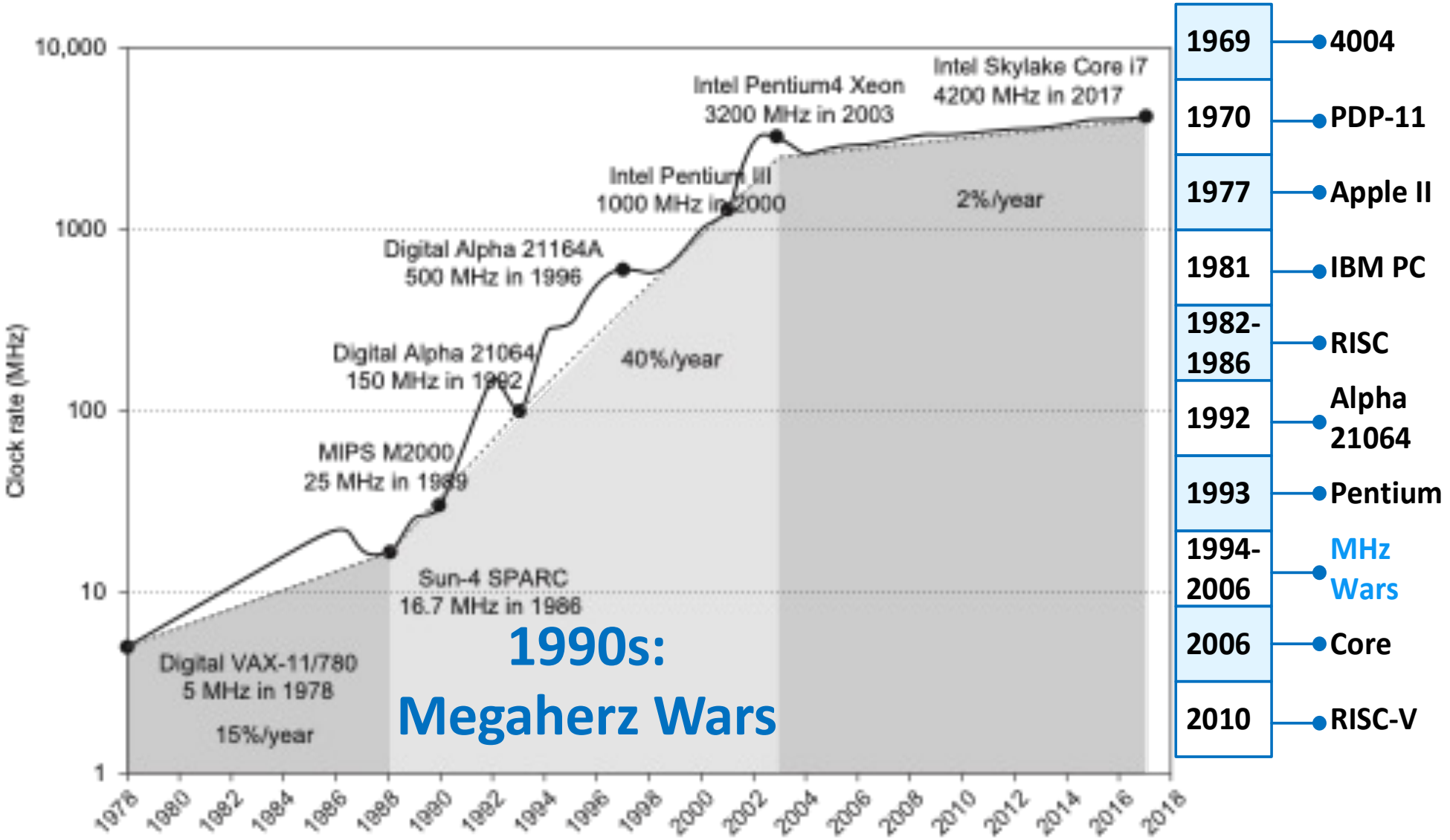
Processor Performance



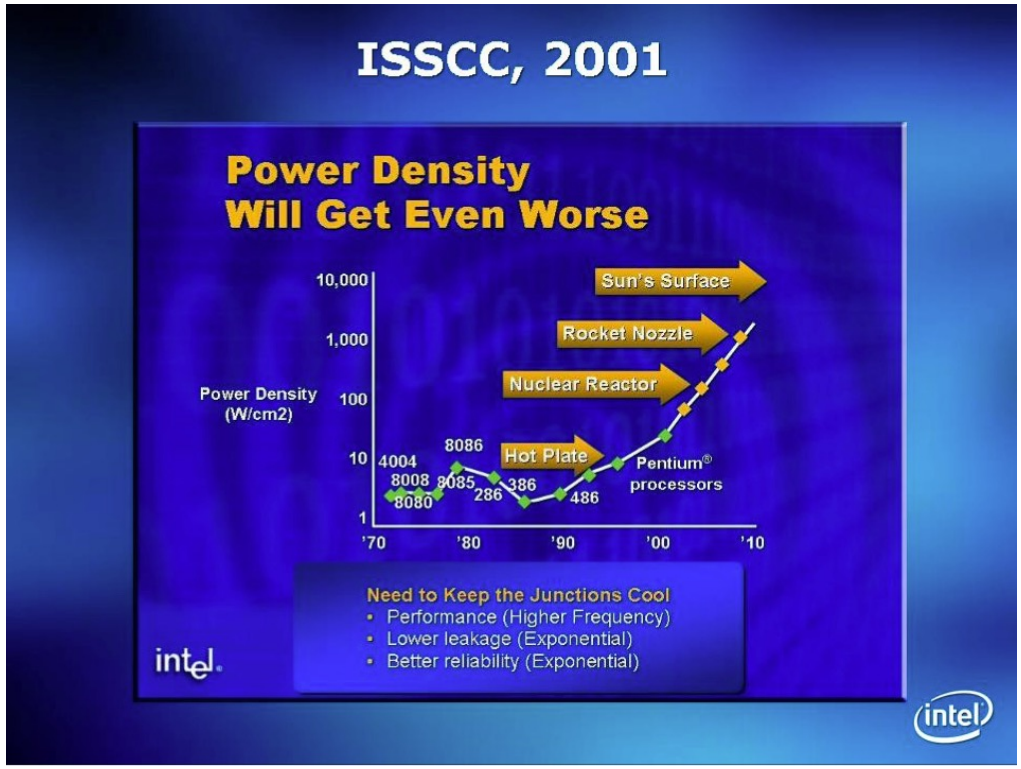
J. Hennessy and D. Patterson, *Computer Architecture: A Quantitative Approach*, 6th ed., Morgan Kaufmann, 2019.

Processor Clock Speed



J. Hennessy and D. Patterson, *Computer Architecture: A Quantitative Approach*, 6th ed., Morgan Kaufmann, 2019.

Power Density a Problem



https://web.stanford.edu/class/ee380/Abstracts/060607-EE380-Gelsinger.pdf

In 2006, Intel abandoned power-hungry Netburst μarchitecture

- Switched to **Core** μarchitecture
- **Multiple** power-efficient cores
- Attempts to increase performance from **parallelism**

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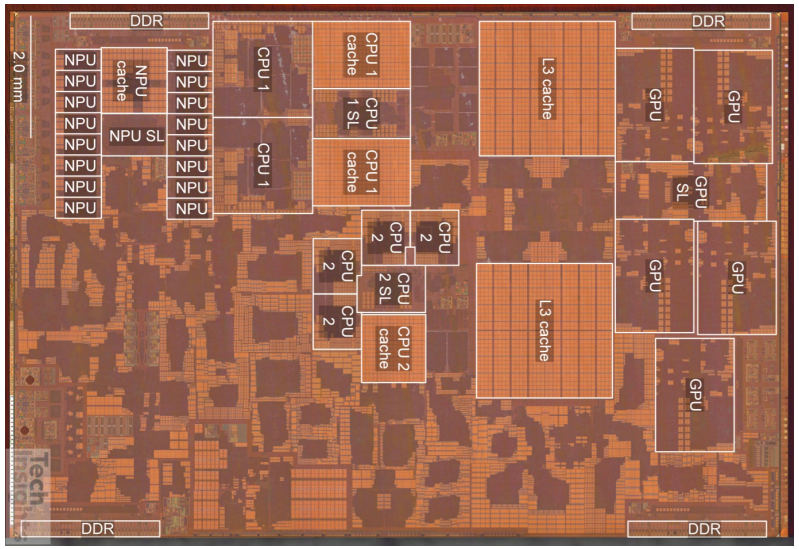
Contemporary Processors (2022)

Apple A15 Bionic (Phones)



6 cores
- 4 energy efficient 2 GHz
- 2 high performance 3.2 GHz

32 MiB system cache

Neural engine 15.8 TOP/s

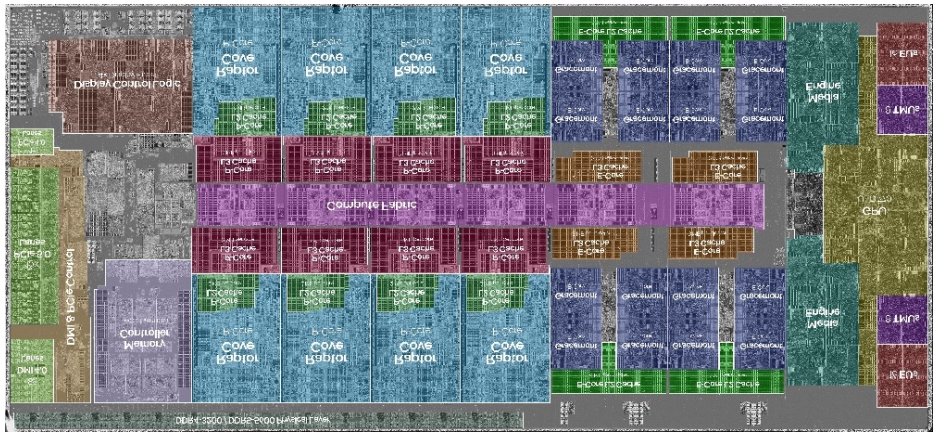
GPU, video, ISP

15 billion transistors

TSMC 5 nm process

http://www.techinsights.com/blog/teardown/apple-iphone-13-pro-teardown

Intel Raptor Lake Core i9 (Laptop/Desktop)



24 cores
- 16 energy efficient
- 8 high performance to 5.7 GHz

30 MiB L3$

Graphics & video accelerators

Memory, display, PCI controllers

257 mm^2 die

Intel 10 nm process

https://commons.wikimedia.org/wiki/File:Intel_Core_i9-13900K_Labelled_Die_Shot.jpg

About these Notes

RISC-V System-on-Chip Design Lecture Notes