FPGA Documentation

Lecture 05

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Outline

- Documentation Overview
- FPGA documentation Bingo
- Manual design mapping exercise
- Quick basic testbench review

Learning Objectives

By the end of this lecture you should be able to…

- Find basic specs in the FPGA documentation to answer questions about your system like DC logic levels, max clock speed, etc.
- Determine the number of logic cells required by simple Verilog modules.
- Recall how to write a Verilog testbench

Lattice iCE40UP Documentation

Documentation

Quick Reference	Technical Resources	Information Resources	Downloads
Key Documents	Reference Design	Product Brochure	IBIS Model
Data Sheet	Product Change Notification	Quality Assurance	
Application Note	Schematic	White Paper	
Pin & Package			
User Manual			

TITLE	NUMBER	VERSION	DATE	FORMAT	SIZE
iCE40 UltraPlus Family Data Sheet	FPGA-DS-02008	2.0	9/20/2021	PDF	1.1 MB
Memory Usage Guide for iCE40 Devices	FPGA-TN-02002	1.7	10/14/2020	PDF	954.3 KB
iCE40 I2C and SPI Hardened IP Usage Guide	FPGA-TN-02010	1.7	9/11/2020	PDF	1.3 MB
iCE40 SPRAM Usage Guide	FPGA-TN-02022	1.3	4/16/2021	PDF	912.9 KB
iCE40 Hardware Checklist	FPGA-TN-02006	2.0	3/10/2022	PDF	355.4 KB
iCE40 Oscillator Usage Guide	FPGA-TN-02008	1.7	1/25/2021	PDF	675 KB
iCE40 sysCLOCK PLL Design and User Guide	FPGA-TN-02052	1.4	4/30/2022	PDF	1.3 MB
iCE40 LED Driver User Guide	FPGA-TN-02021	1.5	11/29/2021	PDF	2 MB

Lattice iCE40UP Documentation

- Info on FPGA chip itself
  - DC logic levels
  - Timing information
  - Package dimensions
  - Pinout information
  - Block diagrams of internal components

iCE40 UltraPlus Family Data Sheet

Data Sheet

FPGA-DS-02008-2.0

Package Diagrams

Data Sheet

FPGA-DS-02053-6.8

UPduino Documentation

Specs specific to the UPduino board

- Schematics
- Supporting hardware
- Programming instructions

UPduino Documentation

tinyVision.ai

UPDuino v3.0: PCB Design Files, Designs, Documentation

The UPDuino v3.0 is a small, low-cost FPGA board. The board features an on-board FPGA programmer, flash and LED with _all_ FPGA pins brought out to easy to use 0.1" header pins for fast prototyping.

The tinyVision.ai UPduino v3.0 Board Features:

- Lattice UltraPlus ICE40UP5K FPGA with 5.3K LUTs, 1Mb SPRAM, 120Kb DPRAM, 8 Multipliers
- FTDI FT232H USB to SPI Device
- _ALL_ 32 FPGA GPIO on 0.1" headers
- _ALL_ FTDI pins brought to test points
- 4MB SPI Flash
- RGB LED
- On board 3.3V and 1.2V Regulators, can supply 3.3V to your project
- Open source schematic and layout using KiCAD design tools
- Integrated into the open source APIO toolchain

FPGA Documentation Bingo

Bingo Card

Question	Answer	Reference
Recommended operating voltage for VCCIO	1.71-3.46 V	Table 4.2, p. 29
I/O pin input capacitance	C1 = 6 pF	Table 4.5, p. 32
3.3 V LVCMOS Logic Levels	VIL (-0.3, 0.7) VIH (2.0, VCCIO + 0.2), VOL 0.4, VOH 0.4	Table 4.18, p. 34
Recommended core input voltage	1.14-1.26 V	Table 4.2, p. 29
Maximum speed of sysI/O buffer	250 MHz	Table 4.19, p. 36
Maximum PLL output frequency	275 MHz	Table 4.22, p. 38
Maximum output current	+/- 8 mA	Table 4.13, p. 34
Operating temperature range	-65-125 ˚C	Table 4.1, p. 29
Input leakage current	IIl, IIH = 10 µA	Table 4.5, p. 32
What FPGA device is on the UPduino v3.1 board?	ICE40UP5K-SG48ITR	UPduino schematic
Major elements in a Logic Cell (LC)	4-input LUT, 1-bit DFF, Carry logic	Figure 3.2, p. 12
What is the range of clock frequencies for the high speed internal oscillator?	48 MHz, +/-20%	Table 4.11, p. 34
How many logic element are on our FPGA?	5280	Table 2.1, p. 9; multiple

Bingo Card

Question	Answer	Reference
How many EBR memory blocks?	30,120 Kbits total	Table 2.1, p. 9
How many SPRAM memory blocks?	4, 1024 Kbits total	Table 2.1, p. 9
What is the difference between EBR and SPRAM?	EBR can be configured at boot, SPRAM no	
How many I/O banks?	3 (0, 1, 2)	Figure 3.9, p. 24
Data buss skew across a bank of I/Os?	510 ps	Table 4.21, p. 37
Propagation delay through 4-input LUT?	9 ns	Table 4.21, p. 37
PIO input register setup time	-0.5 ns	Table 4.21, p. 37
PIO input register hold time	5.55 ns	Table 4.21, p. 37
PIO output register clock to output (Q)	10 ns	Table 4.21, p. 37
Number of multipliers in the FPGA	Single 16-bit x 16-bit or two 8-bit x 8-bit	Section 3.1.7, p. 18
Package for our FPGA chip	SG48 (48-pin QFN 0.50 mm pin pitch)	UPduino Documentation
How many user I/Os does the FPGA chip have?	39	Table 2.1, p. 9; multiple
What is the area of the FPGA package?	7 mm x 7 mm	Package Diagrams document, p. 36
What voltage does the FPGA core run on?	1.2 V	Table 4.2, p. 29

Manual Design Mapping

Going from Verilog HDL to logic cells

- 2-input AND: 1 LE
- 4-input AND: 1 LE
- 5-input AND: 2 LE
- 16-input AND: 5 LEs
- Arbitrary function of 5 inputs: 3 LEs (f(0), f(1), select between)
- Arbitrary function of 6 inputs: 7 LEs (4 functions of 4 inputs, two levels of 2:1 mux to choose output from the four individual 4-input LUT.)
- 2 inverters: 2 LEs
- Divide by 3 counter: 2 LEs (2 flops + 2 functions of 2 inputs)

Wrap up

- FPGA documentation contains important information like logic levels and timing specs
- Learning to navigate the documentation is a skill that must be practiced. Try to browse instead of search.
- As a hardware designer, you should be able to explain how many logic cells

Announcements/Reminders