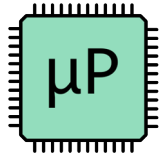
Graphics and Displays

Lecture 19

Microprocessor-based Systems (E155)

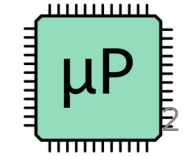
Prof. Josh Brake



Outline

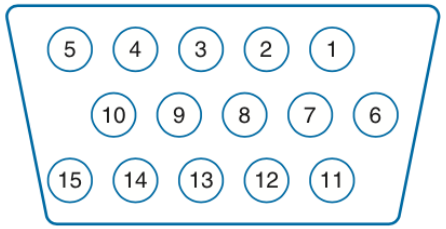
- Video Graphics Array (VGA)
- Liquid Crystal Display (LCD)
- Digital Visual Interface (DVI) and High-Definition Multimedia Interface (HDMI)

Video Graphics Array (VGA)



Video Graphics Array (VGA) History

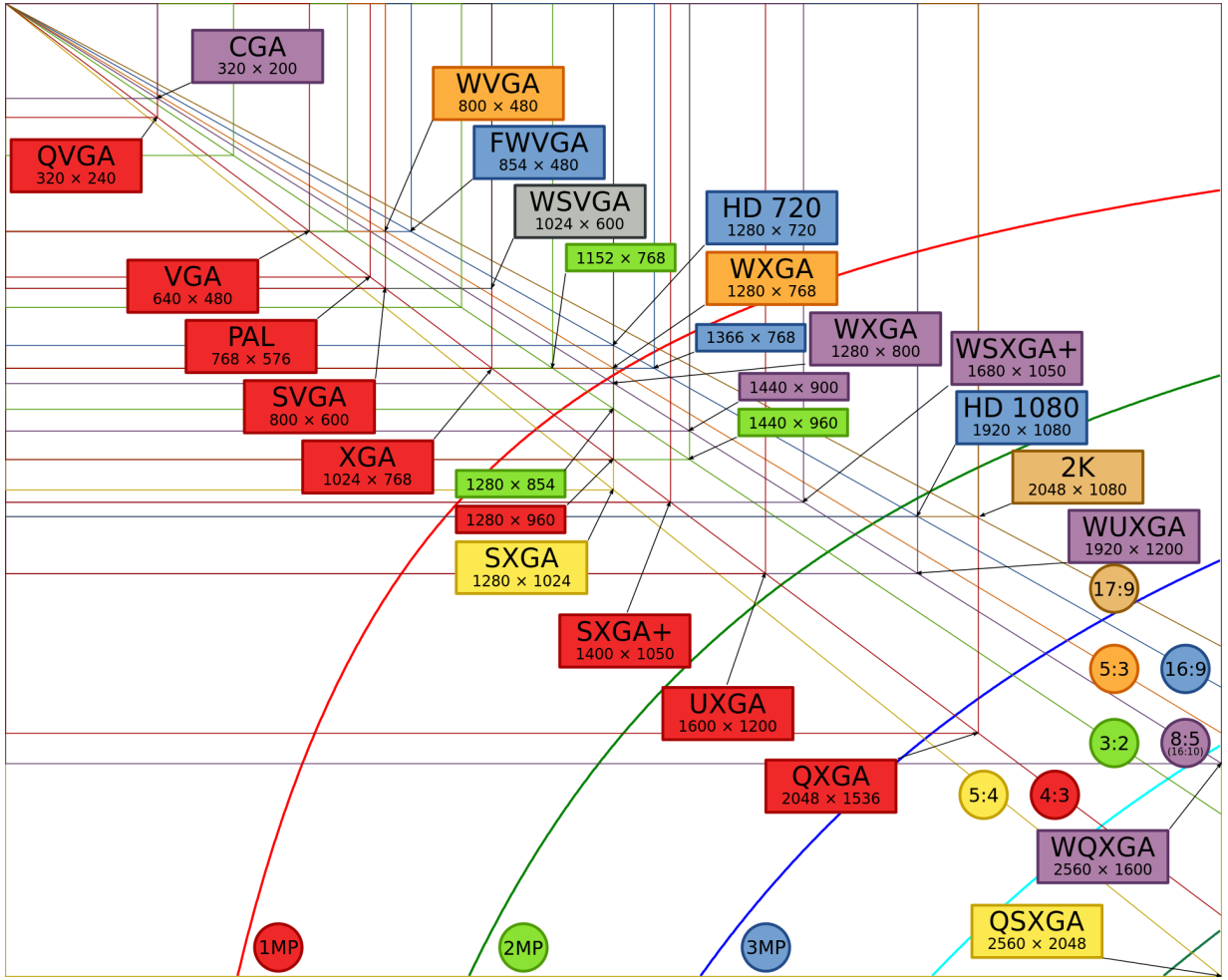
- Introduced in 1987 for the IBM PS/2 computers
- Video information relayed using analog voltages
- 15-pin connector



1: Red
2: Green
3: Blue
4: Reserved
5: GND
6: GND
7: GND
8: GND
9: 5 V (optional)
10: GND
11: Reserved
12: I^2C data
13: Hsync
14: Vsync
15: I^2C clock

Figure e9.27 VGA connector pinout

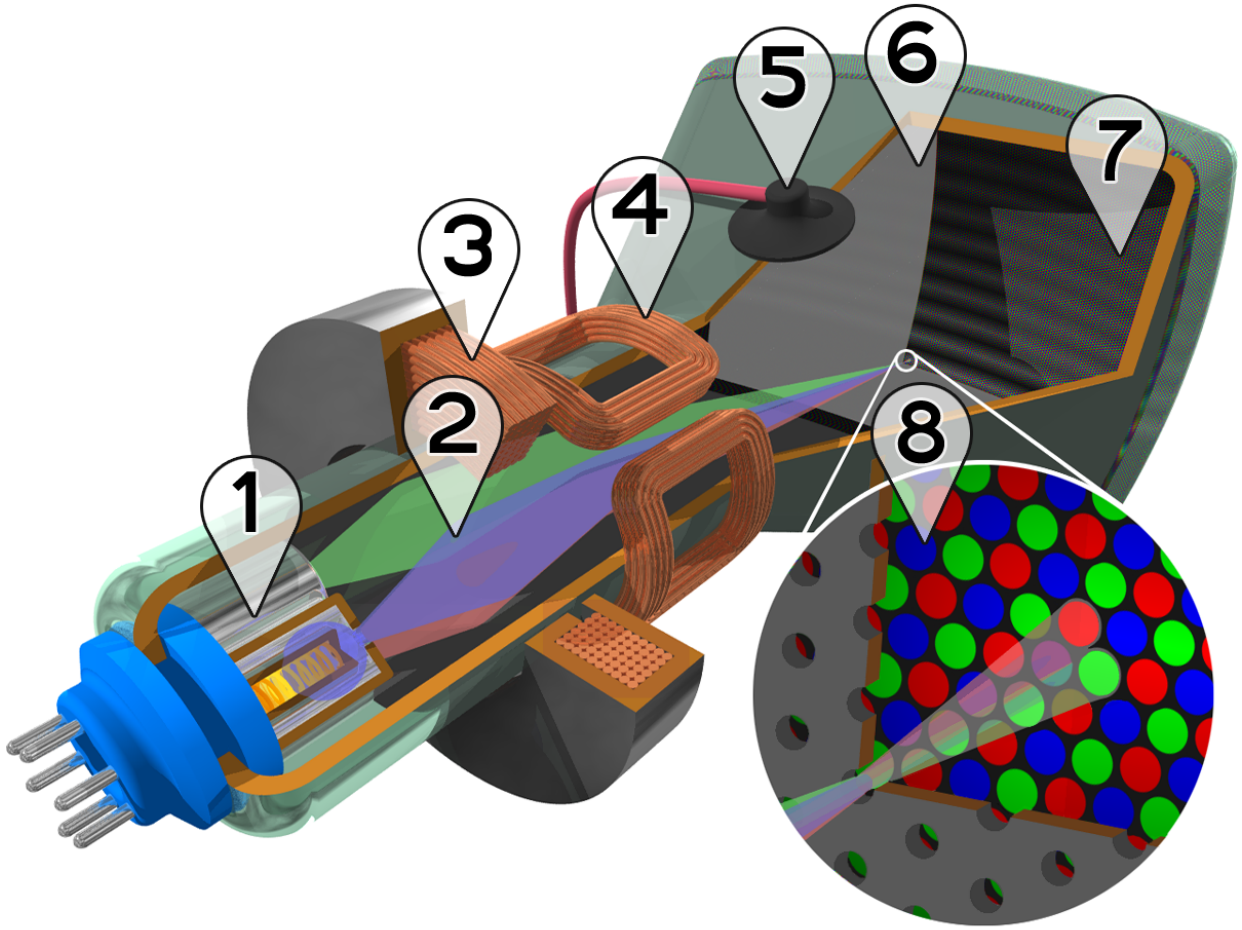
Figure e9.27 in DDCA ARMed Edition



[Comparison of standard resolutions including VGA's 640x480](#) by [XXV](#) under [CC BY-SA 3.0](#)

VGA and Cathode Ray Tubes (CRTs)

1. Electron beam emitters
2. Electron beams
3. Focusing coils
4. Deflection coils
5. Connection for final anodes
6. Mask for separating red, green, and blue zones
7. Cluse-up of phosphor-coated inside of screen



VGA Timing

- Cathode ray tube work by raster scanning left to right and exciting fluorescent material for each pixel.
- At the end of the line, the gun turns off for the *horizontal blanking interval* to return to the beginning of the next line.
- After all lines are complete, it turns off for the *vertical blanking interval* to return to the top left
- Each line begins and ends with a "*porch*" which is a blank area of zeros where the CRT gun is turned off while it is moving in position for the next line. These porches exist for both horizontal and vertical lines.

VGA Timing

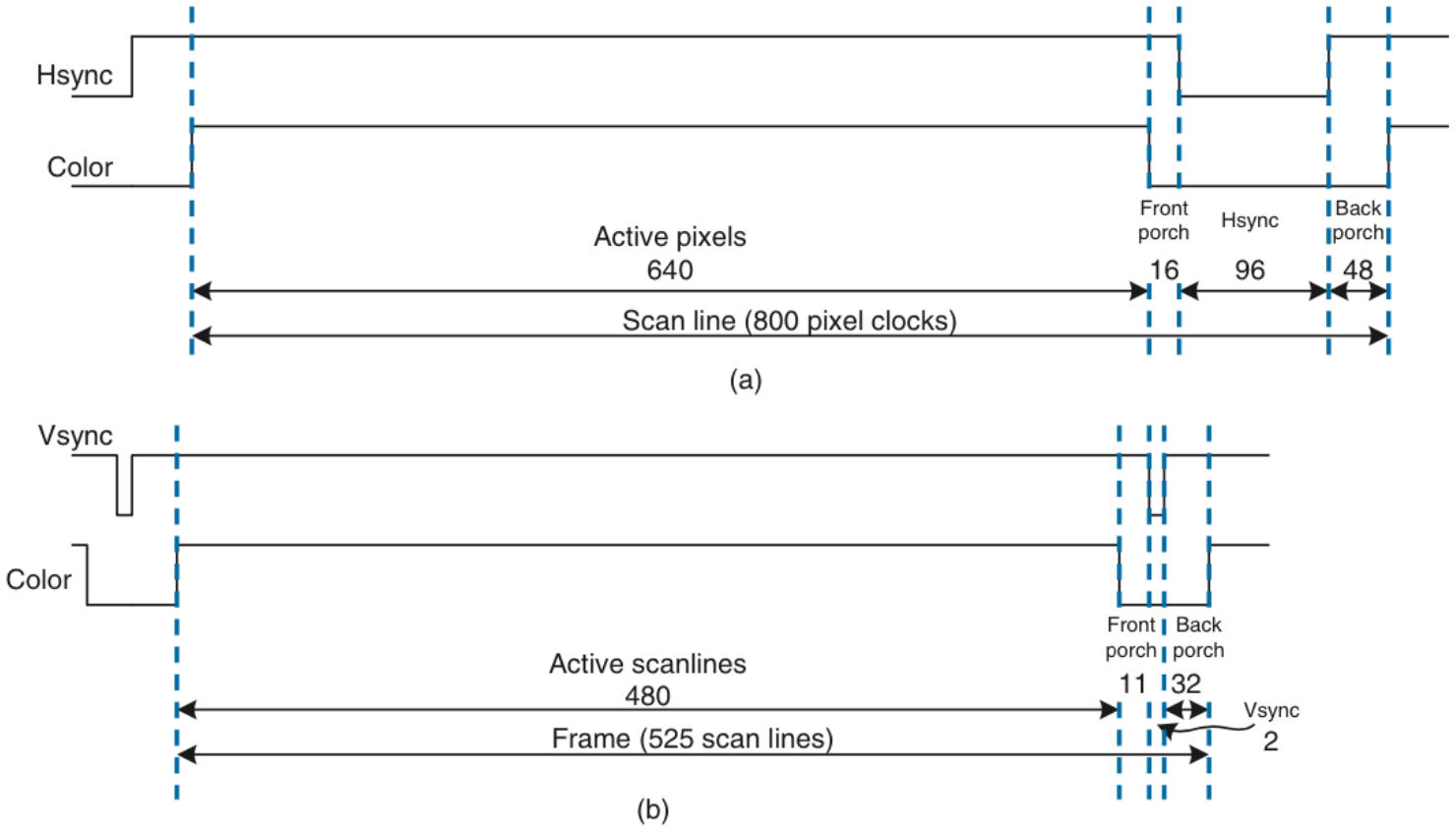
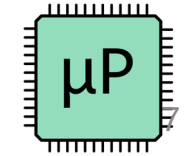


Figure e9.26 VGA timing: (a) horizontal, (b) vertical

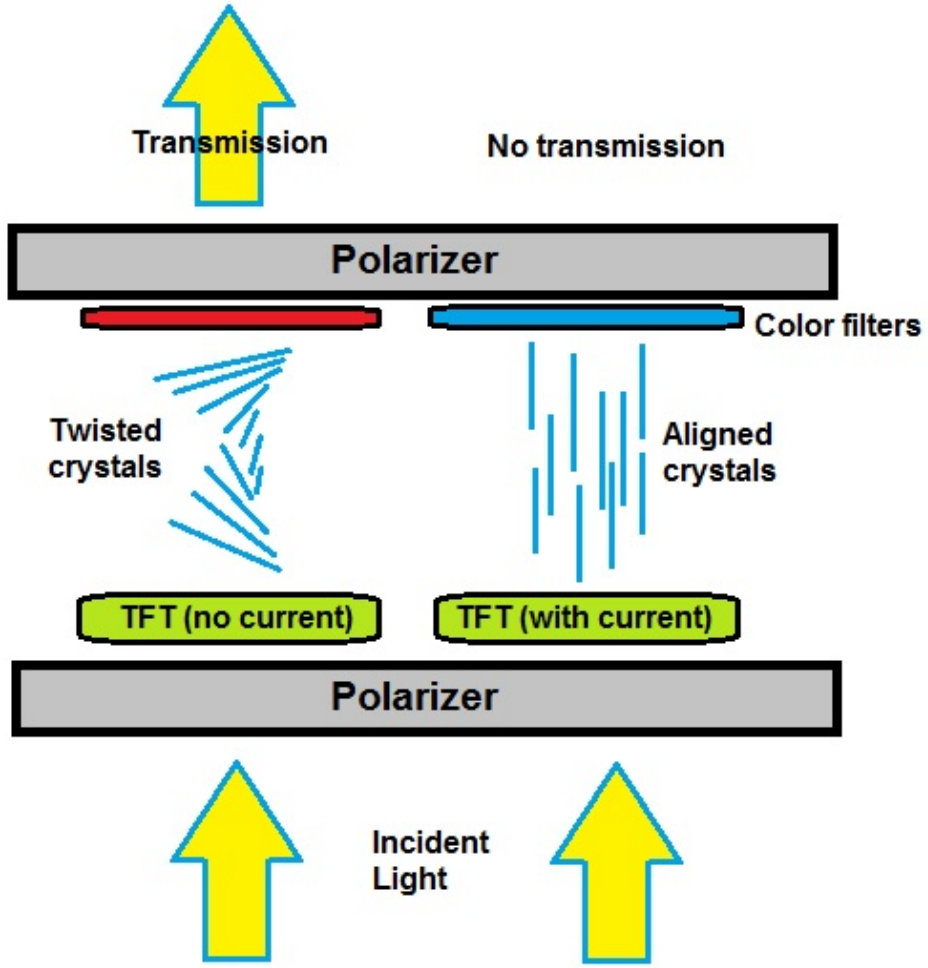
Figure e9.26 in DDCA ARMed Edition

Liquid Crystal Display (LCD) Technology



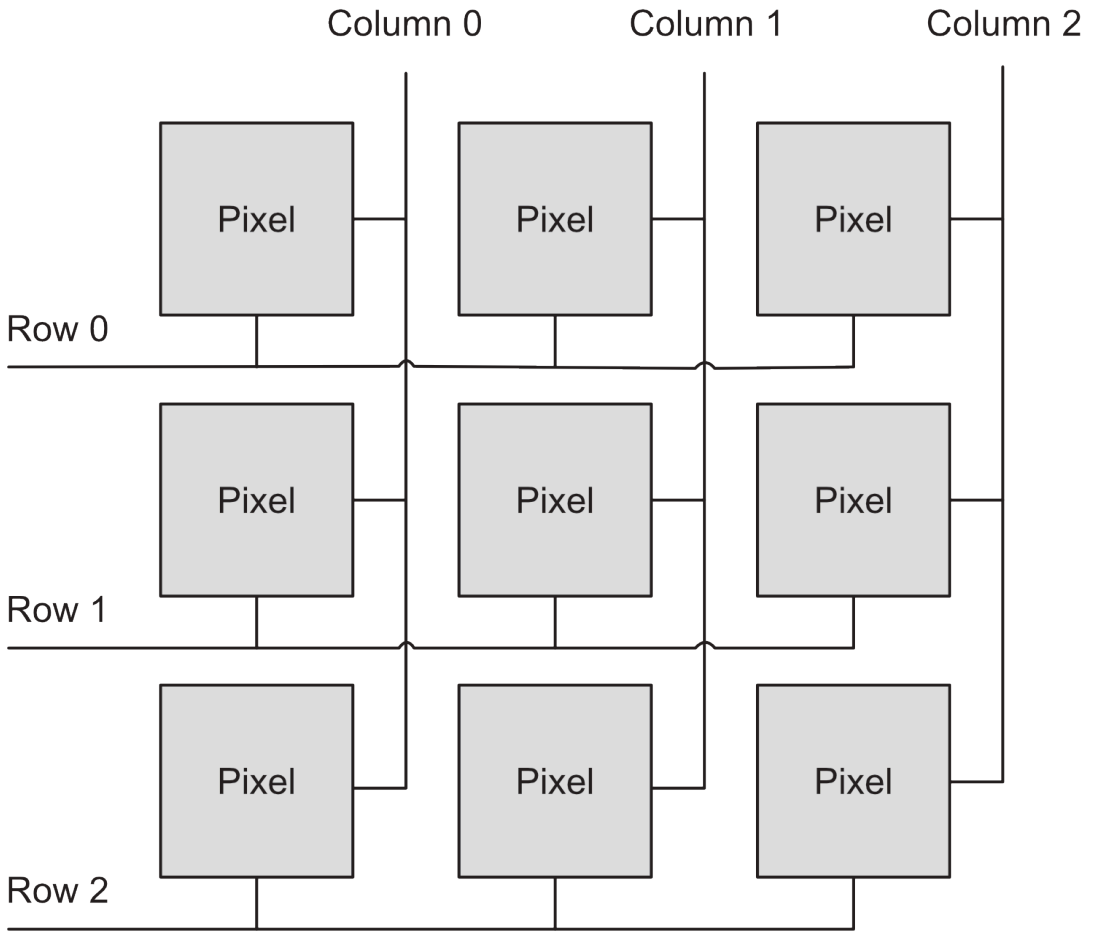
Liquid Crystal Display (LCD)

- Liquid crystals under electric field used to change the polarization of light traveling through it.
- When not energized, light is transmitted through cross polarizers
- When energized, light does not pass through crossed polarizers



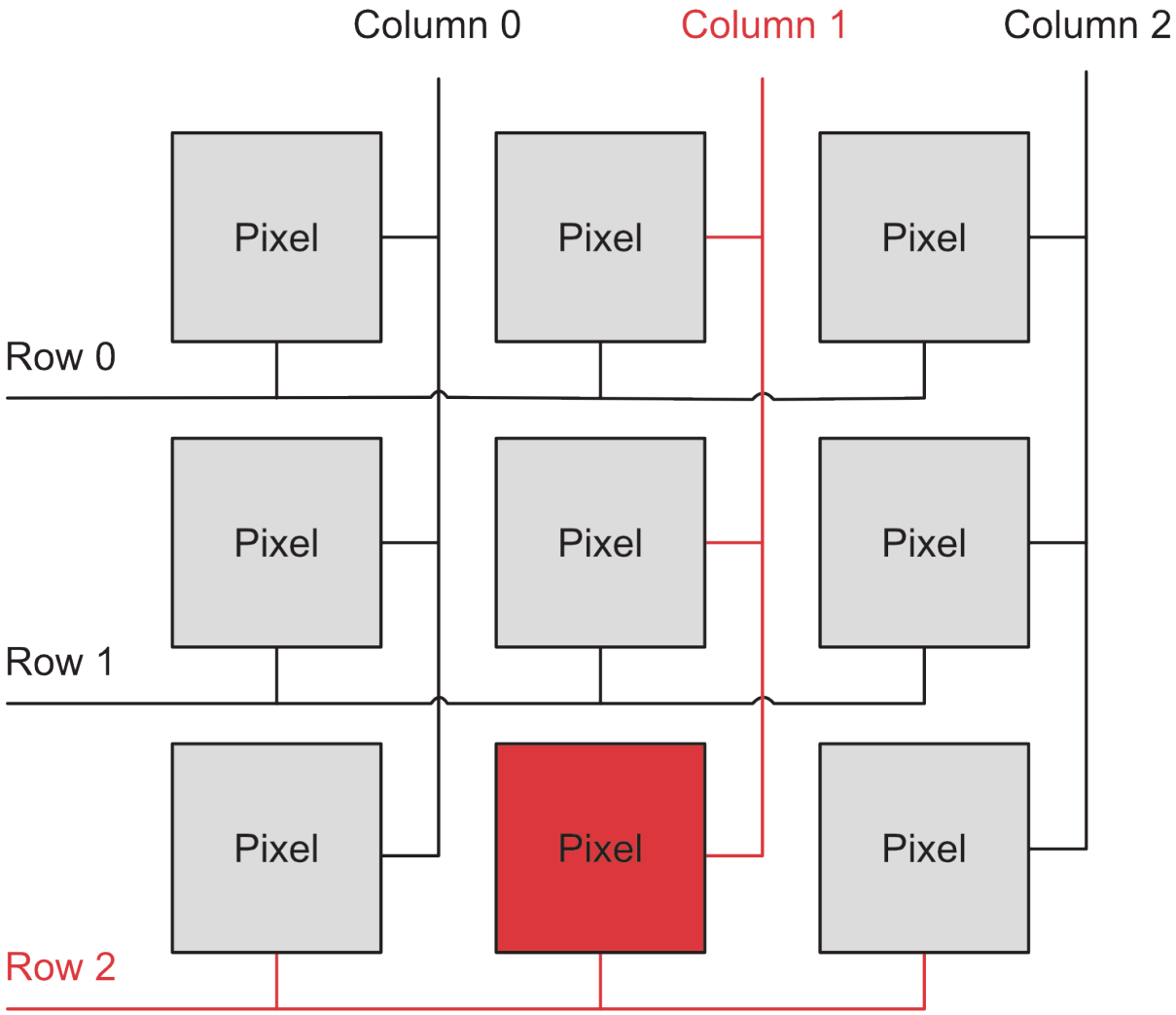
LCD Matrix

- Pixels are arranged in a grid
- All pixels on a row and column are connected



Selecting Pixel in LCD

- To select a given pixel, choose its row and column
- *Passive* matrices use liquid crystal for each pixel.
- *Active* matrices add thin-film transistor to actively maintain its state while other pixels are addressed



LCD Timing

- Same ideas as in VGA, but now we are just dealing with selecting individual pixels instead of scanning electron beam

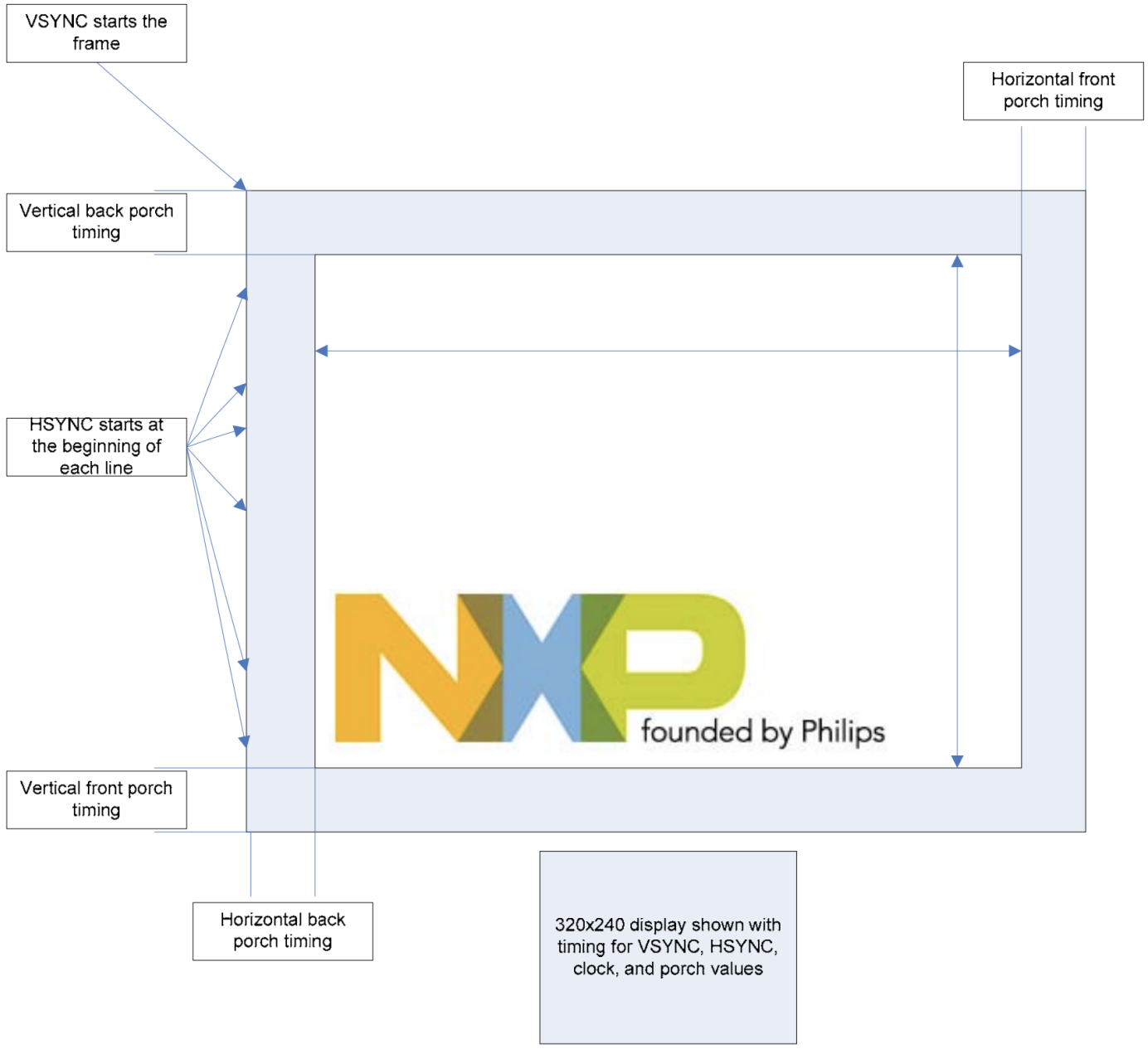
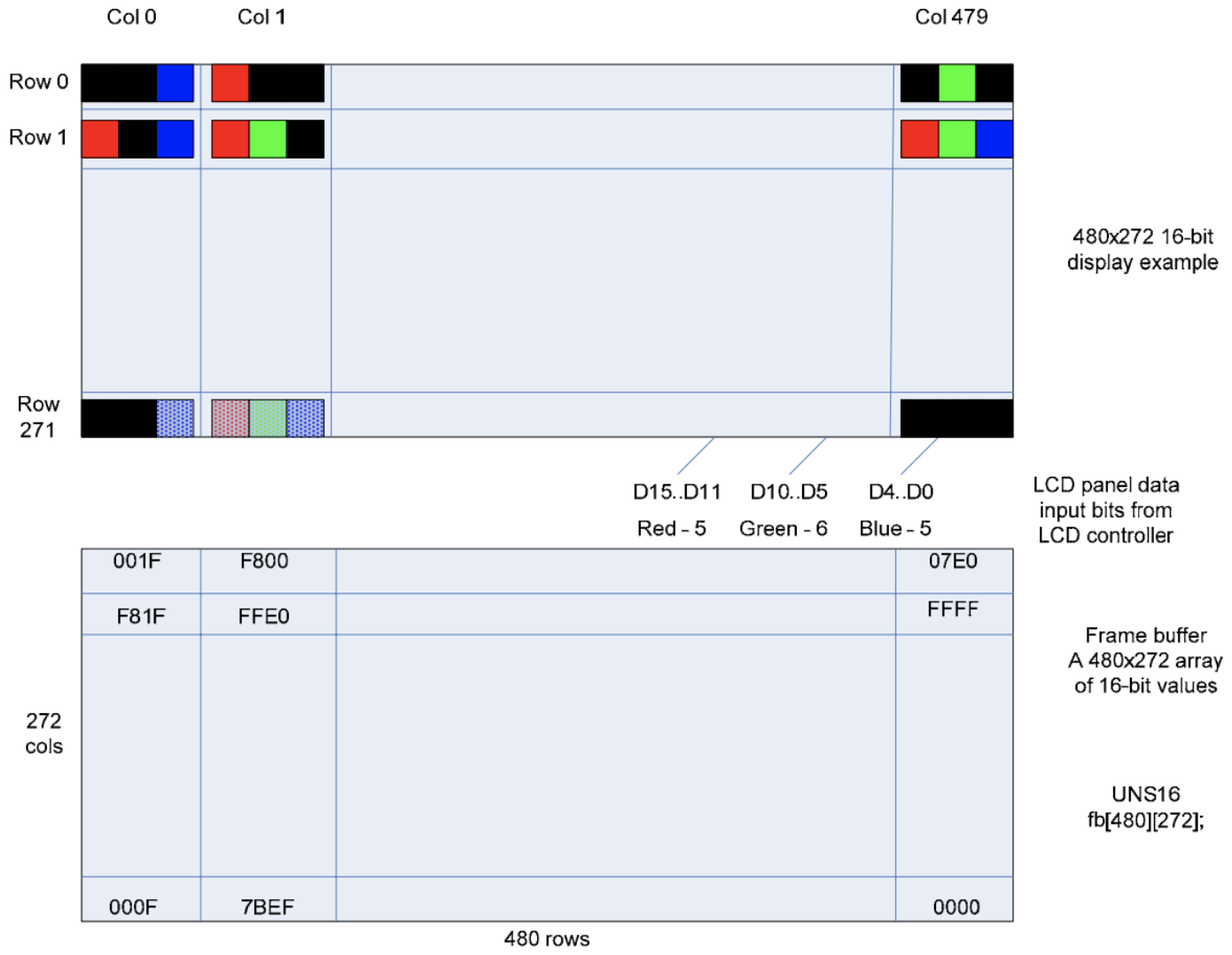


Figure from [Introduction to graphics and LCD technologies]

Frame buffer

- The frame buffer is an array of memory used to store the data to be displayed
- Double buffered displays have two buffers so that the display can be updated without directly writing to the display.

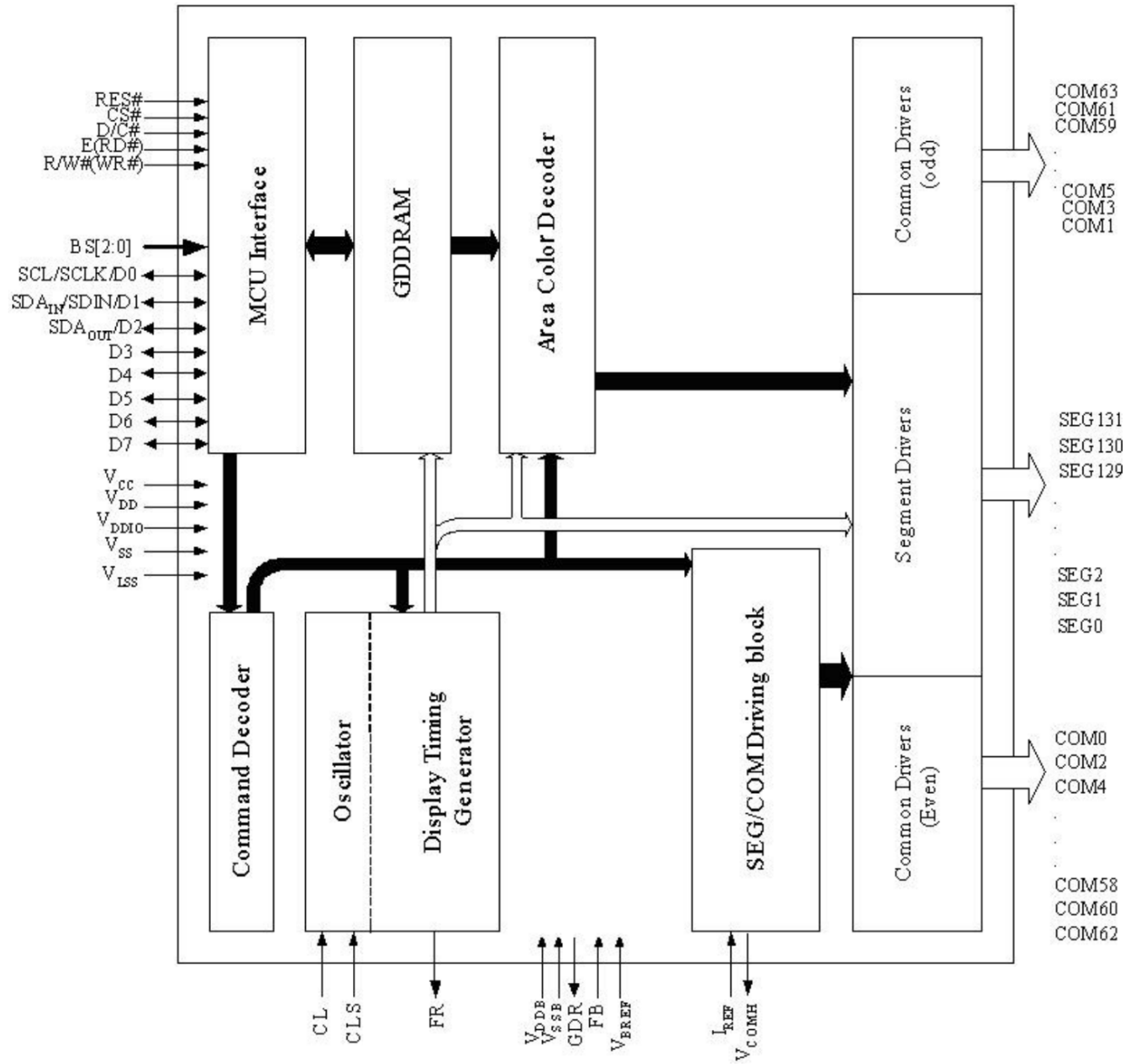


Frame Buffer 16bpp from Introduction to graphics and LCD technologies

SSD1305 Driver

- Time multiplexing to drive array

Figure 4-1 : SSD1305 Block Diagram



Digital Visual Interface (DVI) and High-Definition Multimedia Interface (HDMI)

Why use DVI?

- LCDs are inherently digital and converting from digital to analog and then back again wastes time, energy, and reduces fidelity.

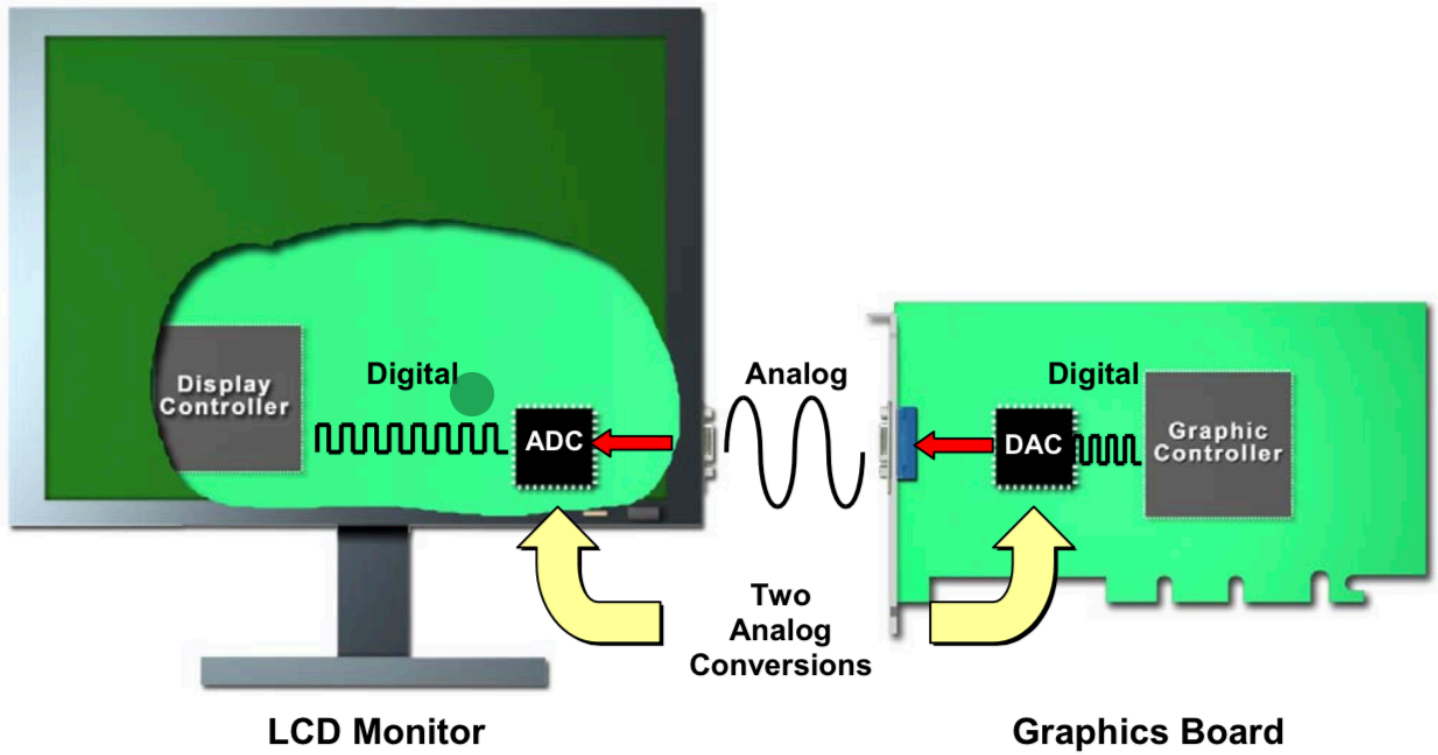


Figure 2: Analog Conversions

Figure from [DVI and TMDS Extensions - Silicon Image White Paper]

DVI History

- Developed in 1998 by the Digital Display Working Group (DDWG). Composed of Fujitsu, Compaq, HP, IBM, Intel, NEC, and Silicon Image
- DVI 1.0 spec released in April 1999
- Transition minimized DC-balanced signaling (TMDS) is key enabling cost-effective digital data at high rate and also allowing bandwidth to be doubled with a second link.

Why not use Low-Voltage Differential Signaling (LVDS)

- LVDS's speed (and thus resolution) limited by cable length. DVI supports up to 15 meter cable length.
- No universal connector solution
- LVDS can only support up to QXGA (2048 x 1536)

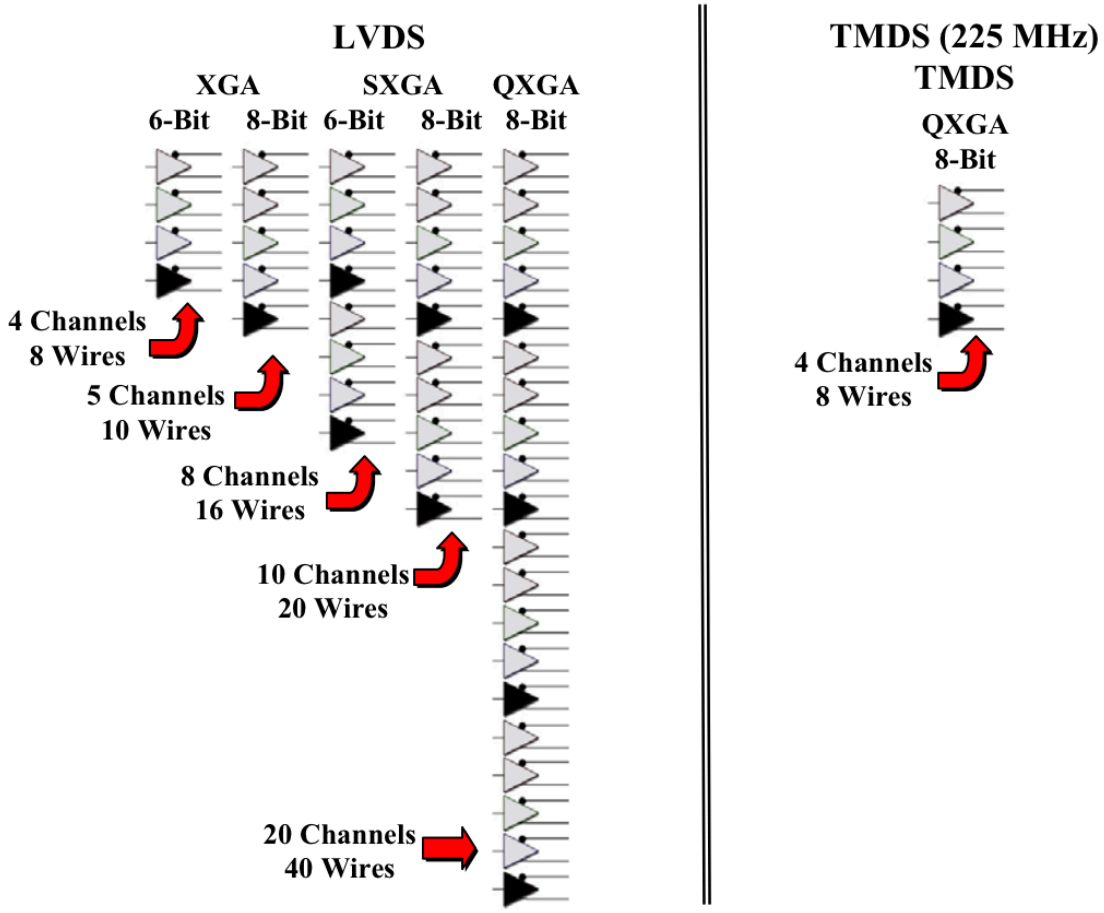


Figure 1: LVDS vs. TMDS

[DVI and TMDS Extensions - Silicon Image White Paper]

DVI Components

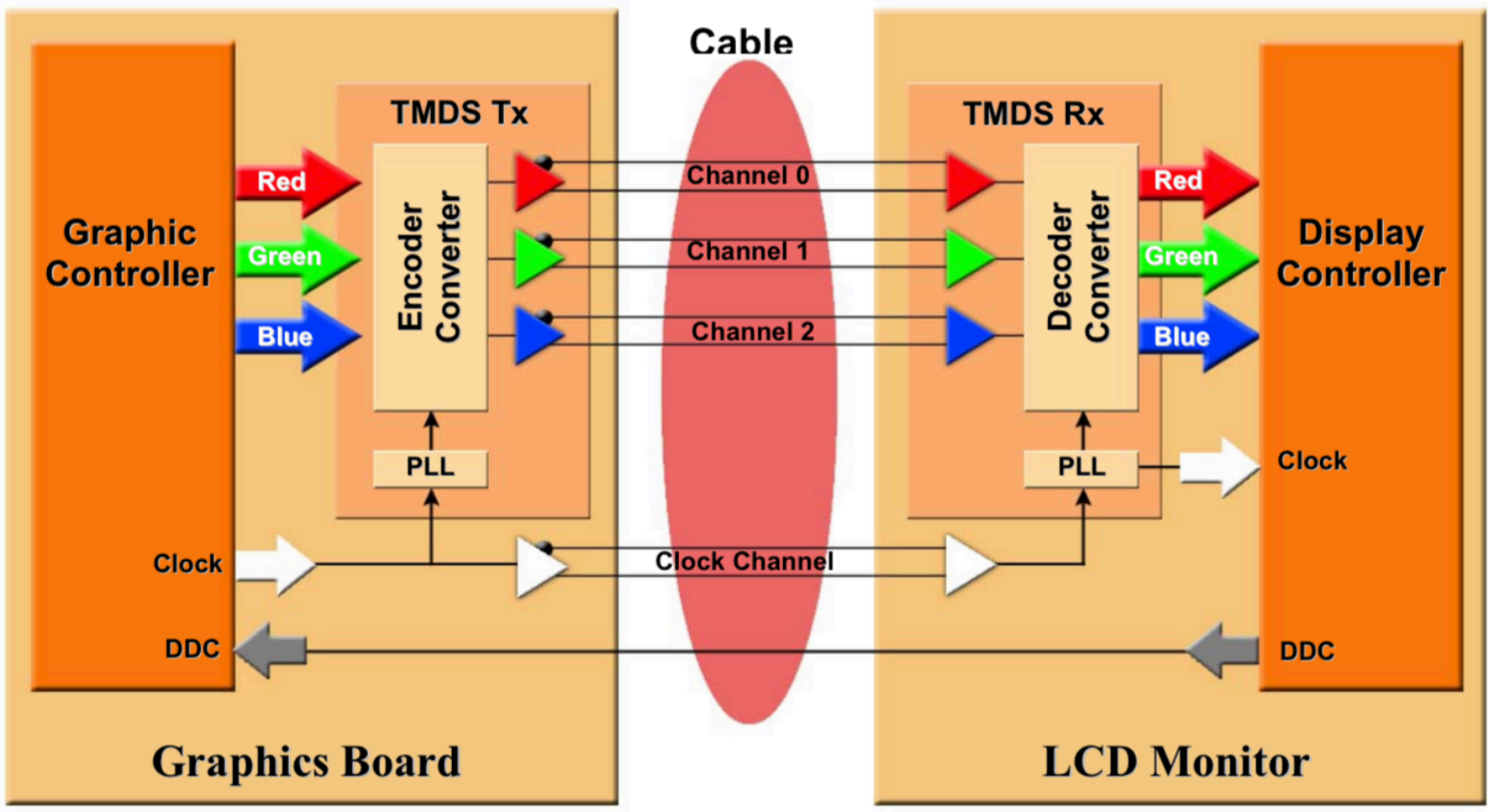


Figure 5: Single-Link DVI

Figure from [DVI and TMDS Extensions - Silicon Image White Paper]

DVI Components

- TMDS transmitter
  - Prepares 24 bits of parallel data (8 bits for each color channel) for serial transmission by encoding and serializing it
  - 4 channels: clock, R, G, and B.
- TMDS receiver
  - Converts from serial data stream to parallel output
- DVI connector
- DVI cable

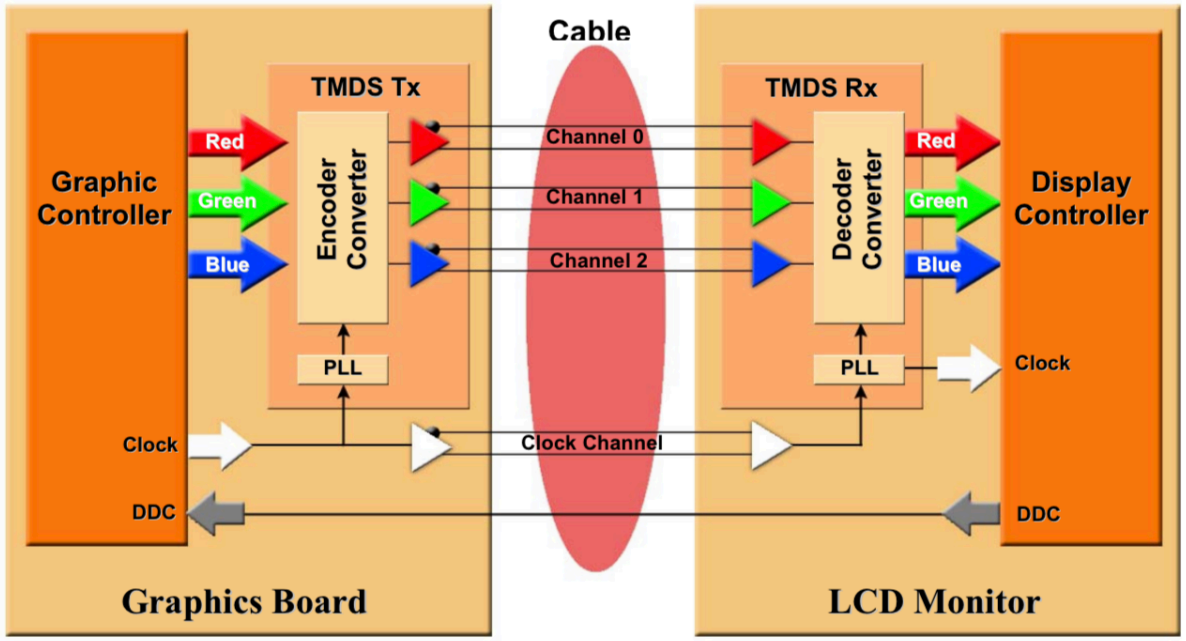


Figure 5: Single-Link DVI

Figure from [DVI and TMDS Extensions - Silicon Image White Paper]

Video Signal

- Uses transition-minimized differential signaling
- TMDS = transition-minimized differential signaling
- 4 TMDS differential pairs of interest
  - clock +/-
  - data0 +/-
  - data1 +/-
  - data2 +/-
- Data lines used for RGB color signals

TMDS Signal: Transition minimization

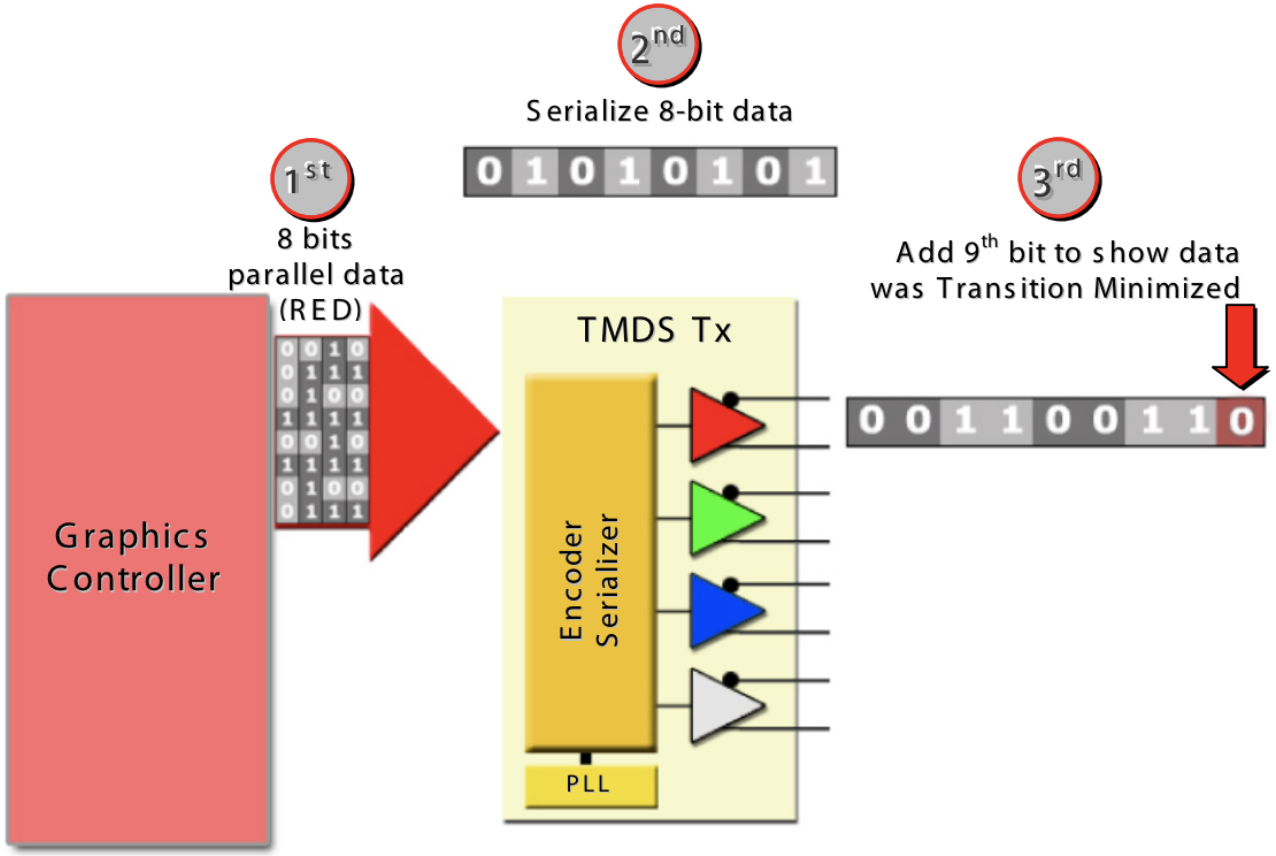


Figure 7: TMDS Transmitter

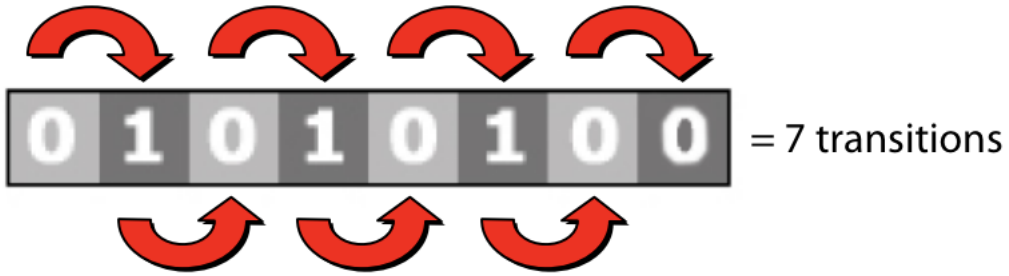


Figure 8: Too Many Data Transitions

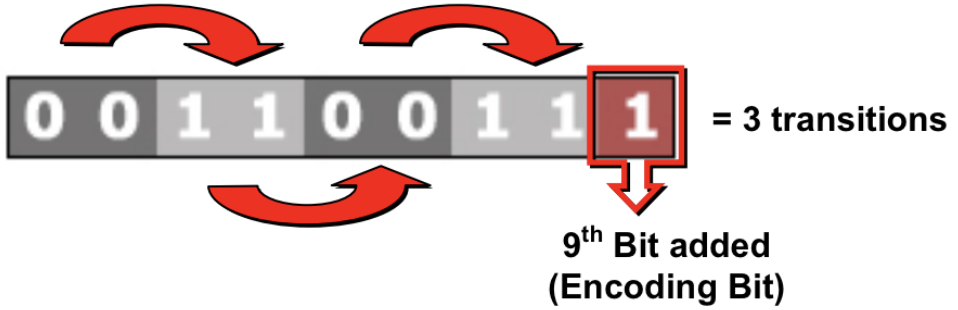


Figure 9: Minimizing Transitions

Figures from [DVI and TMDS Extensions - Silicon Image White Paper]

TMDS Signal: DC-balancing

- Use two lines instead of one where they are opposites of each other
- Common mode noise is rejected

Figure 16: Differential Signal

Figure 17: Differential Signal (Two Wires)

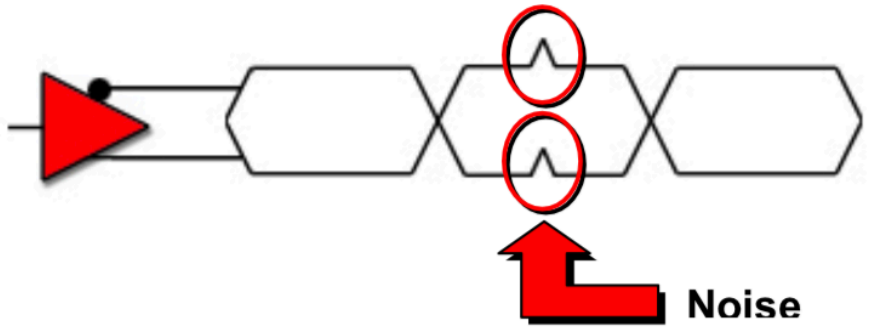


Figure 18: Noise on Line

Figures from [DVI and TMDS Extensions - Silicon Image White Paper]

TMDS Algorithm

D, C0, C1, DE	The encoder input data set. D is eight-bit pixel data, C1 and C0 are the control data for the channel, and DE is data enable
cnt	This is a register used to keep track of the data stream disparity. A positive value represents the excess number of "1"s that have been transmitted. A negative value represents the excess number of "0"s that have been transmitted. The expression cnt{t-1} indicates the previous value of the disparity for the previous set of input data. The expression cnt(t) indicates the new disparity setting for the current set of input data.
q_out	These 10 bits are the encoded output value.
$N_1\{x\}$	This operator returns the number of "1"s in argument "x"
$N_0\{x\}$	This operator returns the number of "0"s in argument "x"

Table 3-1 Encoding Algorithm Definitions

Algorithm details from Digital Visual Interface DVI Rev. 1.0 from Digital Display Working Group

TMDS Algorithm

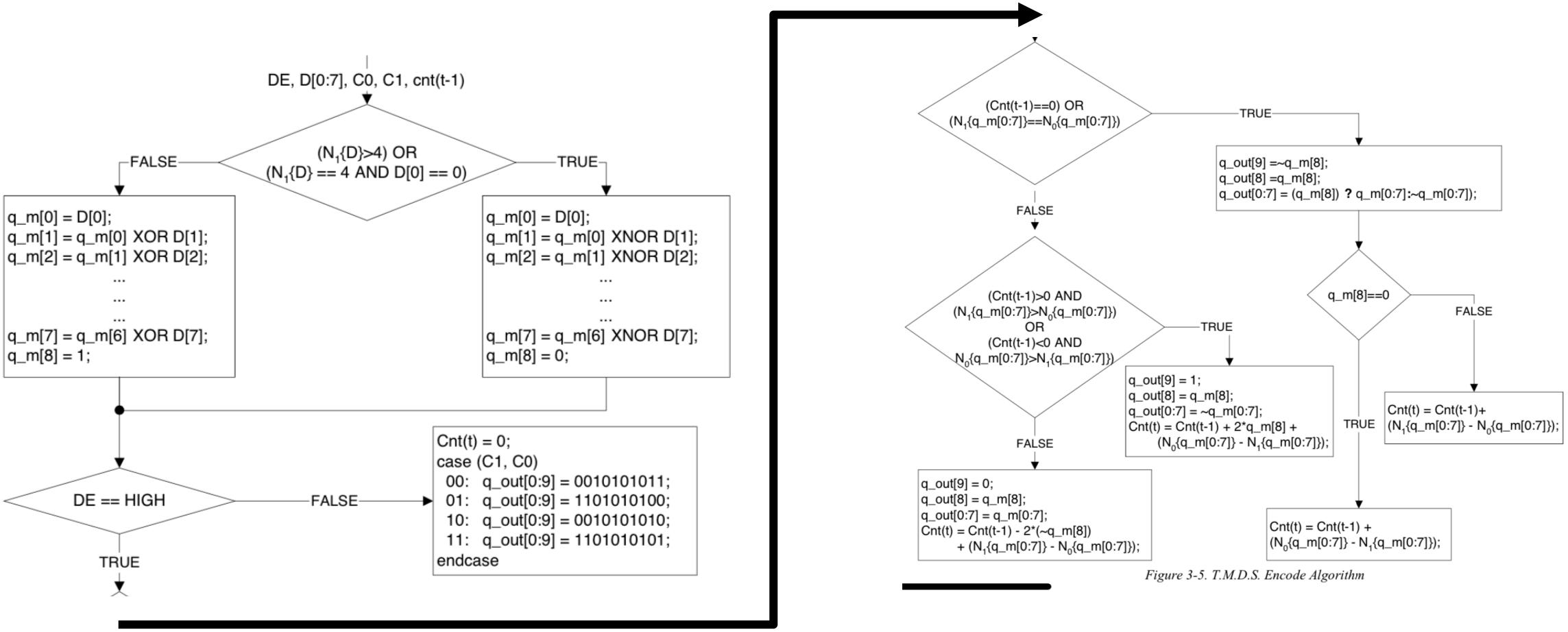


Figure 3-5. T.M.D.S. Encode Algorithm

Algorithm details from [Digital Visual Interface DVI Rev. 1.0 from Digital Display Working Group]

DVI Pinout

- DVI pinout contains three main pieces
  - TMDS signals
  - Plug & Play signals
  - Analog signals

Pin	Signal	Pin	Signal	Pin	Signal
1	Data 2 -	9	Data 1 -	17	Data 0 -
2	Data 2 +	10	Data 1 +	18	Data 0 +
3	Shield (2 & 4)	11	Shield (1 & 3)	19	Shield (0 & 5)
4	Data 4 -	12	Data 3 -	20	Data 5 -
5	Data 4 +	13	Data 3 +	21	Data 5 +
6	Clock DDC	14	Power +5V	22	Shield Clock
7	Data DDC	15	Ground	23	Clock +
8	Analog Vertical Sync	16	Hot Plug	24	Clock -
C1	Analog Red				
C2	Analog Green				
C3	Analog Blue				
C4	Analog Horizontal Sync				
C5	Analog Ground				

TMDS
PLUG & PLAY
ANALOG

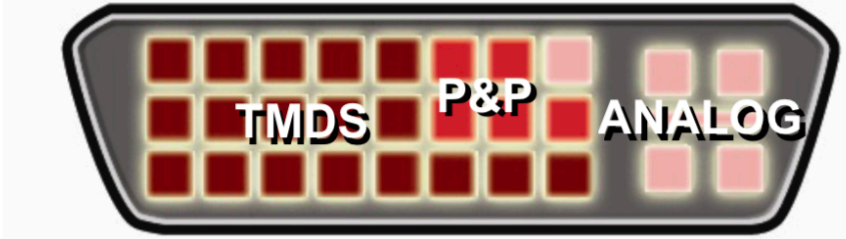


Figure 20: TMDS, Plug & Play and Analog Signals

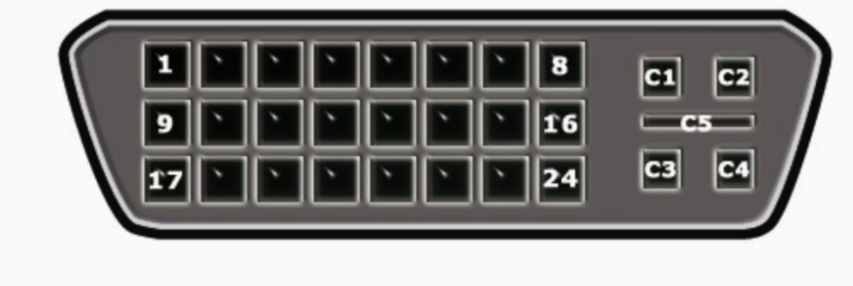


Figure 19: DVI-I Signal Pins

DVI pinout from [DVI and TMDS Extensions - Silicon Image White Paper]

HDMI is just DVI+

- 4 TMDS signals
- Display Data Channel (DDC) two way communication including HDCP signal
- CEC data line
- Hot Plug Detection (HPD)
- +5V power

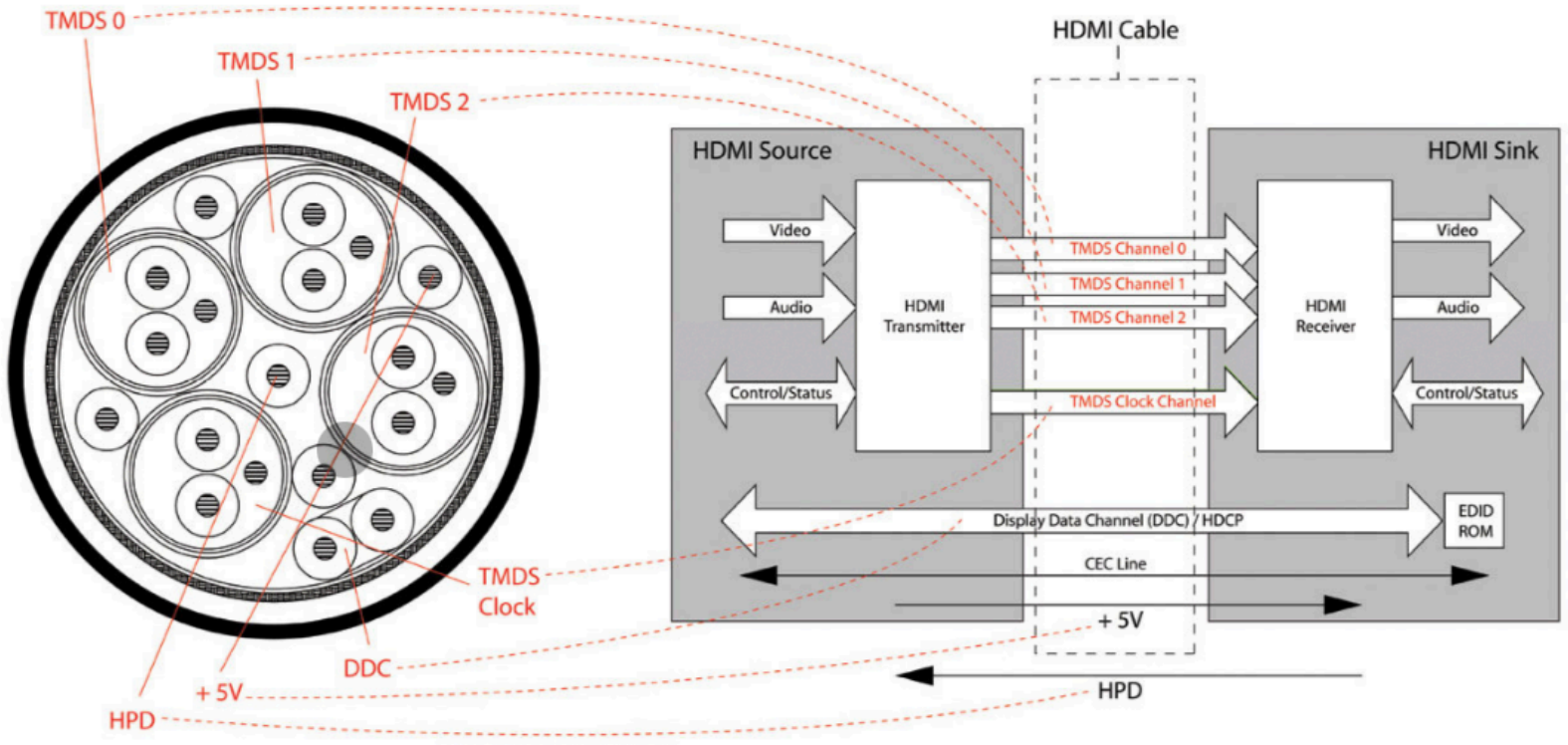


Fig.1 Components inside a HDMI Cable

Figure from [HDMI Demystified]

Summary

- VGA was one of the first major graphics display technologies developed but was optimal for analog displays like CRTs
- Digital displays like LCDs are better served by a new interface
  - Pixels are addressed in row-column array and time-multiplexed
  - Active displays enable each pixel's current value to be stored while others are being updated
- Digital Visual Interface (DVI) is a standard display technology for many devices today (HDMI is built on top of the key technology behind it)
  - Transition-minimized DC-balanced signaling (TMDS)

Resources and Further Reading

- HDMI from fpga4fun.com
  - DVI and TMDS Extensions - Silicon Image White Paper
  - HDMI Demystified
  - Digital Visual Interface DVI Rev. 1.0 from Digital Display Working Group
- HDMI Made Easy from Analog Devices

Lecture Feedback

- What is the most important thing you learned in class today?
- What point was most unclear from lecture today?

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