Lab 2: Physical Properties of Digital Circuits
E85 Spring 2016
Due: 2/3/16

Overview:
This lab explores the physical reality of digital circuits using discrete field effect transistors and gates. You will learn how to use an oscilloscope, breadboard and bench power supply. You will then study the physical characteristics of a transistor-based inverter. You will also study stable and unstable circuits based on inverters.

What to turn in:
1. Your answers to the questions in part A
2. Did you complete part B?
3. Your plots, tables and answers to part C

Feedback:
Let us know:
What went well in this assignment?
Were there points of confusion?
How long did you need to work on this assignment?
Part A – Physical digital circuits with transistors

(a) The specifications for a 45 nm node CMOS transistor are that they have a nominal drive current of 1 mA/µm². Assuming they are being supplied with a 1 volt power supply to achieve this condition, what is the channel resistance in the on state ($R_{on}$) of the transistor if its channel dimensions are 45 nm and 200 nm? Assume the off resistance is $10^6$ times higher. What is the value when the transistor is off ($R_{off}$)?

(b) The specifications for a 45 nm node CMOS transistor also specifies that the equivalent oxide thickness of the gate is 1 nm. Calculate the gate capacitance of the transistor with the same dimensions as in (a). You may assume the relative permittivity ($\varepsilon_r$) of silicon dioxide is 3.9. Look up the permittivity of free space if you do not know the value by heart.

The formula for the capacitance of a parallel plate capacitor is: $C = \frac{\varepsilon_r \varepsilon_0 A}{d}$

(c) Draw the CMOS transistor circuits corresponding to the following digital circuits:

(d) Assume input logical high occurs at 0.6 V. Assume that the voltage at node A is 0 V at $t = 0$. Redraw the circuits as an equivalent RC circuit to change the voltage at node B. Recall that capacitances in parallel add simply ($C_{total} = C_1 + C_2 + C_3 + \cdots$)

If A was driven instantly from 1 V to 0 V at $t = 0$, at what time will B become 0.6 volts for each circuit? This is the propagation delay of the inverter.

(e) If we needed to keep the propagation delay to less than 200 ps how many inverters can a single inverter drive? This number is called the fan out.
(2) Consider the following circuit, taking Vdd to be 2 V. Let the transistor turn on when: $|V_{gs}| > 0.4 \, V$.

Consider the 4 combinations of A and B at 0 and 2 V. What is the approximate voltage at Y for each? You justify your answer with equivalent resistive sketches for each. You may assume $R_{off}/R_{on} > 10^6$. 

Part B – Tutorial: Breadboards, Oscilloscopes and Power Supplies

In the E85 lab each workstation has a large solderless breadboard (see figure on next page).

Breadboards like these allow for the rapid construction of simple circuits that have extruded pins on a 0.1 inch pitch (pitch = the space between the pins). In the 70s and 80s the primary package for integrated circuits was the DIP (dual inline package). DIP packages and their variants plug directly into breadboards. Other through hole leaded packages also often work well with breadboards.

Increasingly electronics are only available in surface mount (SMD) packages only. These packages can be made compatible with a breadboard by the use of a small “breakout” PCB. Vendors like Adafruit and Sparkfun have many such boards available for common ICs of this type.

Breadboards are still useful because of their reusable nature. Their primary downside is they have large parasitic capacitances that preclude their use with signals over nominally 10 MHz. Breadboards are organized into rows and columns which are connected together. This allows the use of rows and columns on the breadboard as nodes in a circuit. The general configuration of a breadboard is shown below.

From left to right on the board:
- In the first section, all of the holes in the first column are connected together, as are all of the holes in the second column. These columns are normally used for power distribution.
- In the second section, each of the rows is connected across 5 columns of pins. The same configuration is used the third section of the board. Finally the forth section matches the first section. DIP chips are inserted so that one side of the packages’ pins are in column E and the other side of the packages’ pins are in column F.

The breadboard workstations in the lab have 3 of these modules. Each of the modules has a break in the vertically connected columns halfway down the board. In addition the workstations have long rows at the top of the area that are permanently connected to power supplies. Be careful not to wire the power supplies together using these rows.

Two of the power supplies are variable using the knobs at the top of the workstation, the other supply is fixed at 5V.

The power supplies are turned on by the large power switch at the top left of the breadboard workstation.

Source of breadboard layout image: [http://www.ece.utah.edu/eceCTools/_Outreach/_Outreach.htm](http://www.ece.utah.edu/eceCTools/_Outreach/_Outreach.htm)
The image above shows the E85 breadboard workstation. The blue box at the top shows the 4 rows which are connected horizontally to the 5V, +1.3-15V, -1.3-15V and GND power supply rails as noted by the white lines. The 12 yellow boxes show areas where columns are connected together. The 6 red boxes show where rows are connected together.

At most workstations in the lab you will find a bench triple power supply from Agilent or HP. There are also 4 oscilloscopes. Please share these between 2 workstations as you complete this lab.

The bench triple supply (above) has a variable output from 0-6 V and +/- 20 V. Each power rail is attached to a binding post on the front of the supply. While the voltage output is controlled by the rotary knob. The tracking ratio sets the ratio between the positive and negative supplies that are settable from 0-20 V.
Normally the tracking ratio is set so that the supplies track 1:1. The meter buttons change which supply is monitored with the panel readout.

The binding posts function in order are 6 V supply, common, +20 V supply, -20 V supply, and earth ground. The power supplies are *floating* so the one terminal of each voltage source is attached to common (COM) *not* earth ground. Only in limited circumstances should COM be tied to the earth ground.

The reason for this is something called a ground loop. Having more than one long path to the earth ground can create a large wire loop through which magnetic fields can create noise in a circuit.

An example of when you would connect the earth ground to COM is when you need to ground a metal enclosure to protect a user from an electrical shock hazard.

The oscilloscope is the most complex instrument in the lab. It measures voltage signals as a function of time. The scopes in the E85 lab have two channels.

An oscilloscope collects data when it is *triggered*. The source of the trigger event is selected using the *source* button in the *Trigger* section of the front panel, then selecting the source using the *buttons below the screen*. For this lab we will use *Line* (which is the AC 60 Hz line signal) and channel 1.

*Turn on the oscilloscope using the Line button.*

*Make sure channel 1 is displayed on the screen you should see a 1 marker at the right hand side if it is. If it is not press the 1 button and turn it on.*

*Set the oscilloscope to trigger off of “1”.*
Attach an oscilloscope probe to channel 1 and the reference pin as shown below:

You should see Run in the upper right of the screen. If you do not press the run button.

To change the vertical scale the Volts/Div knobs are used. There is one for each channel.

To change the horizontal scale use the Time/Div knob.

Adjust the voltage and time so that the display looks similar to the image above.

You can also shift a signal in time and voltage using the offset knobs position and delay. Finally you can add measurements both of voltage and time parameters using the measurement buttons at the top of the scope.

To practice using all the parts we will add a hex inverter to the breadboard, supply it with power and measure it using our power supply and scope.

You will find the hex inverters (7404) in the black cabinet in the E85 lab.

The pinout for these chips is show below:

The orientation of the chip can be determined from the U shaped indent at the top of the chip. We must supply 5 volts to Vcc and 0 volts to GND. Each inverter has an input A and an output Y.
The full datasheet for the hex inverter is here: http://www.ti.com/lit/ds/symlink/sn74ls04.pdf

We shall construct the following circuit using our hex inverter chip:

![Schematic of the hex inverter circuit](image)

In the schematic at the right and side the top port dot represents the center pin of the scope probe we used to look at the reference frequency with and the bottom pin is the alligator clip of the probe.

Use any value greater than 100 ohm and less than 1 Mohm for R1 (also found in the cabinet). This circuit transferred to the breadboard looks like this:

![Image of the breadboard setup](image)

Notice the use of wires on the scope probe. **Do not** insert the probe end into the breadboard. Wire is available in the cabinet as are wire strippers.

*Change the trigger on the scope to Line*

*Slowly vary the voltage on the 6 V rail between 0 and 5V and note when the output starts to become noisy/unstable and then when it becomes stable again at high or low.*

*Make note of these voltages in both “sweep” directions. Use the measure function on the scope to add a measurement of the average voltage of channel one. Record a few points to build up an IV transfer function of this inverter as discussed in class.*
Part C – Transistor inverter and n-inverter circuits

For this part of the lab you will need 2 hex inverter chips, 1 N-FET and 1 P-FET. The N-FET and P-FETs are located in bags in the cabinet. Please check writing on the transistors used matches the datasheets below in case they get returned to the wrong locations by mistake!

(1)

Remind yourself of the schematic of a CMOS inverter from class by drawing it and labeling the source, drain and gate of each transistor.

Referring to the following datasheets:

Build a CMOS inverter using 1 N-FET and 1 P-FET transistor. In similar manner to the tutorial add a resistor between input of the inverter and ground to help limit noise.

Starting at 0 volts slowly sweep the voltage on the input of the inverter noting the output voltage on the oscilloscope (you may find the voltage measurement functions useful). Record at least 20 input/output voltage points between 0 and 5 volts.

In what voltage range is the input logically low and logically high for this gate? What range should be forbidden as a logical input? Why?

(2)

Using your hex inverter chips, create the following circuit:

Set the Agilent bench power supply to 5V as noted in the schematic. Using a wire, briefly touch node A to node B then node C. What happens to the output that the oscilloscope is probing? Is the output stable when you are not touching A to either B or C? What could this circuit be used for?
(3)

Change the triggering on the oscilloscope to trigger off channel 1 and create the following circuits:

Use the scope to probe output of the first inverter in each circuit. Adjust the time base and trigger level until you see an oscillating waveform. A trigger level around 1 V should work for most people.

Use the measurement function of the scope, measure the period of each circuit and record the results in a table.

Plot the period you measured vs the number of gates. What is the propagation delay for a single inverter?

Look at the datasheet for the hex inverter. Does it match (see: switching characteristics)? If it does not is it reasonable? Why?