Errata

Title & Document Type: 8753A Network Analyzer On-Site Service Manual

Manual Part Number: 08753-90022

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement business is now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual provides the best information we could find. It may be incomplete or contain dated information, and the scan quality may not be ideal. If we find a better copy in the future, we will add it to the Agilent website.

Support for Your Product

Agilent no longer sells or supports this product. You will find any other available product information on the Agilent Test & Measurement website: www.tm.agilent.com.

Search for the model number of this product, and the resulting product page will guide you to any available information. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available.

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HP 8753A
NETWORK ANALYZER

SERIAL NUMBERS

This manual applies directly to any HP 8753A network analyzer having a serial number prefixed 2543A or 2606A.

For additional information about serial numbers, refer to INSTRUMENTS COVERED BY MANUAL in the General Information section of the Operating and Programming Manual.

MANUAL PART NO. 08753-90022
Microfiche Part Number 08753-90023

Printed: JUNE 1986

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CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of delivery. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation. This product has been designed and tested in accordance with international standards.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with his symbol when it is necessary for the user to refer to the instruction manual (refer to Table of Contents).

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

BEFORE APPLYING POWER

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer make sure the common terminal is connected to the neutral (grounded side of the mains supply).

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from their power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

HP 8753A On-Site System Service Manual
TABLE OF CONTENTS

General Introduction

INTRODUCTION

This Hewlett-Packard 8753A Network Analyzer On-Site System Service Manual contains information to verify, adjust, and service the HP 8753A network analyzer. It is part of a three manual set, which also includes the System Operating and Programming Manual and the Test Sets and Accessories Manual.

The System Operating and Programming Manual contains instructions for setting up and operating the HP 8753A with related test sets and accessories. The Test Sets and Accessories Manual binder is provided to hold the manuals supplied with the test sets and measurement accessories.

ON-SITE SYSTEM SERVICE MANUAL

This On-Site System Service Manual is divided into sections that provide the following information:

- GENERAL INTRODUCTION is a brief outline of the On-Site Service Manual, with cross-references to the information in the Operating and Programming Manual and the Test Sets and Accessories Manual.
- SYSTEM VERIFICATION provides a procedure to verify system-level error-corrected measurement performance of the HP 8753A with a test set. Known traceable standards, available in the HP 85029A verification kit, are measured and compared with recorded data that is supplied with this kit on a disc. The procedure is automated and is contained in firmware internal to the HP 8753A. Therefore, an external controller is not required. A disc drive is required.
- PERFORMANCE TESTS provides procedures to verify that the performance of the HP 8753A is in accordance with the individual specifications listed in the HP 8753A Operating and Programming Manual. Performance tests for the test sets are in their individual operating and service manuals. Each of the performance tests provides traceability through calibrated standards and test equipment. Some tests are semi-automated and require the use of an external controller. The test software is supplied on a 3.5 inch disc with a single-sided format, packaged inside the manual. The entire sequence of performance tests takes about four hours to run, not including instrument warm-up time.
- ADJUSTMENTS AND CORRECTION CONSTANTS provides instructions for correct adjustment and alignment of the instrument after repair or replacement of an assembly. Procedures are given for reloading correction constants after replacement of one or more specified assemblies. Software for these semi-automated adjustment procedures is provided on disc with the performance test software.
- REPLACEABLE PARTS provides part numbers and illustrations of the HP 8753A replaceable assemblies and miscellaneous chassis parts, together with ordering information.
- MANUAL BACKDATING contains backdating information required to make this manual compatible with earlier shipment configurations of the instrument.

- SERVICE explains how to troubleshoot and repair the HP 8753A to the assembly level. It provides procedures to isolate a problem to the defective assembly.

SYSTEM OPERATING AND PROGRAMMING MANUAL

This manual consists of separate documents which provide the following information:

- GENERAL INFORMATION AND SPECIFICATIONS provides a description of the instrument, options, test sets, and accessories. Also included are tables of instrument specifications and supplemental performance characteristics, and information to determine expected system performance after accuracy enhancement.
- SYSTEM INSTALLATION provides information for site preparation and installation.
- OPERATOR'S CHECK is a brief procedure that provides reasonable confidence that the instrument or system is functional.
- USER'S GUIDE is a step-by-step tutorial guide for making measurements with the HP 8753A using front panel controls.
- HP-IB INTRODUCTORY OPERATING GUIDE describes remote operation of the HP 8753A with an HP 9000 series 200 or 300 computer as a controller.
- SAMPLE MEASUREMENTS PROGRAM is a typical measurement program intended for use in developing programs specific to user needs.
- HP-IB QUICK REFERENCE GUIDE is a reference synopsis for remote operation of the HP 8753A with a controller.
- OPERATING AND PROGRAMMING REFERENCE is a complete reference for both local and remote operation of the HP 8753A, organized functionally.
- QUICK OPERATING GUIDE, packaged separately, is a pocket-sized reference book that contains brief information on the softkey menus and manual operation.

TEST SETS AND ACCESSORIES MANUAL

The HP 8753A Test Sets and Accessories Manual is a binder provided for the storage and organization of the manuals that are shipped with the accessory products. This binder is shipped empty except for divider tabs, instructions, and a connector care manual.

The connector care manual describes all types of connectors used in HP 8753A measurement accessories, and documents the considerations specific to each connector.

REQUIRED TEST EQUIPMENT AND TOOLS

Table 1 lists the equipment necessary to test, troubleshoot, or adjust the HP 8753A. This table lists the equipment required, the recommended HP model, critical specifications, and the procedures that require the equipment.

Note that there are three different ways to test the performance of your HP 8753A. These are Performance Tests, System Verification, and Operator's Check. The equipment required depends on which of these three you choose to use to test your system. Refer to the individual procedures for information about each of these (the Operator's Check is in the Operating and Programming Manual).

In addition to test equipment listed in Table 1, the following tools are also required:

- #1 and #2 Pozidriv screwdrivers.
- Flat-blade screwdrivers — small, medium, and large.
- 5/16 inch open-end wrench (for SMA nuts).
- 3/16 inch and 5/16 inch hex nut drivers.
- Non-conductive and non-ferrous adjustment tool.
- Needle-nose pliers.
- Tweezers.
- Anti-static work mat with wrist-strap.

Table 1. Service Test Equipment (1 of 2)

INSTRUMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL	USE*
Series 200/300 Controller (mass storage as needed)	No substitute	HP 216, 226, 236, 220, 217, 310	P, A
BASIC 3.0 or 4.0 Operating System	No substitute	HP 98613A	P, A
Printer	Raster graphics capability	HP 2225A, 9876A, 2671G, 82906A	P, SV
Spectrum Analyzer	No substitute	HP 8566A/B	P, A
Frequency Counter	Frequency: 300 kHz-3 GHz Accuracy: 1 ppm	HP 5386A, 5342A, 5343A	P, A
Transmission/Reflection Test Set	Frequency: 300 kHz-3 GHz Directivity: 30 dB	HP 85044A	P
Power Meter (HP-IB)	No substitute	HP 436A, 438A	P, A, T
Power Sensor	Frequency: 300 kHz-3 GHz	HP 8482A	P, A,T
Power Splitters: Two-way (2)	Frequency: 300 kHz-3 GHz Tracking between outputs: ±0.5 dB Output SWR: ± 1.1 dB	HP 11667A Opt 001	OC,P,A,T
Three-way	Frequency: 300 kHz-3 GHz Tracking between outputs: ±.25 dB Output SWR: ±1.1 dB	HP 11850C	P
100 dB Step Attenuator	No substitute	HP 8496A/G[1]	P
Attenuator/Switch Driver	No substitute	HP 11713A[1]	P
Type-N Calibration Kit	No substitute	HP 85032B	P
Type-N 50 Ohm Termination (3)	No substitute	HP 908A	P
Fixed Attenuators: 3 dB 10 dB 20 dB (2) 30 dB	Return loss: >32 dB Type N Type N Type N Type N	 HP 8491A Opt. 003 HP 8491A Opt. 010 HP 8491A Opt. 020 HP 8491A Opt. 030	 P P, A P, A P

Table 1. Service Test Equipment (2 of 2)

INSTRUMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL	USE*
RF Cable Set	No substitute	HP 11851B	P, A, OC, T
RF Cables (2)	12″ Phase matched	HP 11500B	A
HP-IB Cables (5 max.)		HP 10833A/B/D	P, A, SV
Oscilloscope	Bandwidth: 100 MHz	any	A, T
DVM	Resolution: 10 mv	any	A
Coaxial Filter		HP 360B	A
Tool Kit	No substitute	HP part number 08753-60023	A, T
Verification Kit	No substitute	HP 85029A	SV
7 mm Calibration Kit	No substitute	HP 85031B	SV
7 mm Test Port Return Cables	No substitute	HP 11857D	SV, P
Disc Drive	CS80 protocol - SV only	HP 9122S/D	SV, P
Signature Multimeter		HP 5005B	A, T

* **SV** – System Verification
OC – Operator's Check
P – Performance Tests
A – Adjustment
T – Troubleshooting

1 The performance test procedure uses the HP 8496G programmable attenuator with the HP 11713A attenuator driver, or the HP 8496A manual attenuator.

HP 8753A
NETWORK ANALYZER

System Verification

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System Verification

INTRODUCTION

System verification is a procedure used to verify the *system-level error-corrected uncertainty limits* for the HP 8753A with the HP 85046A S-parameter test set.

The verification procedure is automated and is contained in the firmware internal to the HP 8753A. The procedure involves first calibrating the HP 8753A, then measuring a set of verification devices (supplied in the HP 85029A 7 mm Verification Kit) at specific frequencies and comparing the measured data to the traceable data and uncertainty limits supplied with the kit on a disc. The difference between the measured data and the supplied traceable data of the devices must fall within the uncertainty limits at *all* frequencies to pass the system verification. If this procedure is performed by a Hewlett-Packard Customer Engineer, and the system passes the verification at all frequencies, a Certificate of Traceability and a system verification sticker is issued.

Keep in mind that the system verification verifies *system-level* uncertainty limits, not *instrument-level* specifications. The individual instrument-level specifications of the HP 8753A and the test set can be verified using the procedures in the Performance Tests section in this manual and in the test set manual. Instrument-level specifications for the HP 8753A are listed in the General Information and Specifications section of the Operating and Programming Manual. Test set specifications are listed in the specific test set manual.

Another method available for testing the performance of your HP 8753A is the Operator's Check in the Operating and Programming manual. The Operator's check verifies that the circuits in the HP 8753A are functioning properly. However, it does not verify the test set or other HP 8753A accessories. It also does not verify the specifications.

SYSTEM VERIFICATION CYCLE AND KIT RE-CERTIFICATION

The recommended system verification cycle is every six months. It is also recommended that the verification kit be re-certified annually. For more information about kit re-certification, refer to the HP 85029A 7 mm Verification Kit Manual.

MEASUREMENT UNCERTAINTY

Associated with any network analyzer are measurement errors that add an uncertainty to the measured results. This uncertainty defines how accurately a device under test (DUT) can be measured.

The accuracy enhancement procedure, also called measurement calibration, measures and removes the systematic (repeatable) errors. This is accomplished by measuring a set of calibration devices with known characteristics. However, residual systematic errors remain after accuracy enhancement

primarily due to the limitations of how accurately the electrical characteristics of the calibration devices can be defined and determined. Also, there are other errors, known as *random* (non-repeatable) errors, that cannot be quantified and measured. The residual systematic errors along with the random errors continue to affect measurements after accuracy enhancement, adding a total uncertainty to the measurement results.

The measurement uncertainty is defined to be the sum of the residual systematic (repeatable) and random (non-repeatable) errors in the measurement system after accuracy enhancement. Systematic errors include directivity, source match, load match, reflection and transmission tracking, and isolation (crosstalk). Random errors include errors due to noise, drift, connector repeatability, and test cable stability. A complete description of the errors and how they affect measurements is provided in the Operating and Programming Reference Manual under "Accuracy Enhancement Fundamentals" in Chapter 5 — Measurement Calibration.

Measurement uncertainties of any HP 8753A system also depend upon the characteristics of the device under test. Expected measurement uncertainty of your HP 8753A system when measuring any device under test can be determined by using the equations provided in the "General Information and Specifications" section of the Operating and Programming Manual. The specifications section also provides a system error model (flow graph) that shows the relationship of the systematic and random errors. This is useful for predicting overall measurement performance.

The measurement uncertainty limits for system verification are the sum of the worst-case uncertainties associated with measuring the verification devices on the factory HP 8753A system *plus* the worst-case uncertainties associated with measuring these same devices on the system being verified.

EQUIPMENT

The system verification procedure verifies the minimum HP 8753A system, which includes the following instruments and accessories:

- HP 8753A Network Analyzer (with or without options)
- HP 85046A 50 ohm test set
- HP 85031B 7 mm Calibration Kit
- HP 11857D 7 mm Test Port Return Cables (used with the HP 85046A test set)

NOTE: Additional equipment or accessories used with the above system are not verified by system verification.

The following equipment and accessories are required to verify the HP 8753A system:

- HP 85029A 7 mm Verification Kit
- Disc drive (see Table 1 in the Introduction section for recommended HP models).
- Graphics printer (see Table 1 in the Introduction section for recommended HP models).
- HP-IB cables

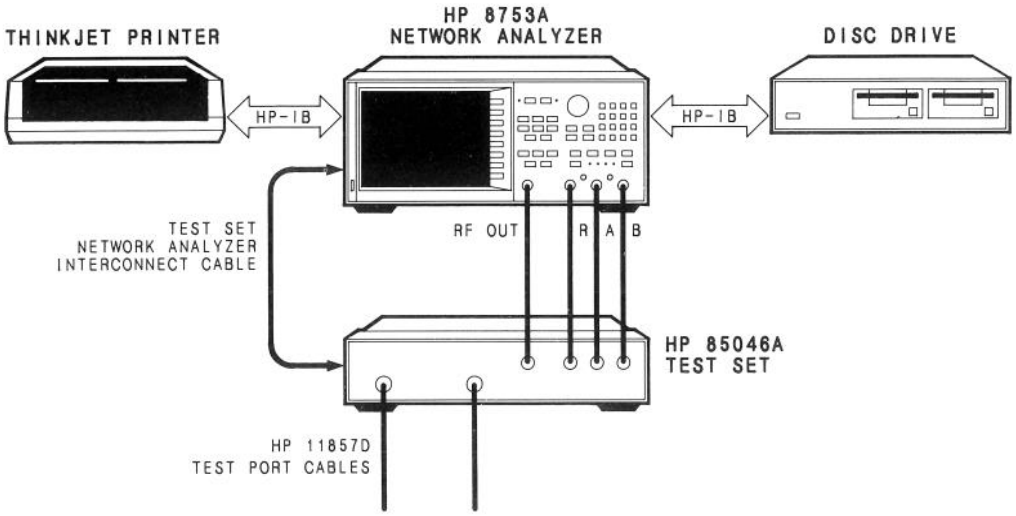

Figure 1. System Verification Setup.

PROCEDURE

1. Connect the HP 8753A system as shown in Figure 1.
2. Insert the verification disc (supplied in the HP 85029A verification kit) into disc drive 0 (left drive).
3. Allow the system to warm up for 1 hour.
4. Review the Microwave Connector Care Manual supplied in the Test Sets and Accessories Manual for proper care and connection techniques of microwave connectors. Proper connections and clean, undamaged connectors are critical for accurate measurement results.

   NOTE: When cleaning and inspecting the open calibration device, you may notice a metal shim between the dielectric and the inner wall of the outer conductor. This is normal — do not try to remove it.

Initialization

5. Press **[PRESET]**, then **[LOCAL] [SYSTEM CONTROLLER]**. This allows the HP 8753A to control the bus. No other controller should be connected to the bus.
6. The default unit number for the disc is 0. If necessary, press **[DISC UNIT NUMBER]** and change to the appropriate setting. The default HP-IB address of the disc is 0; the printer address is 1. If necessary, press **[SET ADDRESSES]** and change these settings to reflect the actual addresses of these devices.
7. If a printout of *all* verification data for *all* devices is required, press **[SYSTEM] [SERVICE MENU] [TEST OPTIONS] [RECORD ON]**. All results will be printed. Note that if this record function is turned ON now, it cannot be turned off during the verification procedure. (Make sure the paper in the printer is set up so that printing starts at the top of the page.)

   If a printout of data for only a particular verification device(s) is desired, go to the next step; the record function will be turned on later in the verification procedure.

8. Press **[SYSTEM] [SERVICE MENU] [TESTS] [SYS VER TESTS]**. The message "TEST 27 Sys Ver Init −ND−", will be displayed. The "−ND−" indicates the test status. A listing of the test status codes that may appear during this procedure is available in Table 1 below. If the record function is ON, "/REC" will also be displayed.

Table 1. Listing of Test Status Codes

Test Status Code	Meaning of Code
PASS	Pass
FAIL	Fail
(NA)	Not Available
−ND−	Not Done
−IP−	In Progress
DONE	Done

9. Press **[EXECUTE TEST]**. This recalls the instrument state file from the disc and sets up the HP 8753A for a measurement calibration. When it's done initializing, "TEST 27 Sys Ver Init DONE" will be displayed.

Measurement Calibration

The following Measurement calibration procedure measures and removes the systematic errors present in the HP 8753A system. This involves measuring a set of calibration devices, supplied in the HP 85031B 7 mm Calibration Kit, with known electrical characteristics. Following the calibration, the verification procedure will verify that the sum of the *residual* errors (present after calibration) are within the specified uncertainty limits. The measurement calibration *must* be performed before continuing on to the system verification.

NOTE: Calibration and verification data is taken at the following frequencies (MHz): .300, 30, 100, 250, 500, 750, 1000, 1250, 1500, 1750, 2000, 2250, 2500, 2750, 3000.

10. Press **[CAL] [CALIBRATE MENU] [FULL 2-PORT] [ISOLATION]**.

11. Connect the load (supplied in the HP 85031B Calibration kit) to the port 1 cable, and the other load to the port 2 cable.

12. Press **[FWD ISOL'N/ISOL'N STD]**.

    NOTE: Measurements are complete when the instrument beeps and the softkey that was pressed is underlined. Also, note that while the calibration device data is being taken, the trace shifts; this is normal.

13. When the measurement is complete, press **[REV ISOL'N/ISOL'N STD]**.

14. When the measurement is complete, press **[ISOLATION DONE]**.

15. Press **[REFLECT'N]**, then **[S22: LOAD]**.

16. When the measurement is complete, disconnect the port 2 load.

17. Connect the "short" end of the short/open calibrator device (supplied in the HP 85031B Calibration Kit) to the port 2 cable.

18. Press **[S22: SHORT]**.

19. When the measurement is complete, disconnect the short. Connect the "open" end of the calibrator device to the port 2 cable.
20. Press **[S22: OPEN]**.
21. When the measurement is complete, disconnect the device.
22. Press **[S11: LOAD]**.
23. When the measurement is complete, disconnect the load from the port 1 cable, then connect the "short" end of the calibrator device to the port 1 cable.
24. Press **[S11: SHORT]**.
25. When the measurement is complete, disconnect the short, then connect the "open" end of the device to the port 1 cable.
26. Press **[S11: OPEN]**.
27. When the measurement is complete, disconnect the open from the port 1 cable.
28. Press **[REFLECT'N DONE]**.
29. Press **[TRANSMISSION]**.
30. Connect the two test port return cables together to form a "thru" configuration.
31. Press the **[FWD.TRANS.THRU]** softkey.
32. When the measurement is complete, press **[FWD.MATCH.THRU]**.
33. Continue with the **[REV.TRANS.THRU]** and **[REV.MATCH.THRU]** measurements.
34. Press **[TRANS.DONE]**.
35. Press **[DONE 2-PORT CAL]**.
36. The **[SAVE]** softkey menu will automatically be displayed. Save the calibration in any register.
37. Calibration is now complete.

System Verification

The following verification procedure is automated. The program is contained in the HP 8753A firmware and therefore does not require an external controller. For each verification device the HP 8753A reads a file from the verification disc and sequentially measures the magnitude and phase for all four S-parameters. The three verification devices are: 20 dB coaxial attenuator, 50 dB coaxial attenuator, mismatch attenuator. The mismatch attenuator is measured twice; once with its "A" end connected to port 1, and once with its "A" end connected to port 2. The ends are marked on the device.

The test number and device number for each verification device is as follows:

Verification Device	Test Number	Device Number
20 dB attenuator	28	1
50 dB attenuator	29	2
mismatch attenuator ("A" end on port 1)	30	3
mismatch attenuator ("A" end on port 2)	31	4

38. Press **[SYSTEM] [SERVICE MENU] [TESTS] [28] [X1].**

39. In the active entry area on the CRT, the following will be displayed:

    "TEST 28 Ver Dev 1"

40. If the Record function was turned ON in step 7, or if a printout is not desired, go to the next step.

    If a printout of the data for this device is desired, press **[SYSTEM] [SERVICE MENU] [TEST OPTIONS] [RECORD ON] [SYSTEM] [SERVICE MENU] [TESTS].** Make sure the paper in the printer is set up so that printing starts at the top of the page.

41. Press **[EXECUTE TEST].**

42. When prompted, connect the 20 dB attenuator verification device as shown in Figure 2.

    NOTE: When measuring the 20 and 50 dB attenuators, connect the "A" end of the device to the port 1 cable. With the device label facing the user, the "A" end is on the left.

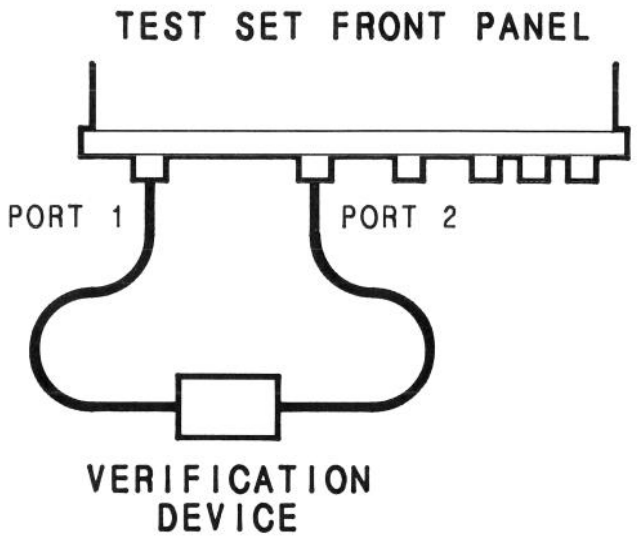

Figure 2. Setup For Verification Measurement.

43. Press **[CONTINUE]**. The tests will begin.

44. If the record function is OFF (printout is not required), the program will pause after each S-parameter measurement and you will need to press **[CONTINUE]** after each measurement. (There are eight measurements for each device — magnitude and phase for four S-parameters.)

    NOTE: Note that S-parameter measurements that are not useful for system verification will not display PASS/FAIL information. If a measurement fails, note which device and S-parameter failed and continue on with the remaining tests. Then go to the In Case of Failure procedure at the end of this section.

    Also note that both the measured data and the factory data are displayed on the CRT.

    If the record function is ON, the program will measure all S-parameters without pausing after each measurement. Note that only S-parameter measurements that are useful for system verification will be printed. While it is printing, a listing of the measured data will be displayed on the CRT.

45. When all tests are complete, the TESTS softkey menu will appear. Disconnect the verification device.

46. Enter Test 29 (using step keys, entry keys, or RPG). Repeat steps 40 through 45 using the 50 dB attenuator verification device.

47. Enter Test 30 (using step keys, entry keys, or RPG). Repeat steps 40 through 45 using the mismatch attenuator — with the "A" end connected to the port 1 cable.

48. Enter Test 31 (using step keys, entry keys, or RPG). Repeat steps 40 through 45 using the mismatch attenuator. Connect the "A" end to the port 2 cable.

49. The measurement printouts show both a plot of the measurement and a list of the measured frequencies with corresponding data. The plot includes both the measured data trace and the supplied factory data trace. The listing includes only the measured data. If there is a failure at any frequency, an asterisk will be next to the measured data and the out-of-specification measured data on the plot will be blanked out.

IN CASE OF FAILURE

If the system fails the verification at any frequency, perform the following simple checks to help determine the cause of failure. If the system fails to execute the initialization, check that it is in the SYSTEM CONTROLLER mode (press **[LOCAL]**), then start over (from step 5).

1. Check all connections and connectors (but do not disconnect the cables from the test port; doing so will invalidate the calibration). The connectors on the cables and the verification devices should be clean and properly gaged. Connections should be properly torqued. Refer to the Microwave Connector Care Manual (in the Test Sets and Accessories binder) for complete information about connector care and making connections. After checking the connectors and connections, press **[PRESET]**, then recall the calibration (press **[RECALL]**, then the softkey corresponding to the register that you saved it in). Repeat the test.

2. Check the three input power levels (R, A, and B) as follows:

   a. Press **[PRESET]**.

   a. Disconnect the verification device.

   b. Press **[MEAS] [Refl: FWD S11 A/R] [INPUT PORTS] [A]**. Typically, the beginning of the trace should be at about −19 dB (± 2 or 3 dB) and the end should at about −24 dB (± 2 or 3 dB). The trace will have some ripple, but there should be no large variations (e.g. power holes).

   c. Press **[R]**. The trace should be similar to input A.

   d. Press **[S PARAMETERS] [Refl: REV S22 B/R] [INPUT PORTS] [B]**. The trace should be similar to inputs A and R.

   e. If any one of the port traces are not at the correct power levels, or if there are any power holes, this indicates a possible problem in the test set or the HP 8753A receiver. If all three inputs are bad, it is more likely that it is a problem with the HP 8753A source.

3. Check the calibration as follows:

   a. Recall the calibration: press **[RECALL]**, then the softkey corresponding to the register that you saved it in.

   b. Connect the short to the port 1 cable.

   c. Press **[MEAS] [Refl: FWD S11 A/R]**. Set scale to .05 dB/div.

   d. Trace should be 0.00 dB ± 0.05 dB.

   e. Press **[FORMAT] [PHASE] [SCALE REF] [PHASE OFFSET] [10] [x1] [REFERENCE VALUE] [170] [x1]**. Set scale to 0.4 deg/div.

   f. Trace should be 0.0 deg ± 0.4 deg.

   g. Disconnect the short. Connect the cables together.

   h. Press **[FORMAT] [LOG MAG] [MEAS] [Trans: FWD S21 B/R]**. Set scale to .05 dB/div. Trace should be 0.00 dB ± 0.05 dB.

   If any of the traces are out of the limits given, repeat the calibration, then repeat the verification test.

4. Printout the error terms. Refer to "Error Term Troubleshooting" in the Troubleshooting Reference section for instructions and descriptions of the terms. Compare the E-term printout data with the uncorrected data listed in the tables of expected system performance under "System Performance" in the General Information and Specifications section of the operating manual.

5. Refer to Service section.

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Performance Tests

INTRODUCTION

This section consists of step-by-step tests that confirm certain performance specifications of the HP 8753A network analyzer. Performance tests are provided for all specifications that are coded S-1 in the table of HP 8753A instrument specifications in the General Information and Specifications section of the Operating and Programming Manual. All tests may be performed without removing the instrument covers.

Performance tests are arranged for convenience, with the least time-consuming tests placed first and those requiring longer times placed last. However, tests may be performed singly, or in any order desired. Approximately four hours is required to complete all performance tests, not including instrument warm-up time. Allow the HP 8753A to warm up for one hour before starting any performance test.

Table 1 lists all performance tests.

Table 1. Performance Tests

Manual Performance Tests	Automated Tests
Frequency Range and Accuracy Minimum R Level Receiver Noise Level Input Crosstalk Trace Noise Frequency Response Absolute Amplitude Accuracy Input Impedance	Output Power Spectral Purity Dynamic Accuracy

MANUAL AND AUTOMATED PERFORMANCE TESTS

Some performance tests are to be done manually, and some are automated and require a controller. All manual and automated tests must be performed to completely verify instrument performance. There are no manual equivalents to the automated tests.

The use of automation reduces the time and effort required to perform otherwise tedious or time-consuming measurements. Appropriate performance tests are automated, and grouped together for convenience.

The test software is supplied on 3.5 inch disc with single-sided format and packaged inside this manual.

It is recommended that HP 8753A internal tests (self test) be run before the performance tests are started. These quick, automated internal checks may save time by indicating an instrument fault before time is invested doing performance tests. Internal tests are described in the Troubleshooting Reference section of this manual.

The table of recommended test equipment in the General Introduction section of this On-Site System Service Manual lists the equipment needed to perform all manual and automated performance tests. Equipment lists for individual tests are provided in each performance test.

Some tests require common RF adapters that are not shown or listed. Adapters are called out when they are used in unique setups. In many test setups, an asterisk (*) is shown next to RF paths between connectors that are to be directly connected without using a cable.

CALIBRATION CYCLE

It is recommended that the HP 8753A network analyzer be calibrated at least once every year.

PERFORMANCE TEST RECORD

The Performance Test Record at the end of this section is provided to record the values measured in each of the manual performance tests. The record for all automated tests is generated by a printer during those tests.

IN CASE OF DIFFICULTY

If a particular manual or automated performance test fails, refer to the "In Case of Difficulty" paragraph at the end of the procedure for that test. This provides troubleshooting hints or references to other manual sections to help resolve the problem.

After any performance test failure, it is recommended that the system-level troubleshooting procedures be followed. Make sure that the test equipment used in each test conforms to its own published specifications and that all connectors are clean. Refer to the Microwave Connector Care Manual having HP part number 08510-90064 for specific information on the use, cleaning, mating, and gaging of type-N connectors, as well as precision 7mm, SMA, and precision 3.5mm connectors.

The table of Related Service Procedures located in the Troubleshooting Reference of this manual shows which performance tests and adjustments are interactive. Use it to determine which other performance tests, if any, need to be done after adjustment or repair of the instrument.

Manual Performance Tests

Frequency Range and Accuracy

SPECIFICATIONS

Frequency Range: 300 kHz to 3 GHz ± frequency accuracy
Frequency Accuracy: ± 10 ppm (25°C ± 5°C)

DESCRIPTION

In this test, the frequency accuracy of the HP 8753A is measured over its entire frequency range. Frequencies in each of the analyzer's eleven internal sub-bands are checked due to its harmonic mixing scheme.

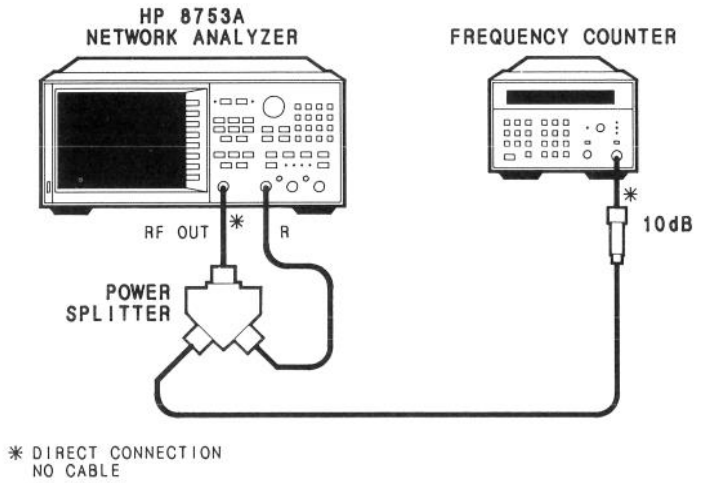


Figure 1. Frequency Range and Accuracy Test Setup

EQUIPMENT

Frequency Counter	HP 5343A
50Ω Power Splitter	HP 11667A Option 001
10 dB Attenuator	HP 8491A Option 010
RF Cable	Part of the HP 11851B Cable Set

PROCEDURE

1. Connect the equipment as shown in Figure 1.
2. On the HP 8753A, press **[PRESET]**.
3. Press **[MENU] [CW FREQ] [3] [0] [0] [k/m]** to select a CW frequency of 300 kHz. The counter reading should display 300 kHz ± 3 Hz (299.997 kHz to 300.003 kHz).

   Record the measured frequency on the Performance Test Record located at the end of the Manual Performance Tests section.
4. Repeat step 3 for each of the frequency settings listed in the Performance Test Record. The tolerance and measurement window are different for each frequency selected.

IN CASE OF DIFFICULTY

If any frequency measured is close to specification limits (either in or out of specification), check the time base accuracy of the counter used.

If the analyzer fails by a significant margin at all frequencies, the master time base probably needs adjustment. In this case, refer to the frequency accuracy adjustment in the Adjustments section of this manual.

Two adjustments are related to this performance test. They are the frequency accuracy adjustment and the fractional-N frequency range adjustment. Refer to the Source Functional Group portion of the Service section for related troubleshooting information.

Minimum R Level

SPECIFICATIONS

Minimum R Level: −35 dBm

DESCRIPTION

Source phase lock is achieved by sampling power at the R input. The phase detection circuitry must receive sufficient power from input R for proper source operation.

As R input power is decreased, the signal-to-noise ratio in the phase-locked loop decreases. This phase-locked loop noise is translated into spectral noise at the RF output and is ultimately observed as noise in the receiver.

In this test, R input trace variation is measured with the phase lock power level at −35 dBm. Four frequency ranges are tested in order to exercise phase lock circuitry in different internal bands. Trace math (DATA/MEMORY) is used to eliminate frequency response errors in the test setup.

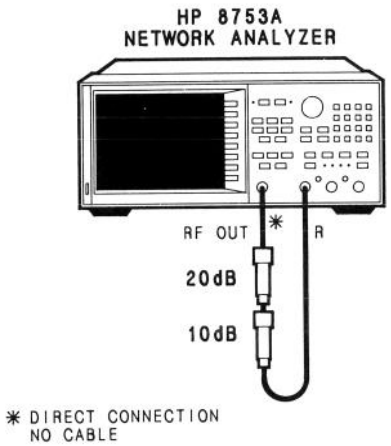


Figure 2. Phase Lock Sensitivity Test Setup

EQUIPMENT

10 dB Attenuator	HP 8491A Option 010
20 dB Attenuator	HP 8491A Option 020
RF Cable	Part of the HP 11851B Cable Set

PROCEDURE

1. Connect the equipment as shown in Figure 2.
2. Press **[PRESET]**.
3. Press **[MEAS] [R]** to select R magnitude.
4. Press **[MKR FCTN] [STATS ON]** to display marker statistics.
5. Press **[MKR SEARCH ON] [TRACKING ON] [SEARCH: MAX]** to select continuous marker tracking of the peak signal.
6. Press **[MENU] [NUMBER OF POINTS] [8] [0] [1] [x1]** to select 801 data points.
7. Press **[POWER] [-] [6] [x1]** to set the power level into R to approximately −36 dBm to ensure that power across the band is < −35 dBm.
8. The marker 1 power level readout in the upper right-hand corner of the display should not not be greater than −36 dBm. If the power level exceeds −36 dBm, press **[▼]** to decrease the power level by 1 dB and repeat this step.

   Note the source power reading in the active entry area (upper left-hand side of the display).
9. Press **[STOP] [3] [.] [3] [M/u]** to set the stop frequency to 3.3 MHz.
10. Press **[MENU] [POWER] [1] [4] [x1]** to set the power level into R input to approximately −16 dBm.
11. Press **[DISPLAY] [DATA → MEMORY]** to store the data into memory.
12. Press **[DATA/MEMORY]** to display data/memory.
13. Press **[MENU] [POWER]**, enter by keypad the power level noted earlier in step 8, and press **[x1]**.
14. Observe the peak-to-peak (p-p) marker statistic in the upper right-hand corner of the display. If the reading is less than 1 dB, record "passed" in the appropriate place on the Performance Test Record located at the end of the Manual Performance Tests section.

    Press **[DISPLAY] [DISPLAY DATA]** to view the measured data.
15. Press **[START] [3] [.] [3] [M/u]** to set the start frequency to 3.3 MHz.
16. Press **[STOP] [4] [.] [3] [M/u]** to set the stop frequency to 4.3 MHz.
17. Repeat steps 10 through 14 for the new frequency range.
18. Press **[START] [4] [.] [3] [M/u]** to set the start frequency to 4.3 MHz.
19. Press **[STOP] [1] [5] [.] [9] [9] [9] [9] [9] [9]** to set the stop frequency to 15.999999 MHz.
20. Repeat steps 10 through 14 for the new frequency range.
21. Press **[START] [1] [6] [M/u]** to set the start frequency to 16 MHz.
22. Press **[STOP] [3] [G/n]** to set the stop frequency to 3 GHz.
23. Repeat steps 10 through 14 for the new frequency range.

IN CASE OF DIFFICULTY

Remove the instrument top cover and check flexible RF cable W8 connected between R sampler assembly A4 and phase lock assembly A11. Make sure the main body of this cable is on top of the sampler assemblies and not positioned next to phase lock assembly A11.

Use the A sampler assembly as the phase lock loop sampler in place of the R sampler assembly. Do this by removing flexible RF cable W8 at the R sampler assembly A4 connector and attaching it to the similar connector on A sampler assembly A5. Disconnect the 10 dB attenuator from input R and connect it to input A. Repeat the test, but press **[MEAS] [A]** in step 3. If the test passes, R sampler assembly A4 is bad.

Suspect possible failure of the A11 phase lock assembly.

The high/low band transition adjustment is related to this performance test. Refer to the Source Functional Group portion of the Service section for related troubleshooting information.

Receiver Noise Level

SPECIFICATIONS

Noise Level (Inputs A, B): −90 dBm (3 kHz IF bandwidth)
−100 dBm (10 Hz IF bandwidth)

DESCRIPTION

In this test, receiver noise level (noise floor) is determined by connecting 50 ohm terminations to the A and B inputs, and measuring the mean trace value in linear magnitude format. This noise level ultimately limits the sensitivity of the receiver.

Input R must be > −35 dBm for phase locking the source and is not tested for receiver noise level.

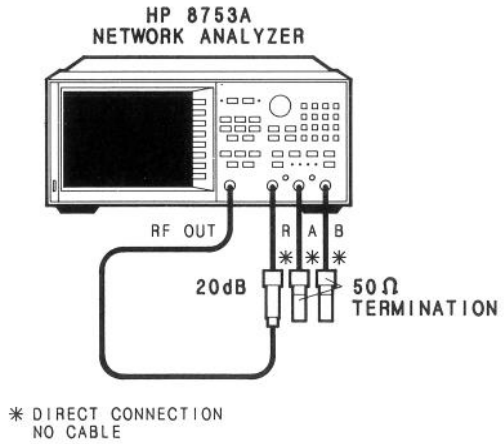


Figure 3. Noise Level Test Setup

EQUIPMENT

20 dB Attenuator	HP 8491A Option 020
50Ω Termination (2)	HP 908A
RF Cable	Part of the HP 11851B Cable Set

PROCEDURE

1. Connect the equipment as shown in Figure 3. Press **[PRESET]**. The IF bandwidth is now 3 kHz, the default value assigned when the instrument is preset.
2. Press **[MEAS] [A] [FORMAT] [LIN MAG]** to format input A for linear magnitude.
3. Press **[SCALE REF] [AUTO SCALE]** to bring the input A trace into view.
4. Press **[MKR FCTN] [STATS ON]** to display marker statistics.
5. Press **[MENU] [POWER] [-] [1] [0] [x1]** to set the power at input R to −30 dBm.
6. Press **[MENU] [TRIGGER MENU] [SINGLE]** to enable a single sweep, and note the trace mean value at the completion of the sweep. The mean value is displayed as a marker statistic in the upper right-hand corner of the display.

   The mean value is displayed typically in μU (microvolts), or nU (nanovolts), and has the following relationship with receiver noise level power in dBm:

   power (dBm) = 20 Log_{10} (Linear Magnitude measured value)

   −90 dBm corresponds with 31.623 μU.
   −100 dBm corresponds with 10 μU.

   Calculate the power level of the value just measured using the above equation. Record this power level in the Performance Test Record located at the end of the Manual Performance Tests section.
7. Press **[MEAS] [B] [FORMAT] [LIN MAG]** to format input B for linear magnitude. Repeat step 6 for input B with a 3 kHz IF bandwidth.
8. Press **[AVG] [IF BW] [1] [0] [x1]** to select an IF bandwidth of 10 Hz.

   In the next steps, the sweep time is automatically increased (decreasing the sweep rate) to accomodate the decreased IF bandwidth, and "CAUTION: SWEEP TIME INCREASED" appears on the display. Disregard this message.
9. Repeat step 6 for input B with a 10 Hz IF bandwidth.
10. Press **[MEAS] [A]** to select input A magnitude. Repeat step 6 for input A with a 10 Hz IF bandwidth.

IN CASE OF DIFFICULTY

If the receiver noise level performance test fails on all inputs, suspect a faulty A10 digital IF board assembly.

The ADC linearity correction constants adjustment is related to this performance test. Refer to the Receiver Functional Group portion of the Service section for related troubleshooting information.

Input Crosstalk

SPECIFICATIONS

Input Crosstalk (10 Hz IF bandwidth): −100 dB from 300 kHz to 1 GHz
−90 dB from 1 GHz to 3 GHz

DESCRIPTION

Crosstalk is defined as leakage interference between inputs, and is tested by observing the signal level on a terminated input while driving another input. Because the signal into R input is required for phase lock, crosstalk interference into R input is not tested (A-into-R, or B-into-R).

In the following procedure, an RF signal is connected to input R to check input R crosstalk (R-into-A, and R-into-B). An RF signal is then connected to input B to test input B crosstalk (B-into-A). Lastly, an RF signal is connected to input A to test input A crosstalk (A-into-B).

Ratioed measurements are used to compensate for any frequency response effects.

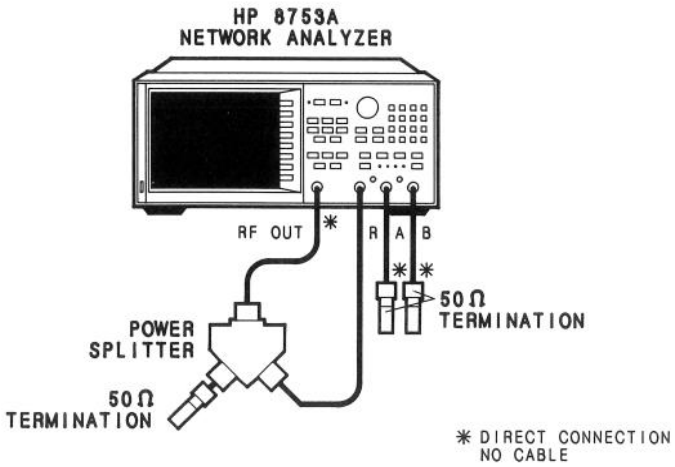


Figure 4. R-into-A and R-into-B Input Crosstalk Test Setup

EQUIPMENT

50Ω Power Splitter	HP 11667A Option 001
50Ω Termination (3)	HP 908A
20 dB Attenuator	HP 8491A Option 020
50Ω RF Cable Set	HP 11851B

PROCEDURE

1. Connect the equipment as shown in Figure 4.
2. Press **[PRESET]**. During preset, A/R is selected as the default measurement parameter.
3. Press **[AVG] [AVERAGING FACTOR] [5] [x1] [AVERAGING ON]** to enable a sweep-to-sweep IF averaging factor of 5.
4. Press **[IF BW] [1] [0] [x1]** to select a 10 Hz bandwidth. Disregard the "CAUTION: SWEEP TIME INCREASED" message on the display.
5. Press **[MKR FCTN] [MARKER → REFERENCE]** to bring the A/R trace to the reference line.
6. Press **[MKR SEARCH ON] [TRACKING ON] [SEARCH: MAX]** to select continuous marker tracking of the peak signal.
7. Press **[MENU] [POWER] [6] [x1]** to set the power level into R input to 0 dBm.
8. Press **[START] [.] [3] [M/u] [STOP] [1] [G/n]** to set a frequency span of .3 MHz to 1 GHz.
9. Observe the number of averaged sweeps shown in the upper left-hand side of the display. When the fifth sweep has completed (in approximately two minutes), note the marker value in the upper right-hand corner of the display. This is the peak value of crosstalk.

   Record this value in the Performance Test Record located at the end of the Manual Performance Tests section.
10. Press **[START] [1] [G/n] [STOP] [3] [G/n]** and repeat step 9 to measure R-into-A crosstalk in the 1 GHz to 3 GHz frequency range.
11. Press **[MEAS] [B/R]** and repeat step 9 to measure R-into-B crosstalk in the 1 GHz to 3 GHz frequency range.
12. Repeat steps 8 and 9 to measure R-into-B crosstalk in the .3 MHz to 1 GHz range.
13. Connect the equipment as shown in Figure 5.
14. Press **[MEAS] [A/B]** and repeat step 9 to measure B-into-A crosstalk in the .3 MHz to 1 GHz frequency range.
15. Press **[START] [1] [G/n] [STOP] [3] [G/n]** and repeat step 9 to measure B-into-A crosstalk in the 1 GHz to 3 GHz frequency range.
16. Remove the 50Ω load from input A. Remove the cable from input B and connect it to input A. Connect the 50Ω load to input B.
17. Press **[MEAS] [CONVERSION ON] [1/S]** to convert A/B to a B/A measurement.
18. Repeat step 9 to measure A-into-B crosstalk in the 1 GHz to 3 GHz frequency range.
19. Repeat steps 8 and 9 to measure A-into-B crosstalk in the .3 MHz to 1 GHz range.

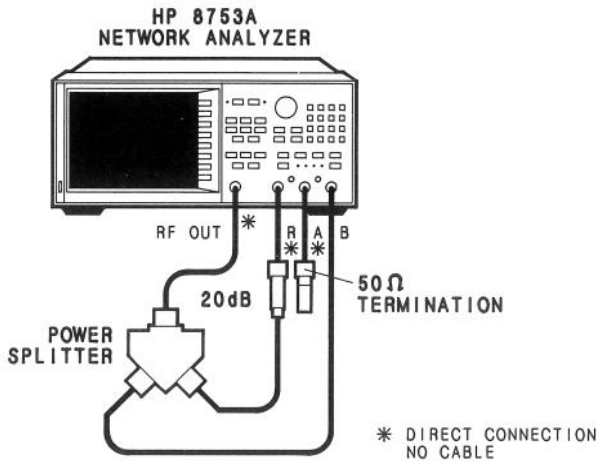


Figure 5. B-into-A Input Crosstalk Test Setup

IN CASE OF DIFFICULTY

If any part of the input crosstalk performance test fails, first make sure that all external RF test cable and termination connectors are tight. Inspect all cables for signs of damage, wear, or faulty shielding.

Remove the network analyzer top cover and tighten any loose SMA connector nuts on the four semi-rigid cables located between the A4/5/6 sampler/mixer assemblies and the front panel type-N connectors. These connectors should be torqued to 8 pound-inches.

Tighten any loose screws on the A4/5/6 sampler/mixer assembly covers, and on the A7 pulse generator assembly. Inspect the shielding clips on the A5 sampler/mixer and A7 pulse generator. Inspect the shielding posts on the A10 digital IF board assembly.

There are no related adjustments for this performance test. Refer to the Receiver Functional Group portion of the Service section for related troubleshooting information.

Trace Noise

SPECIFICATIONS

Trace Noise: (A/R, B/R, A/B, at −10 dBm, 3 kHz bandwidth)	Magnitude: Phase:	<0.006 dB rms <0.035° rms

DESCRIPTION

This test measures trace noise on a high level CW signal in ratio mode. The test is done in CW in order to eliminate any effects of frequency response. It is tested at 3 GHz because conditions are the noisiest at that frequency.

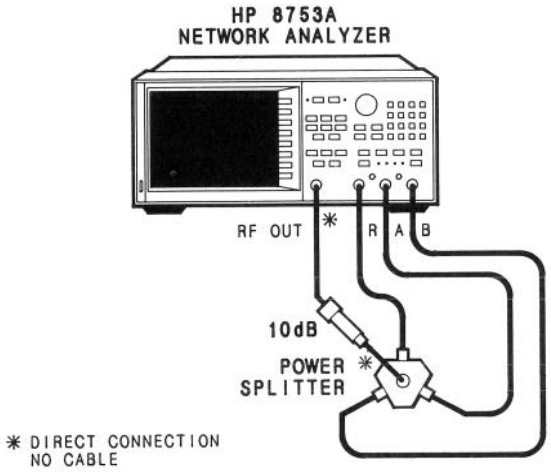


Figure 6. Trace Noise Test Setup

EQUIPMENT

50Ω Three-Way Power Splitter	HP 11850C
10 dB Attenuator	HP 8491A Option 010
50Ω RF Cable Set	HP 11851B

PROCEDURE

1. Connect the equipment as shown in Figure 6.
2. Press **[PRESET]**.
3. Press **[MEAS] [A/R]** to select A/R magnitude.
4. Press **[MENU] [POWER] [1] [0] [x1]** to adjust the power level to approximately −10 dBm into each input.
5. Press **[MENU] [NUMBER OF POINTS] [1] [6] [0] [1] [x1]** to increase the number of points measured to 1,601.
6. Press **[CW FREQ] [3] [G/n]** to select a CW frequency of 3 GHz.
7. Press **[MKR FCTN] [STATS ON]** to enable marker statistics.
8. Note the standard deviation trace value, displayed as a marker statistic (s. dev) in the upper right-hand corner of the display. This value corresponds directly to rms, and is updated after each sweep.

   Record this value on the Performance Test Record located at the end of the Manual Performance Tests section.
9. Press **[MEAS] [B/R]** to enable a B/R ratio measurement, and repeat step 8 for B/R.
10. Press **[A/B]** to enable an A/B ratio measurement, and repeat step 8 for A/B.
11. Press **[FORMAT] [PHASE]** to set A/B for phase format. Repeat step 8.
12. Press **[MEAS] [B/R] [FORMAT] [PHASE]** to set B/R for phase format. Repeat step 8.
13. Press **[MEAS] [A/R] [FORMAT] [PHASE]** to set A/R for phase format. Repeat step 8.

IN CASE OF DIFFICULTY

If this test fails, suspect a problem on the A10 digital IF board assembly.

There are no related adjustments for this performance test. Refer to the Receiver Functional Group portion of the Service section for related troubleshooting information.

Frequency Response

SPECIFICATIONS

Magnitude Ratio Accuracy (A/R, B/R, A/B): ±0.5 dB
(−10 dBm on all inputs)

Phase Frequency Response (A/R, B/R, A/B): ±3° from linear phase
(−10 dBm on all inputs)

DESCRIPTION

Magnitude ratio accuracy is the frequency response tracking between two inputs and is determined by measuring the peak-to-peak variation of the ratioed trace.

Phase frequency response is phase tracking and is measured as deviation from linear phase.

Both magnitude and phase frequency response are tested for A/R, B/R, and A/B input ratios in swept mode.

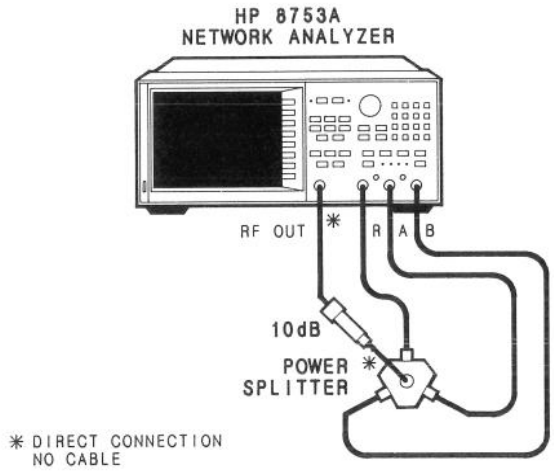


Figure 7. Frequency Response Test Setup

EQUIPMENT

50Ω Three-Way Power Splitter	HP 11850C
10 dB Attenuator	HP 8491A Option 010
50Ω RF Cable Set	HP 11851B

PROCEDURE

Magnitude Ratio Accuracy

1. Connect the equipment as shown in Figure 7.
2. Press **[PRESET]**.
3. Press **[MENU] [POWER] [1] [0] [x1]** to set the power level to approximately −10 dBm at all inputs.
4. Press **[MEAS] [A/R]** to measure A/R magnitude ratio.
5. Press **[SCALE REF] [.] [1] [x1]** to set the scale to .1 dB per division.
6. Press **[MARKER → REFERENCE]** to bring the trace to the reference line.
7. Press **[DISPLAY] [DATA → MEMORY]** to store the measured data. The instrument will beep to indicate that the trace is stored.
8. Reverse the R and A cable connections on the HP 8753A input ports. Disregard any CAUTION messages on the CRT, as the HP 8753A loses phase lock whenever the R input is disconnected.
9. Press **[DATA and MEMORY]**. Visually average the two traces. In other words, imagine a trace directly between the two traces. This average "trace" must be $< \pm 0.5$ dB (five divisions) peak to peak.

   If both traces are not completely visible, increase the scale per division. Press **[SCALE REF]** and enter an appropriate value using the keypad.

   The averaged result represents the A/R magnitude frequency response of the input alone, without frequency tracking errors from the power splitter or cables. Record the maximum "averaged" power deviation on the Performance Test Record located at the end of the Manual Performance Tests section.
10. Press **[DISPLAY] [DATA] [MEAS] [B/R]** and repeat steps 6 through 9 for B/R, except reverse the B and R input cable connections in step 8.
11. Press **[DISPLAY] [DATA] [MEAS] [A/B]** and repeat steps 6 through 9 for A/B, except reverse the A and B input cable connections in step 8.

Phase Ratio Accuracy

1. Press **[PRESET].**
2. Press **[MENU] [POWER] [1] [0] [x1]** to set the HP 8753A power level to approximately −10 dBm at the input ports.
3. Press **[MKR FCTN] [STATS ON]** to select marker statistics.
4. Press **[MEAS] [A/R] [FORMAT] [PHASE]** to set the A/R response format to measure phase.
5. Press **[SCALE REF] [.] [6] [x1]** to set the scale to 600 m° per division.
6. Press **[ELECTRICAL DELAY]** to enable electrical delay.
7. Turn the RPG to vary the electrical delay until the trace is in the most linear horizontal position. The resultant trace must be $< \pm 3$ degrees (± 5 divisions) from the center reference line.

8. Press **[MENU] [TRIGGER MENU] [SINGLE]** to enable a single sweep. When the sweep is completed, note the peak-to-peak (p-p) trace value on the display. This value is displayed as a marker statistic in the upper right-hand corner of the display.

   Record this value of phase deviation on the Performance Test Record located at the end of the Manual Performance Tests section.

9. Press **[CONTINUOUS]** to enable continuous sweep.

10. Press **[MEAS] [B/R] [FORMAT] [PHASE]** and repeat steps 6 through 9 for B/R phase.

11. Press **[MEAS] [A/B] [FORMAT] [PHASE]** and repeat steps 6 through 9 for A/B phase.

IN CASE OF DIFFICULTY

The phase ratio accuracy measurement can exhibit some characteristics of the splitter. If this test fails, move the RF cables to different ports on the power splitter and re-measure the inputs that failed.

Two adjustments are related to this performance test. They are the sampler diode bias adjustment, and the sampler magnitude and phase correction constants. Refer to the Receiver and Source Functional Group portions of the Service section for related troubleshooting information.

Absolute Amplitude Accuracy

SPECIFICATIONS

Absolute Amplitude Accuracy: 300 kHz to 3.0 GHz: ±1.0 dB
(A, B, R at −10 dBm input)

DESCRIPTION

Absolute amplitude accuracy is a measure of receiver performance alone, regardless of source power variation. It is a measure of how well information is transferred from RF to IF and how accurately that information is processed and displayed.

A CW signal is applied to a power meter and input R using a 2-way power splitter. The splitter is then connected to inputs A and B in turn and the absolute power level of each input is compared to the earlier power meter reading. The process is repeated at several different frequencies.

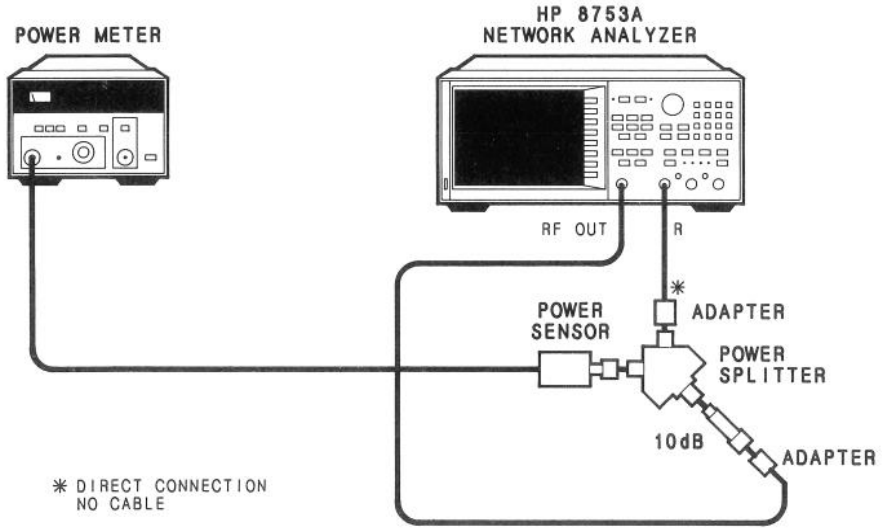


Figure 8. Absolute Amplitude Accuracy Test Setup (Input R)

EQUIPMENT

Power Meter	HP 436A
Power Sensor	HP 8482A
50Ω Power Splitter	HP 11667A Option 001
10 dB Attenuator	HP 8491A Option 010
RF Cable Set	HP 11851B
Adapter type-N (m) to type-N (m)	HP part number 1250-1475
Adapter type-N (f) to type-N (f)	HP part number 1250-1472

PROCEDURE

1. In the following steps, set the power meter cal factor whenever necessary to compensate for variations in power sensor frequency response. Set the power meter mode to measure dBm, and zero the meter.

   Connect the equipment as shown in Figure 8.

2. On the HP 8753A, press **[PRESET]**.

3. Press **[MEAS] [R]** to select R input.

4. Press **[MENU] [POWER] [6] [x1]** to set the R input power level to approximately −10 dBm.

5. Press **[MKR]** to enable a marker to read the input power level.

6. Use the Performance Test Record located at the end of the Manual Performance Tests section to record power levels in the following steps.

7. Press **[MENU] [CW FREQ] [3] [0] [0] [k/m]** to select 300 kHz CW.

8. For each frequency on the Performance Test Record, record the power meter reading and the R input marker power reading in the upper right-hand corner of the display. Use the HP 8753A keypad to change frequency.

9. Repeat step 8 for any other frequency of interest. Extra spaces are provided on the Performance Test Record for this purpose.

10. Connect the equipment as shown in Figure 9.

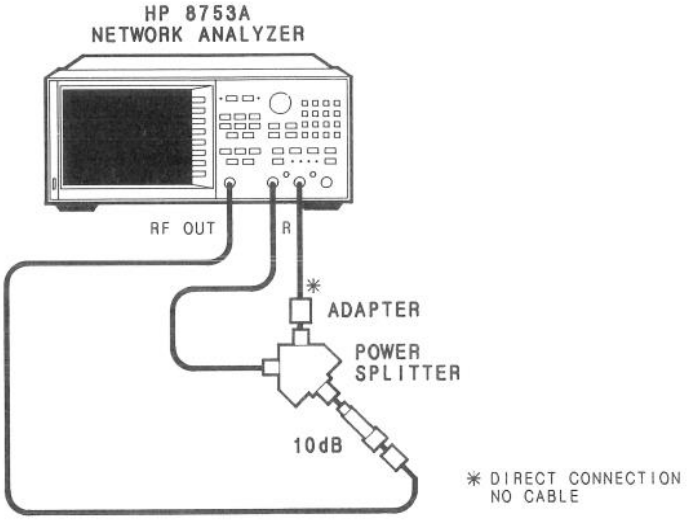


Figure 9. Absolute Amplitude Accuracy Test Setup (Input A)

11. Press **[MEAS] [A]** to select input A.

12. Press **[MENU] [CW FREQ] [3] [0] [0] [k/m]** to select 300 kHz CW.

13. For each frequency on the Performance Test Record, record the input A power marker reading in the upper right-hand corner of the display. Use the HP 8753A keypad to change frequency.

14. Repeat step 13 for any other frequency of interest.

15. Disconnect the power splitter from input A and connect it to input B.

16. Press **[MEAS] [B]** to select input B. Repeat steps 12 through 14 for input B.

17. When all readings have been taken, calculate the difference between the power meter reading and the R, A, and B input readings taken at each frequency. Record the greatest variation in the space provided on the Performance Test Record.

    The final results represent the worst-case absolute amplitude accuracy values for all inputs at the selected frequencies.

IN CASE OF DIFFICULTY

If all inputs fail, suspect poor tracking between ports of the HP 11667A Power Splitter in the test setup.

If inputs A and B fail this test at any frequency, the cause may be source drift of the network analyzer. If this is suspected, connect the equipment as shown in Figure 8, set the power level at the frequency of interest, and repeat the test for that input.

Two adjustments are related to this performance test. They are the sampler diode bias adjustment, and the sampler magnitude and phase correction constants. Refer to the Receiver and Source Functional Group portions of the Service Section for related troubleshooting information.

Input Impedance

SPECIFICATIONS

Input Impedance:	50Ω nominal
Return Loss:	>20 dB from 300 kHz to 2 MHz
	>23 dB from 2 MHz to 2 GHz
	>20 dB from 2 GHz to 3 GHz

DESCRIPTION

The return loss of each input is measured using a transmission/reflection test set and the other two inputs of the HP 8753A.

A/R is used to measure the input impedance of input B. Likewise, B/R is used to measure the input impedance of input A. Because input R must be phase-locked for operation, a power splitter is used in the R input impedance test. A/B is used in this case.

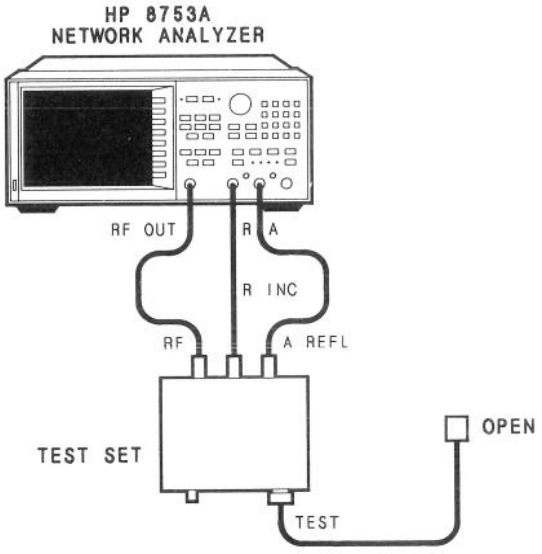


Figure 10. Input B Impedance Test Setup

EQUIPMENT

50Ω Transmission/Reflection Test Set	HP 85044A
50Ω Power Splitter	HP 11667A Option 001
10 dB Attenuator	HP 8491A Option 010
50Ω Termination	HP 908A
50Ω Type-N Calibration Kit	HP 85032B
50Ω Type-N RF Cable Set	HP 11851B
RF Cable	part of the HP 11857D 7mm Test Port Return Cable Set

PROCEDURE

1. Connect the equipment as shown in Figure 10. The HP 85046A 50Ω S-parameter test set may be substituted for the HP 85044A 50Ω transmission/reflection test set. In that case, use port 1 of the HP 85046A. Remember to connect the test set interconnect cable.

2. Press **[PRESET]**. A/R magnitude is automatically selected as the default parameter.

3. Press **[MENU] [NUMBER OF POINTS] [1] [6] [0] [1]** to select 1,601 points. Then connect the 7mm/type-N(m) adapter to the end of the test port cable.

4. Press **[CAL] [CAL KIT] [N 50Ω]** to reference a 50Ω type-N calibration kit for calibration.

5. Press **[CAL] [CALIBRATE MENU] [S11 1-PORT]** to initiate a calibration sequence that will correct for basic reflection measurement frequency response errors.

6. Connect a type-N (f) open to the male adapter on the test port cable and press **[OPENS] [OPEN (M)] [DONE: OPENS]**.

7. Connect a type-N (f) short to the male adapter on the test port cable and press **[SHORTS] [SHORT (M)] [DONE: SHORTS]**.

8. Connect a type-N (f) 50Ω termination to the end of the test port cable and press **[LOAD]**.

9. Press **[DONE 1-PORT CAL]** to complete the calibration sequence (this takes approximately one minute).

10. Remove the 50Ω termination from the end of the test port cable and connect the cable to the open input port on the HP 8753A.

11. Press **[SCALE REF] [AUTO SCALE]** to bring the entire trace into view.

12. Press **[MKR] [MARKER 1] [.] [3] [M/u]** to set marker 1 to 300 kHz. Observe the marker power level in the upper right-hand corner of the display, and record this value in the Performance Test Record located at the end of the Manual Performance Tests section.

    Return loss in the 300 kHz to 2 MHz frequency range is only tested at 300 kHz because return loss is always the greatest at that frequency.

13. Press **[MARKER 1] [2] [M/u]** to set marker 1 to 2 MHz. Press **[MARKER 2] [2] [G/n]** to set marker 2 to 2 GHz. Observe the displayed trace and note the worst-case (peak) value of return loss between the two markers. Turn the RPG (rotary pulse generator) to move marker 2 to the peak value just observed.

If the worst-case peak is not obvious, press **[MARKER 1]** to select marker 1 (which should be set to 2 MHz). Rotate the RPG knob clockwise until 2 GHz is reached. Note the worst-case reading of return loss as the marker frequency is changed.

Record the worst-case value of return loss in the Performance Test Record.

14. Press **[MARKER 1] [2] [G/n]** to set marker 1 to 2 GHz, and press **[MARKER 2] [3] [G/n]** to set marker 2 to 3 GHz.

15. Observe the displayed trace and note the worst-case (peak) value of return loss between the two markers. Turn the RPG (rotary pulse generator) to move marker 2 to the peak value just observed.

    If the worst-case peak is not obvious, press **[MARKER 1]** to select marker 1 (which should be set to 2 GHz). Rotate the RPG knob clockwise until 3 GHz is reached. Note the worst-case reading of return loss as the marker frequency is changed.

    Record the worst-case value of return loss in the Performance Test Record.

16. Press **[MEAS] [B/R]** to select B/R magnitude. Connect the equipment as shown in Figure 11 and repeat steps 4 through 15 for input A return loss.

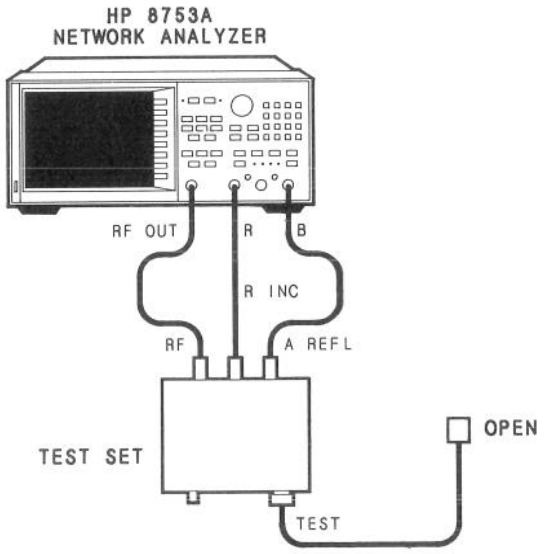


Figure 11. Input A Impedance Test Setup

17. Connect the equipment as shown in Figure 12. Press **[MEAS] [A/B]** and repeat steps 4 through 9 to perform a calibration.

18. Connect the equipment as shown in Figure 13.

19. Repeat steps 11 through 15 to measure R input return loss.

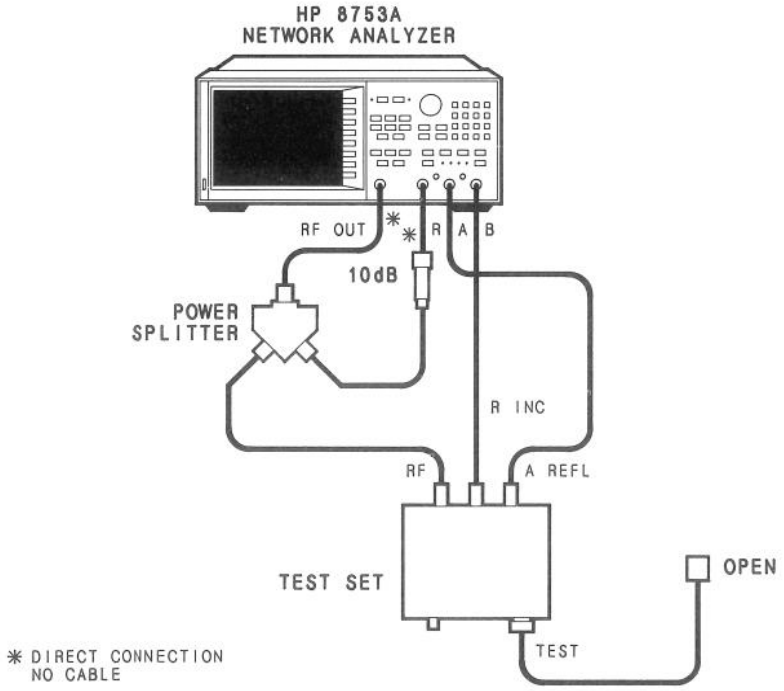


Figure 12. Input R Impedance Test Calibration Setup

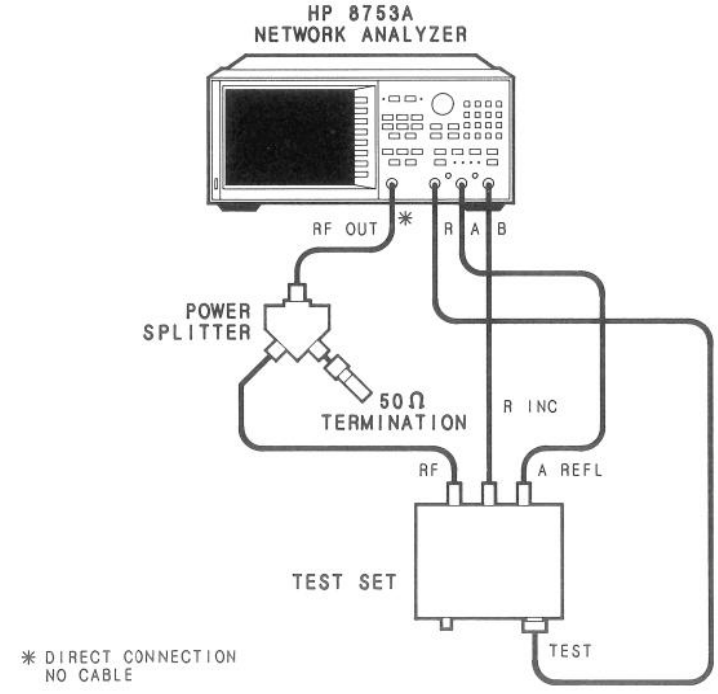


Figure 13. R Input Impedance Test Setup

IN CASE OF DIFFICULTY

Check the type-N input connectors for signs of damage or excessive wear.

Any impedance mismatch is caused by either the input connector, the sampler, or the semi-rigid coaxial cables connecting the A4/5/6 sampler/mixer assemblies to the front panel type-N connectors.

If no damage is apparent at the input connector, try interchanging sampler assemblies. If the problem goes away, the sampler is defective. If it does not go away, suspect the path from input to sampler.

There are no related adjustments for this performance test. Refer to the Receiver Functional Group portion of the Service section for related troubleshooting information.

Manual Performance Tests Record

Manual Performance Test Record (1 of 3)

FREQUENCY RANGE AND ACCURACY

Instrument Frequency (MHz)	Measured Value	Measurement Frequency Range (MHz)			Specification
0.3	_____	0.299997	to	0.300003	± 3 Hz
5.0	_____	4.99995	to	5.00005	± 50 Hz
16.0	_____	15.99984	to	16.00016	± 160 Hz
31.0	_____	30.99969	to	31.00031	± 310 Hz
60.999999	_____	60.99939	to	61.00061	± 610 Hz
121.0	_____	120.99879	to	121.00121	± 1.21 kHz
180.0	_____	179.9982	to	180.0018	± 1.8 kHz
310.0	_____	309.9969	to	310.0031	± 3.1 kHz
700.0	_____	699.9930	to	700.0070	± 7 kHz
1400.0	_____	1399.986	to	1400.014	± 14 kHz
3000.0	_____	2999.970	to	3000.030	± 30 kHz

MINIMUM R LEVEL

Frequency Range	Pass/Fail
0.3 MHz to 3.299999 MHz	_____
3.3 MHz to 4.299999 MHz	_____
4.3 MHz to 15.999999 MHz	_____
16 MHz to 3 GHz	_____

RECEIVER NOISE LEVEL

Measurement	Measured Value	Specification
Input A (3 kHz IF BW)	_____	−90 dBm
Input B (3 kHz IF BW)	_____	−90 dBm
Input B (10 Hz IF BW)	_____	−100 dBm
Input A (10 Hz IF BW)	_____	−100 dBm

INPUT CROSSTALK		
Measurement	**Measured Value**	**Specification**
Input A (A/R, R into A) 300 kHz to 1 GHz	_____	−100 dBm
Input A (A/R, R into A) 1 GHz to 3 GHz	_____	−90 dBm
Input B (B/R, R into B) 1 GHz to 3 GHz	_____	−90 dBm
Input B (B/R, R into B) 300 kHz to 1 GHz	_____	−100 dBm
Input A (A/B, B into A) 300 kHz to 1 GHz	_____	−100 dBm
Input A (A/B, B into A) 1 GHz to 3 GHz	_____	−90 dBm
Input B (B/A, A into B) 1 GHz to 3 GHz	_____	−90 dBm
Input B (B/A, A into B) 300 kHz to 1 GHz	_____	−100 dBm

TRACE NOISE		
Measurement	**Measured Value**	**Specification**
A/R Magnitude	_____	< 0.006 dB
B/R Magnitude	_____	< 0.006 dB
A/B Magnitude	_____	< 0.006 dB
A/R Phase	_____	< 35 m°
B/R Phase	_____	< 35 m°
A/B Phase	_____	< 35 m°

FREQUENCY RESPONSE		
Measurement	**Measured Value**	**Specification**
Input A/R Magnitude	_____	±0.5 dB
Input B/R Magnitude	_____	±0.5 dB
Input A/B Magnitude	_____	±0.5 dB
Input A/R Phase	_____	±3°
Input B/R Phase	_____	±3°
Input A/B Phase	_____	±3°

Manual Performance Test Record (3 of 3)

ABSOLUTE AMPLITUDE ACCURACY

Frequency	Power Meter Reading	R Input Power	A Input Power	B Input Power	Greatest Difference
300 kHz					
5 MHz					
16 MHz					
31 MHz					
61 MHz					
121 MHz					
180 MHz					
310 MHz					
700 MHz					
1.5 GHz					
2.0 GHz					
2.5 GHz					
3.0 GHz					

INPUT IMPEDANCE

Frequency Range	A/R (B Return Loss)	B/R (A Return Loss)	A/B (R Return Loss)	Specification
0.3 MHz to 2 MHz				> 20 dB
2 MHz to 2 GHz				> 23 dB
2 GHz to 3 GHz				> 20 dB

Automated Performance Tests

Software Revision A.01.00

INTRODUCTION

NOTE: Read the next few pages before attempting to run the performance test software. This will avert most problems before they arise.

This section of the performance tests contains instructions and setup diagrams for several automated tests. Automated tests require an HP 9000 series 200/300 desktop computer, associated peripherals and the software provided on disc in this manual. These tests do require operator interaction and are best described as semiautomated.

The rest of this section is organized as follows:

SETTING UP THE SYSTEM: This provides hardware and software model numbers for proper system configuration. It also provides instructions for loading the operating system.

SOFTWARE BACK-UP: This defines the files provided with the performance test software, and also provides instructions for disc copying .

GETTING STARTED: This provides instructions for loading the performance test program. The initial menus associated with program setup are common to all tests, and are documented here. Error messages and recovery from error conditions are discussed. For best results, read the material in this section prior to running test software.

TEST PROCEDURES: Each test procedure is documented separately, with a description of the test and the measured specification. A step-by-step procedure is provided which often references the material in GETTING STARTED. Test set-up diagrams for each test are provided.

SETTING UP THE SYSTEM

System Hardware Configuration

Controllers. The HP 9000 series 200/300 controllers listed in Table 2 can be used to run the performance tests. Other controllers not listed here may work.

Table 2. HP 9000 Controller Models

Series 200: 216, 226, 236, 220
Series 300: 310

Peripherals. The automated tests require mass storage and a printer. (The required measurement instrumentation is listed in the test procedure.)

There are many compatible disc drives. Software is provided on a 3.5 inch floppy disc, formatted single sided so it will be usable in either single or double sided disc drives. The following drives are recommended as a convenience only. Most HP drives will work.

Table 3. Compatible Disc Drives

Model Number	Command Set
HP 9121D	AMIGA
HP 9133A	AMIGA
HP 9133B	AMIGA
HP 9133V/XV	AMIGA
HP 9122D	CS80
HP 9133D/H	CS80
HP 9153A	CS80

A printer is always required to record test results. All test results are output in test record format. Some tests provide additional output in graphical form. This requires a printer capable of accepting raster data (dump graphics) from the controller. Printers that are known to have this capability are listed below.

Table 4. Compatible Printers

HP 2225A ThinkJet
HP 2671G/2673A Thermal Printer
HP 9876A Thermal Line Printer

System Software Requirements

The HP 8753A performance test software requires BASIC versions 3.0 or 4.0.

To load the BASIC system, locate the BASIC System Disc. Insert the disc into the disc drive and power on the computer. The computer will locate the BASIC operating system and load it into memory.

BASIC versions 3.0 and 4.0 provide a modular operating system architecture. The core of the system is provided on the operating system disc. Additional computation and IO capability is available through the use of code modules called binaries. Binaries are separated into two groups: Language Extensions and Drivers. The automated performance test software requires the following binaries.

Table 5. Required Binaries

Language Extensions	Drivers
ERR GRAPH IO KBD MAT MS	CS80 or DISC (depends on disc) HPIB CRTA or CRTB (depends on CRT)

If you already have a pre-configured BASIC system, you can verify whether or not it contains all of the above binaries. Type:

```
LIST BIN
```
(press **[ENTER]** or **[RETURN]** to execute the command)

All binaries currently contained in memory will be listed to the screen. If any of the required binaries are missing, insert the Drivers disc provided with the system and load the Configure program. Type:

```
LOAD "CONFIGURE"
```

Press **[RUN]** to start the program.

This program lets you select the necessary binary modules and loads them for you. Simply follow the prompts. The program tells you to load the appropriate disc, lists the binaries available on that disc and links that binary into the system upon your command.

You must know what type of disc drive you are using and the command set it uses to select the correct mass storage driver. Drives using CS80 or SS/80 command set require the CS80 binary. (Most drives which read double-sided media use CS80 command set.) Other discs use the AMIGA protocol and require the DISC binary. Table 3 lists the command set used by several HP disc drives. If you are unsure, load both binaries.

Refer to the BASIC user's documentation for more comprehensive instructions on loading the operating system and binaries.

SOFTWARE BACKUP

Disc Files

The performance test and adjustment software, HP part number 08753-10010, is provided on two single-sided discs. The files contained on these discs are as follows:

DISC 1

PERFTEST	:	main test program
MS_CONFG	:	mass storage configuration file
DEV_CONFG	:	device configuration file
API_ADJ	:	adjustment program for A13 API spurs

DISC 2

power_test	:	output power test subprograms
spur_test	:	spectral purity test subprograms
dyaccytest	:	dynamic accuracy test subprograms
HP436A	:	HP 436A subprograms
HP438A	:	HP 438A subprograms

Making Working Copies

NOTE: Before doing anything else, make working copies of these discs!

The master discs are shipped from the factory write-protected and cannot be written to or initialized in this mode. We recommend you maintain these discs in write-protect mode. During execution, the performance test program must read from and write to one of these discs, therefore it must not be write-protected in normal use. You must copy the master discs to working copies using the instructions below. If the working copy is damaged or lost, the master is always available.

NOTE: The files contained on Disc 1 must reside on the same mass storage medium. Likewise, the files on Disc 2 must reside on the same mass storage medium.

To copy the master disc, you must initialize a blank disc. Insert a blank disc into the disc drive and type:

```
INITIALIZE ":msus"
```

where *msus* is the address of the drive containing the disc to be initialized. The initialization process takes approximately 60 seconds.

To copy the contents of the master disc to the working disc, follow the instructions below:

Copying to a Hard Disc or Double-Sided Flexible Disc

If you copy both master discs to a storage medium of a larger size, you will have to perform a file-by-file copy instead of copying the entire volume at once. To perform a file copy, follow the instructions below. After typing a command from the keyboard, press **[ENTER]** or **[RETURN]** to execute the command.

1. Insert the master disc into the drive and obtain a directory listing. Type:

   ```
   CAT ":msus"
   ```

   where *msus* is the mass storage unit specifier of the drive containing the master disc.

2. If you are copying to a flexible disc, insert the initialized working disc into the second drive. Type:

   ```
   COPY "filename:master msus"    TO    "filename:destination msus"
   ```

   where *master msus* is the mass storage unit specifier of the disc drive containing the master disc and *destination msus* is the mass storage unit specifier of the flexible or hard disc drive containing the working storage media.

   Perform step 2 for each file in the master disc directory listing, for each master disc.

   An example: Your system includes an HP 9133H disc drive at HP-IB address 700. The hard disc is unit 0 and the floppy drive is unit 1. (The hard disc can be configured as one large volume or several.) To file copy from the master disc in the floppy drive to volume 3 of the hard disc, the copy command syntax would be:

   ```
   COPY "PERFTEST:,700,1"    TO    "PERFTEST:,700,0,3"
   ```

Copying Flexible Discs with Two Drives

1. Insert the master disc into one drive and the initialized working disc into the other drive.
2. Type:

   ```
   COPY ":source msus"    TO    ":destination msus"
   ```

   where *source msus* is the mass storage unit specifier of the drive containing the disc you want to copy, and *destination msus* is the mass storage unit specifier of the drive containing the initialized working disc.

   An example: With an HP 9122D dual disc drive at address 700, the master disc in the left drive, and the working disc in the right drive, the copy command syntax would be:

   ```
   COPY ":,700,0"    TO    ":,700,1"
   ```

Copying Flexible Discs with One Drive

When only one drive is available, disc contents must first be copied into memory, then from memory to the destination disc.

1. Type:

   ```
   INITIALIZE ":MEMORY,0"
   ```

2. Insert the master disc into the disc drive.
3. Type:

   ```
   COPY ":msus"    TO    ":MEMORY,0"
   ```

   where *msus* is the mass storage unit specifier of the disc drive.

4. When the copying is done, remove the master disc from the disc drive and insert an initialized disc into the drive.
5. Type:

   ```
   COPY ":MEMORY,0"    TO    ":msus"
   ```

   where *msus* is the mass storage unit specifier of the disc drive.

GETTING STARTED

The following text provides instructions on loading the performance test software and interacting with the program. If you wish to run the software while reading the instructions, then you must refer to the TEST PROCEDURE subsection and connect the system as indicated for the test you wish to run. Then follow the procedure for that test. It will refer you back to GETTING STARTED for instructions on using the program menus and prompts.

Loading the Performance Test Program

NOTE: Before loading or running programs, set the mass storage unit specifier (MSUS) to the address of the drive containing Disc 1 of the performance test software.

Example: Your system mass storage is an HP 9122 dual disc drive. Insert Disc 1 into the left drive and type:

```
MSI ":,700,0"
```

This command sets the current MSUS to drive 0 of the mass storage device at HP-IB address 700. If the MSUS is not set to the drive containing Disc 1 files, subsequent program errors will occur.

Load the performance test program. Type:

```
LOAD "PERFTEST"
```

Press **[RUN]**.

During the initialization process, the program searches for the files MS_CONFG and DEV_CONFG at the current MSUS. If these files are not present, an error is reported.

HP 8753A System Configuration Menu

The first menu you see will be the HP 8753A System Configuration Menu.

Press **[SELECT]** to select **EDIT MASS STORAGE**.

Edit Mass Storage. Selecting this menu allows you to establish where certain files will reside: CALIBRATION DATA files, and DISC 2 FILES.

Later in the program, you will enter power sensor calibration data. The program will store this data into a file so that it can be easily retrieved at a later date.

Press the **[SELECT]** softkey. Type in the MSUS of the mass storage media where the calibration data should be stored. (Since you made copies of the master discs, and they are no longer write-protected, you can elect to store calibration data files on either of these discs.)

Press **[▼]** and **[SELECT]** to modify the MSUS for volume DISC2 FILES. Type in the MSUS for the mass storage device containing Disc 2.

Example: Your system consists of an HP 9836A and an HP 9122D dual disc drive at HP-IB address 700. Disc 1 resides in unit 0 of your HP 9122. Disc 2 resides in unit 1. You decide to store calibration data on a 5.25 inch floppy in one of the internal drives of the HP 9836. Modify the mass storage config edit menu as follows:

VOLUME LABEL	MSUS	SRM DIRECTORY PATH
CALIBRATION DATA	:INTERNAL,4,1	
DISC2 FILES	:,700,1	

The changes made to the mass storage menu are re-stored into file MS_CONFG and will therefore be in effect the next time the program is run. You won't need to re-edit this menu each time the program is run as long as the system configuration remains the same.

If you are using an SRM system, press the right arrow key **[▶]**. A third column should appear on the screen entitled SRM. This column must contain the directory path for the volume label, and the MSUS column must contain the remote MSUS (":REMOTE").

When you are finished editing the mass storage menu, press **[DONE]**. The program returns to the HP 8753A system configuration menu.

Press **[▼]** and **[SELECT]** to select **EDIT DEVICE ADDRESSES**.

Edit Device Addresses. This menu contains four columns, two of which are visible on the screen at any one time. Use the cursor control keys (left, right, up, down) to select different parts of this menu. To view columns three and four, press **[▶]**, twice. DO NOT EDIT COLUMNS 1 OR 2.

This selection allows you to input the actual HP-IB hardware addresses of the equipment you will use in the performance tests. Each instrument address is assumed to be the recommended default address for the instrument with an HP-IB select code of 7:

Printer	701
Power Meter	713
HP 8753A	716
Spectrum Analyzer	718
Attenuator Driver	728

We recommend you change the address on the instrument itself to comply with these factory recommended defaults. However, if this is not possible, use this menu to edit the program's addresses to match your equipment. When you exit this menu, the changes made will be re-stored to file DEV_CONFG and will be in effect the next time you run the program.

The file DEV_CONFG contains one equipment list for all the tests, so there may be equipment listed in this menu that is not pertinent to the test you are about to run.

If you are using an HP 438A power meter, edit the model number column for the power meter. By default, this column says HP436A. Change this to HP438A (no spaces).

Press **[DONE]** to return to the HP 8753A system configuration menu.

Press **[DONE]** again to invoke the HP 8753A performance test menu.

HP 8753A Performance Test Menu

Select the test you wish to run. The computer will load the subprograms specific to that test. (The computer will expect to find the subprograms at the default MSUS or, if you edited the mass storage configuration screen, at the MSUS you provided for the volume DISC2 FILES.)

Each test provides the same main menu choices: **TESTS** and **RESULTS**.

Tests. This selection invokes the necessary setup routines (such as entering calibration factors, etc,) before leading to a menu which allows the selection of individual tests to be run. The setup routines are as follows:

Power Sensor Calibration Factors: You have two choices in this menu: read calibration data from disc, or enter it from the keyboard. If the program has never been run before, there is no calibration data on disc. Select **KEYBOARD ENTRY/EDIT**.

Enter the calibration data from the power sensor label for the frequencies listed in column one. (Enter calibration factors as percentages, for example: 96.7). Press **[SELECT]** and enter the first calibration factor. To enter the second calibration factor, press **[▼]** and **[SELECT]**. Repeat this process for the entire list.

When values are entered from the keyboard, the program asks if you wish to store the data to disc. If so, you are prompted for the last five digits of the power sensor serial number. Enter the number and press **[RETURN]** or **[ENTER]** to complete the input. The program then stores the data in file "8482Annnnn", where nnnnn is the last five digits of the serial number.

When storing calibration data, the program will attempt to create a file on either the default mass storage unit or the MSUS that you input in the mass storage config edit menu for the volume CALIBRATION DATA. If there is no mass storage at that address, an error will occur.

In later executions of the program, you can read this data file from disc by pressing **READ DISC** to load calibration factors into the program.

Attenuator Calibration Factors. The dynamic accuracy program is the only routine that requires attenuator calibration factors. Enter the actual attenuation value in column two, for all steps of the attenuator. Refer to Power Sensor Calibration Factors, above, for instructions on entering/saving these data.

Equipment Initialization. Just before the test menu is displayed, the appropriate power meter subprograms are loaded and the power meter is zeroed and adjusted. Simply follow the prompts on the screen. Any additional equipment is also preset.

Test Routines. Finally, the test menu is displayed. Tests can be run individually or sequentially without interruption (if the test setups are identical). You can rerun these tests as many times as is necessary without repeating all the previous menus. However, results from the previous run will be overwritten.

Results. This selection leads to the test record menu. All test results can be output to a printer in test record format. Some test results can be output in graphical format. Note that the results menu accesses the HP 8753A network analyzer to obtain the serial number of the unit under test.

You can output results as many times as you wish.

Error Recovery

If an error is detected, it is reported to the user with an explanation of the error and the name of the subprogram that detected the error. The error message screen also provides one or more softkeys. The **[ABORT]** softkey returns you to the most recent major menu. Some error messages provide a **[REPEAT]** softkey. Pressing this key will repeat the routine which just detected the error. This is useful in cases, for example, where an HP-IB cable is missing and a device does not respond to the controller. Connect the cable and press **[REPEAT]**.

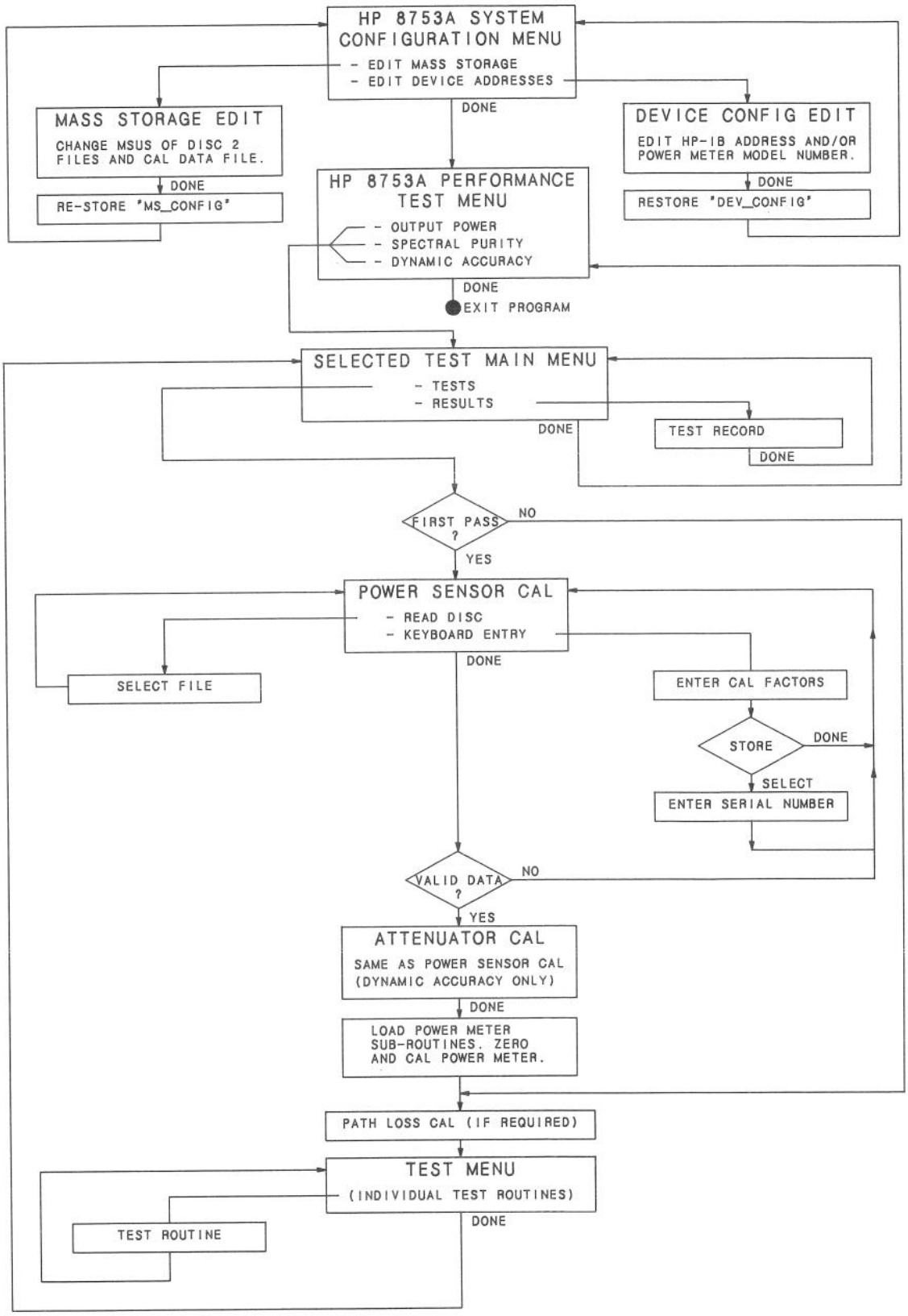


Figure 14. Performance Test Program Flowchart

Output Power

SPECIFICATIONS

Level Accuracy (at +10 dBm output level, 50 MHz)	±0.5 dB
Flatness	±1 dB
Linearity (25°C ±5°C)	
−5 to +15 dBm	±0.2 dB (relative to +10 dBm output level)
+15 to +20 dBm	±0.5 dB (relative to +10 dBm output level)
Range	−5 to +20 dBm

DESCRIPTION

The HP 8753A source power tests include verification of power level accuracy, power level flatness, power linearity and power range.

These tests are preceded by a path loss calibration procedure that stores frequency response data for the power splitter connected between the HP 8753A RF OUT port and the power meter.

Power Level Accuracy

This test measures the actual RF output power level of the HP 8753A when the analyzer is tuned to 50 MHz and the power level has been nominally set to +10 dBm.

Power Level Flatness

Power level flatness is tested at six different power level settings, at various frequency points across the range of the HP 8753A. For example, the power level is first set to −5 dBm. Power meter readings are taken as the HP 8753A CW frequency is tuned to approximately 30 frequencies from 300 kHz to 3 GHz. The power deviation from the nominal power setting is calculated and stored. This procedure is repeated for power levels of 0, +5, +10, +15, and +20.

The peak-to-peak variation is recorded on the test record for each power level tested. Power flatness can also be plotted on Cartesian coordinates with frequency as the x-axis and power variation as the y-axis. The different power level settings are differentiated by line patterns on the graph.

Power Linearity

Power linearity is tested at five CW frequencies (300 kHz, 50 MHz, 1GHz, 2GHz, and 3 GHz). The analyzer is tuned to a test frequency and the power is incremented from −5 to +20 dBm in 1 dB steps. Power is measured at each step with a power meter. For each test frequency, linearity data is normalized to the power reading taken at +10 dBm.

Power Range

The power output range for the HP 8753A is specified as −5 to +20 dBm. Actually, the power can be nominally set from −10 to +25 dBm. This allows the user to overcome power flatness and linearity

variations by setting the power as necessary to obtain a precise power output level at the extremes of the output range.

Power range is reported on the test record as a simple pass or fail. If the test does fail, however, the points that are out of specification are recorded.

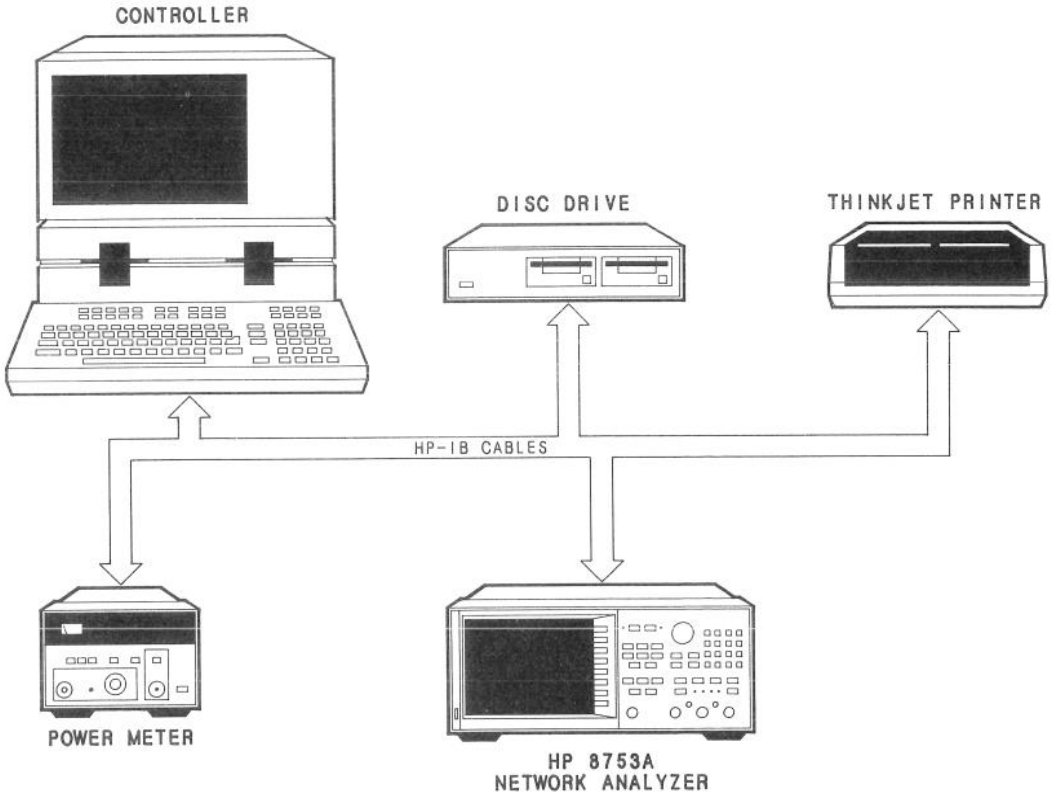


Figure 15. System Configuration for Output Power Tests

EQUIPMENT REQUIRED

Power Meter	HP 436A
Power Sensor	HP 8482A
Power Splitter (2)	HP 11667A Option 001
Attenuator 20 dB (2)	HP 8491A Option 020
Cable Set	HP 11851B

PROCEDURE

1. Connect equipment as shown in Figure 15.
2. Refer to GETTING STARTED at the beginning of this section for instructions on loading the BASIC system and the performance test software. Use GETTING STARTED to work your way through the HP 8753A System Configuration Menu.

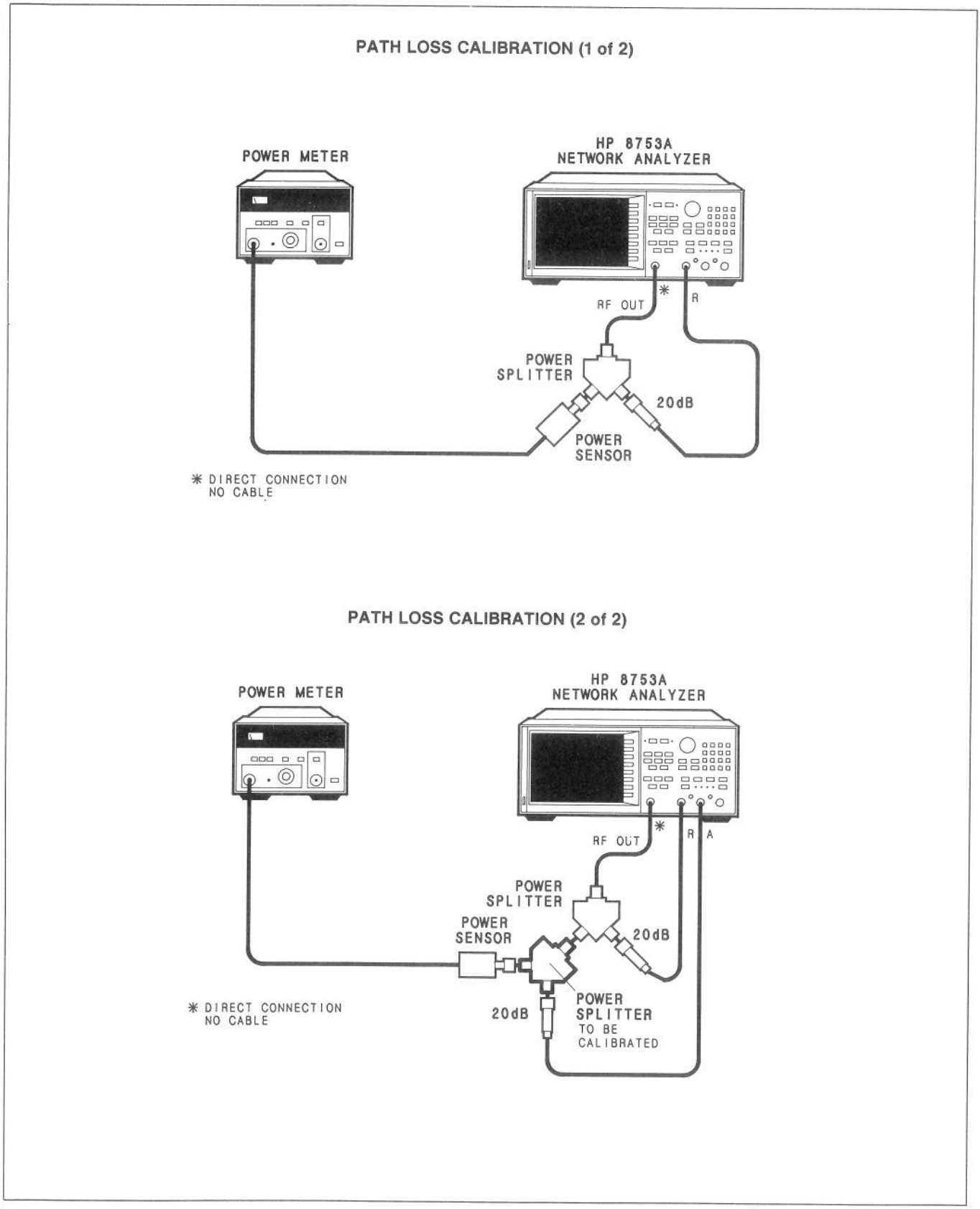


Figure 16. Output Power Path Loss Calibration Setups

3. From the HP 8753A performance test menu, select **Output Power**. The program will perform setup routines such as asking for power sensor calibration factors. Refer to GETTING STARTED and follow the instructions for this menu.

4. From the output power tests menu, select an individual test or select **ALL TESTS** to run all test routines sequentially without interruption. The first routine selected will invoke the path loss calibration routine. Follow the prompts. They will refer to test setup illustrations on the following pages.

5. You can iterate the tests as many times as you like without repeating the path loss calibration, as long as you do not terminate the output power test subprogram or change the actual device connections between the HP 8753A and the power meter.

6. Press **[DONE]** when the tests are finished. Now select **RESULTS** to output the test data to the printer. This test also provides plots of power flatness and linearity.

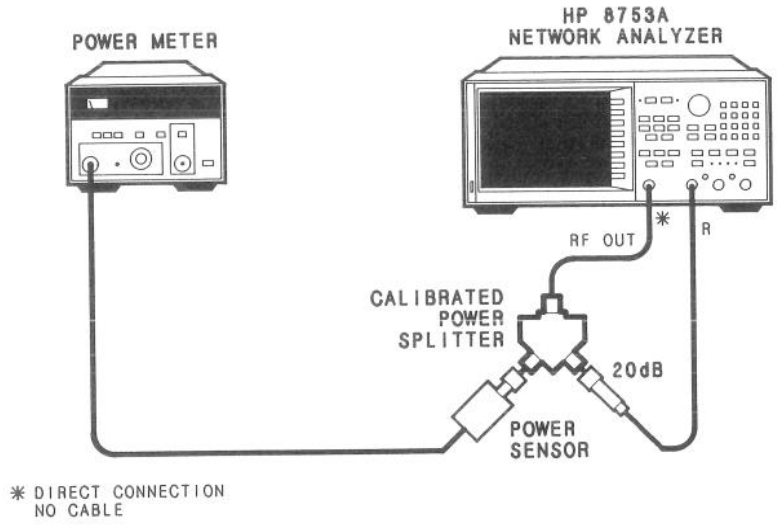


Figure 17. Output Power Performance Test Setup

IN CASE OF DIFFICULTY

Ensure that the power meter and power sensor are operating to specification. Inspect the power splitter connectors. Poor match at these connections can generate power reflections that can cause the HP 8753A to appear to be out of limits.

Likewise, inspect the HP 8753A RF OUT connector for damage.

The source relies on internal correction routines for its high accuracy performance. If any test fails, refer to the Adjustment and Correction Constants section of this manual and perform the RF Output Power Correction Constants routine.

If you encounter a catastrophic source failure, refer to source group troubleshooting in the service section.

Spectral Purity

SPECIFICATIONS

(With 0 to −10 dBm into the R input)

Harmonics	
(at +20 dBm output level)	−25 dBc
Non-Harmonics	
Mixer-related	
(at +20 dBm output level)	−32 dBc
Other Spurious Signals	
(frequency < 135 MHz)	−60 dBc
(frequency ≥135 MHz)	[−60 + 20 log(f/135 MHz)] dBc
Phase Noise	
(10 kHz offset from fundamental in 1 Hz bandwidths)	
(frequency < 135 MHz)	−90 dBc
(frequency ≥ 135 MHz)	[−90 + 20 log(f/135 MHz)] dBc

DESCRIPTION

The spectral purity tests measure several phenomena that may appear in the output spectrum of the HP 8753A. Each of these phenomena is described and the test method explained.

All measurements are made using the 10 MHz timebase reference from the spectrum analyzer connected to the EXT REF INPUT of the HP 8753A. With this configuration, both the spectrum analyzer and the network analyzer are phase locked to the same reference frequency which should ideally eliminate frequency offset errors. (If the two analyzers are not phase-locked, the tests will run, but measurements may be invalid.)

Path Loss Calibration

This is not an HP 8753A performance specification but an ancillary routine that determines the frequency response of the power splitter between the HP 8753A RF OUT port and the power meter. Some of the spectral purity performance parameters are specified at +20 dBm output level. In order for power to be set accurately, the path loss to the power meter must be known.

Harmonics

This routine measures the in-band second and third harmonics of the HP 8753A with the power level of the fundamental at +20 dBm.

The HP 8753A's output power variations and the HP 8566 spectrum analyzer's frequency response are avoided using the following measurement technique. To measure the level of the second harmonic of frequency F, the HP 8753A is set to a CW frequency of 2F. The power is set with the power meter to a level of +20 dBm (minus the path loss). The spectrum analyzer is also tuned to a center frequency of 2F, and the amplitude level of the signal is recorded. This provides a +20 dBm reference level at the spectrum analyzer.

The HP 8753A is then tuned to a frequency of F. The output power is adjusted, if necessary, to +20

dBm. The spectrum analyzer is still tuned to a center frequency of 2F and is therefore measuring the second harmonic of the HP 8753A. The relative harmonic level is calculated by subtracting the +20 dBm reference level from the amplitude level of the second harmonic.

This routine is repeated until the list of test frequencies is exhausted. Third harmonics are tested in the same way, but the +20 dBm reference is established with the HP 8753A set to a CW frequency of 3F. (By setting the reference on the spectrum analyzer at the frequency at which you expect to measure the harmonic, you avoid the spectrum analyzer frequency response error.)

Non-Harmonics

This specification is separated into two main categories: mixer spurs and other spurious signals.

Mixer Spurs. Mixer spurs are generated by the heterodyne process in the A3 source module. Because these spurs are generated in part by the cavity oscillator which resides in the leveling control loop, they are power level dependent. Note they are specified at maximum power level.

These spurs are unwanted products of the mixing process and appear at the sum and difference frequencies of the multiples of the cavity oscillator (F_{cav}) and the YO (F_{yo}). The performance test measures the level of the 2:1 spur and the 3:2 spur. A 2:1 spur is a signal that exists at $2(F_{cav})$ plus or minus F_{yo}. (Spurs at the sums of these two frequencies always occur at frequencies greater than 3 GHz. The HP 8753A specifies the level of in-band impurities only, therefore this routine measures only the difference frequencies.) Likewise, the 3:2 spur is measured at the difference frequency $3(F_{cav})$ minus $2(F_{yo})$.

To accurately calculate the frequency at which these spurs will appear, the exact cavity oscillator frequency must be known. This frequency, nominally 3.8 GHz, is determined by setting the HP 8753A output to a specific CW frequency, and then locating the 2:1 spur. Once the spur frequency is known, the actual cavity oscillator frequency can be algebraically calculated: $F_{cav} = (F_{yo} + F_{spur})/2$.

Spur levels are measured with the same technique described for harmonics. A +20 dBm reference is set on the spectrum analyzer with the HP 8753A set to the calculated spur frequency. Then the frequency of the HP 8753A is changed to the fundamental frequency, and the level of the spur is measured.

Other Spurious Signals. This category includes all other impurities that may appear in the output spectrum. These signals are not power level dependent because the generating mechanism is not in the leveling loop of the source.

An interesting characteristic of these spurs is that the level is frequency dependent. Most of these spurs are generated in the fractional-N synthesizer loop. This loop is the master VCO signal for the HP 8753A. In simplified terms, the fractional-N VCO sweeps from 30 to 60 MHz (or a subset thereof) to generate each of the sub-bands of the HP 8753A. Harmonic mixing translates the stable low frequency VCO signals via the phase-locked loop to the HP 8753A RF output frequencies.

The frequency translation process multiplies the FM-sidebands in the fractional-N VCO output as well as the fundamental. The amplitude relationship of the sideband to the fundamental is proportional to the modulation index:

$$A_{sb} = \frac{1}{2} (\Delta F / F_{mod})$$

where A_{sb} is the sideband amplitude, delta F is the peak deviation of the frequency modulation, and F_{mod} is the rate of modulation. As the HP 8753A RF output frequency increases, the harmonic number used in the sampling process increases, and therefore the peak deviation increases. The modulation frequency, however, remains the same. (This is the mechanism that generates the spur; for example, modulation by the 100 kHz fractional-N reference.) Therefore A_{sb} increases.

Since the level of spurious signals generated in the synthesizer maintains a linear relationship with the output frequency, the spectrum is tested in one band only (band 7, harmonic multiple = 9). If the spur level is acceptable in the tested band, the effective spur levels in any other band (caused by the same mechanism) are assumed to be within specification.

The following spur-causing mechanisms are tested.

API SPURS. The fractional-N loop incurs a phase error as a result of its divide-by-N process. For any frequency containing a fractional part (F/100 kHz), the VCO will gain in phase with each 100 kHz reference cycle. This error is predictable and repeatable and can therefore be compensated. This is the task of the analog phase interpolators. These circuits generate a negative current proportional to the fractional number, to siphon current away from the VCO drive signal and correct for the phase error.

The side effect of this technique is low-level modulation of the fractional-N VCO frequency when the API currents turn on and off. The level of the API spur is somewhat dependent on the value of the fraction (fractional part of the output frequency). The fractional numbers used in the API spur test are 857 for high band and 433 for midband. The test measures the API spur and its second, third, and fourth harmonics. A test frequency is generated as follows:

RF output = 9(frac-N carrier frequency + API number) + 1 MHz

spectrum analyzer center frequency = RF output + API number x harmonic

The RF output frequency is obtained by taking an integer fractional-N carrier frequency, such as 45 MHz, adding the fractional API number (857), multipying that sum by 9 to arrive at the band 7 RF output frequency and adding 1 MHz because the fractional-N trails the actual RF output by 1 MHz (first LO). The output frequency in this case would be 406.007713 MHz. The performance test uses the spectrum analyzer to examine the spectrum at multiples of the API number away from the output frequency (see test record for test frequencies).

100 kHz SPURS. The reference frequency for the fractional-N circuit is 100 kHz. The test looks for 100 kHz and 200 kHz (second harmonic) sidebands at several frequencies in band 7.

IF SPURS. This routine measures 4 kHz and 8 kHz sidebands on the RF output frequency. These spurs occur in low band only and are generated on the A12 reference board. The source of the spur is the 40 MHz crystal reference mixing with the 39.996 MHz VCO. The test is performed at 10 MHz only.

SOURCE CROSSING SPURS. These spurs are caused by intermodulation effects in the limiter circuit, which interfaces the A12 reference board phase lock reference signal to the phase lock detector on the A11 phase lock board.

This spur is generated in low band, where a multiple of the 40 MHz crystal reference and a harmonic of the actual .300 to 16 MHz RF signal combine to produce a spur at the same frequency as the RF output signal.

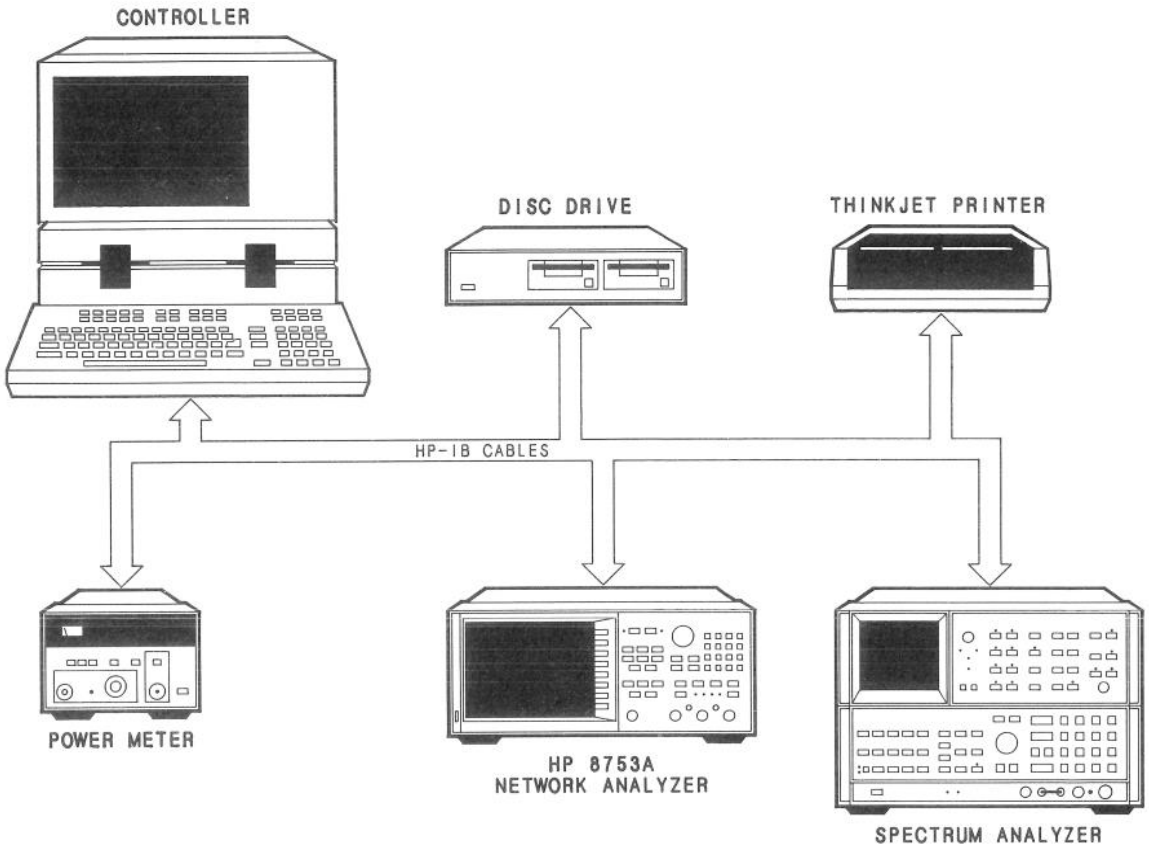


Figure 18. System Configuration for Spectral Purity Tests

EQUIPMENT REQUIRED

Spectrum Analyzer	HP 8566A/B
Power Meter	HP 436A
Power Sensor	HP 8482A
Power Splitter (3-way)	HP 11850C
Power Splitter (2-way)	HP 11667A
Attenuator 20 dB	HP 8491A Option 020
BNC Cable	HP part number 8120-1840

PROCEDURE

1. Connect equipment as shown in Figure 18.
2. Refer to GETTING STARTED at the beginning of this section for instructions on loading the BASIC system and the performance test software. Use GETTING STARTED to work your way through the HP 8753A System Configuration Menu.
3. From the HP 8753A performance test menu, select **Spectral Purity**. The program will perform setup routines such as asking for power sensor calibration factors. Refer to GETTING STARTED and follow the instructions for this menu.

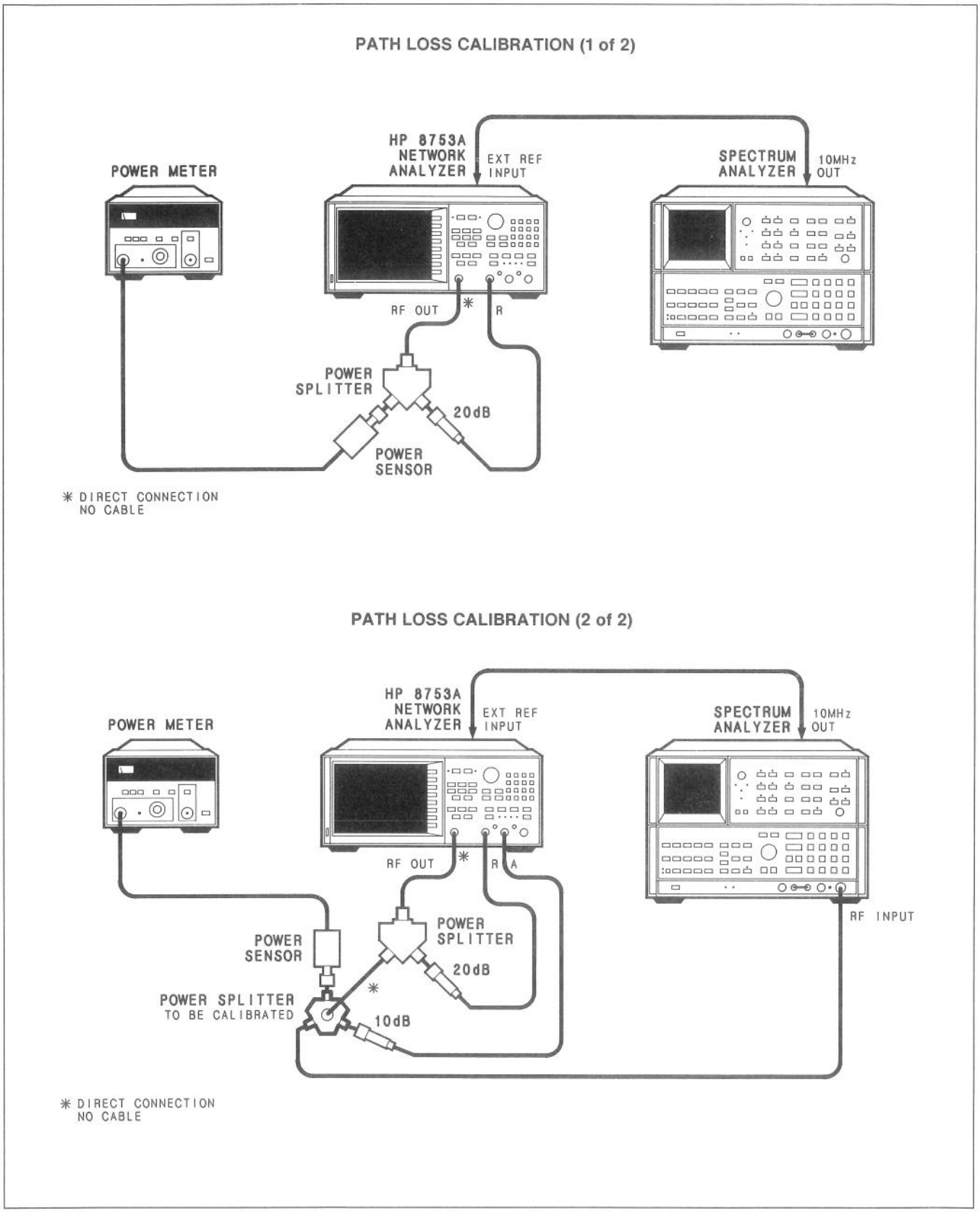


Figure 19. Spectral Purity Path Loss Calibration

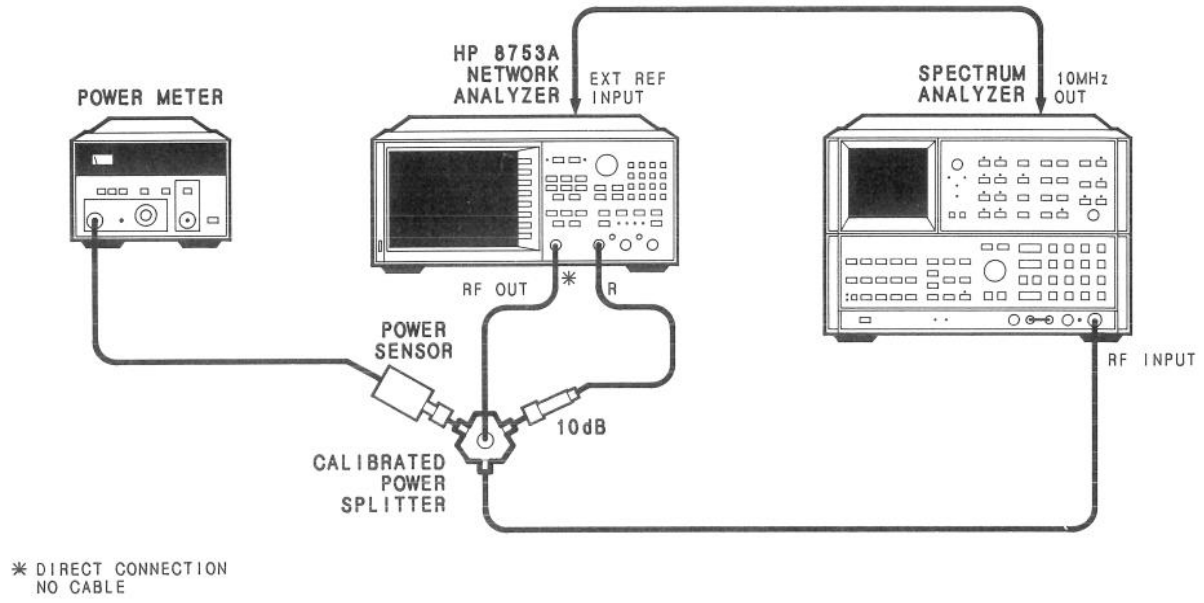


Figure 20. Spectral Purity Test Setup

4. From the spectral purity tests menu, select an individual test or select **ALL TESTS** to run all test routines sequentially without interruption. The first routine selected will invoke the path loss calibration routine. Follow the prompts. They will refer to test setup illustrations contained in this procedure.

5. You can iterate the tests as many times as you like without repeating the path loss calibration, as long as you do not terminate the spectral purity subprogram or change the actual device connections between the HP 8753A and the spectrum analyzer or the power meter.

6. When you are finished with the tests, press **[DONE]** to return to the spectral purity main menu. From here you can select the **RESULTS** menu and print out the test results on the system printer.

IN CASE OF DIFFICULTY

If any test fails, put both the HP 8753A and the spectrum analyzer in local mode and tune each device to the frequency in question. Manually verify that the signals are out of tolerance.

Ensure that any spurious response is not generated by the spectrum analyzer itself. This can be verified by increasing the spectrum analyzer attenuation and observing any change in spur level. If the spur is caused by overdriving the spectrum analyzer input mixer, the effective spur level (dBc below the carrier) will drop with increased attenuation.

Read through the description at the beginning of this test to discover where the out of tolerance signal is being generated. Primarily, harmonics and mixer spurs are a function of the A3 source module. API spurs and 100 kHz spurs are generated in the fractional-N module. IF spurs and low band source crossing spurs are generated on the A12 reference board.

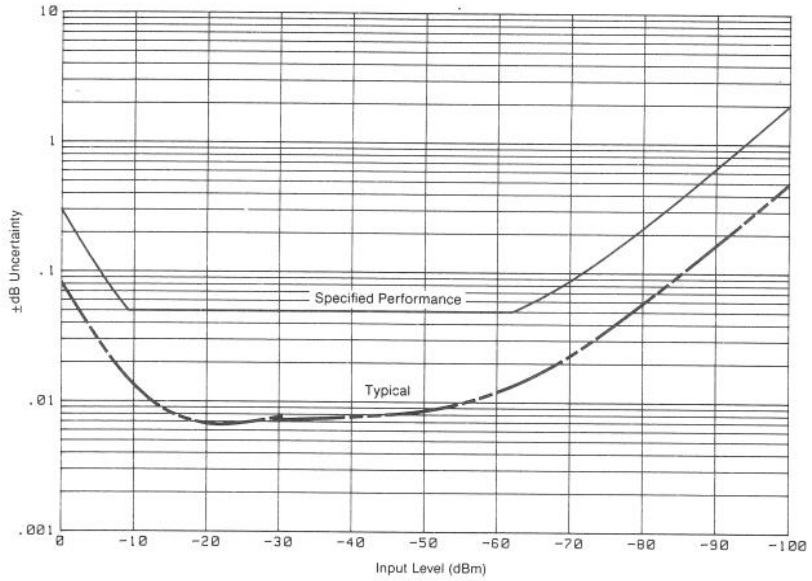
Dynamic Accuracy

SPECIFICATION

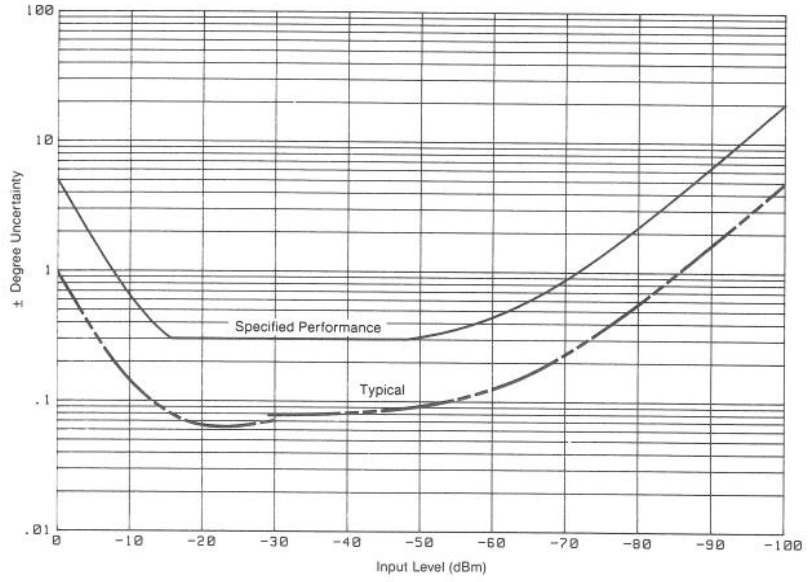
Dynamic Range

Inputs A, B	100 dB
Input R	35 dB

Magnitude Dynamic Accuracy (Inputs A, B, (R to −35 dBm); 10 Hz bandwidth):



Phase Dynamic Accuracy (A/R, B/R, A/B (R to −35 dBm); 10 Hz bandwidth):



DESCRIPTION

Dynamic accuracy is a measure of how well the receiver measures the magnitude and phase components of a signal as that signal varies in amplitude over the specified dynamic range. In this case, the power is varied from −10 to −100 dBm by inserting known attenuation values in the receiver path.

Because dynamic accuracy is a function of the 4 kHz IF processing, magnitude dynamic accuracy measurements are made at a single CW frequency of 30 MHz. Phase dynamic accuracy measurements are made at 3 MHz, where there is less phase error contribution by the individual attenuator segments.

Signal compression and expansion in the RF input samplers impact the dynamic accuracy performance of the receiver at higher power levels. The magnitude of this effect is frequency dependent, therefore compression is tested on all inputs at frequencies of 50 MHz, 1 GHz, 2 GHz, and 3 GHz. For these tests, the attenuator is removed, and input power is manipulated with the HP 8753A output power controls and the power meter.

NOTE: This test allows the use of either a manual or programmable HP 8496A/G attenuator. If the HP 8496G programmable version is used, the HP 11713A attenuator/switch driver module is required to actuate the attenuator upon command from the controller.

NOTE: When receiver performance is measured against a known standard (attenuator), the calibration uncertainty of the standard becomes the primary source of error in the measurement. Hewlett-Packard recommends that attenuators used for this test be calibrated to within 0.03 dB for the 10 through 60 dB steps. This calibration can be obtained from Hewlett-Packard's Loveland Division Standard's Laboratory:

Hewlett-Packard
Loveland Division
815 14th Street S.W.
Loveland, Colorado 80537

EQUIPMENT REQUIRED

Power Meter	HP 436A
Power Sensor	HP 8482A
Power Splitter (3-way)	HP 11850C
Power Splitter (2-way)	HP 11667A Option 001
100 dB Step Attenuator	HP 8496A/G
Attenuator Driver (for HP 8496G only)	HP 11713A
Attenuator Drive Cable (for HP 8496G only)	HP part number 8120-2703
Attenuator 30 dB	HP 8491A Option 030
50 ohm Termination	HP 908A
Cable Set	HP 11851B
Adapter, Type N (f) to Type N (f)	HP part number 1250-1472
Adapter, Type N (m) to Type N (m)	HP part number 1250-1475

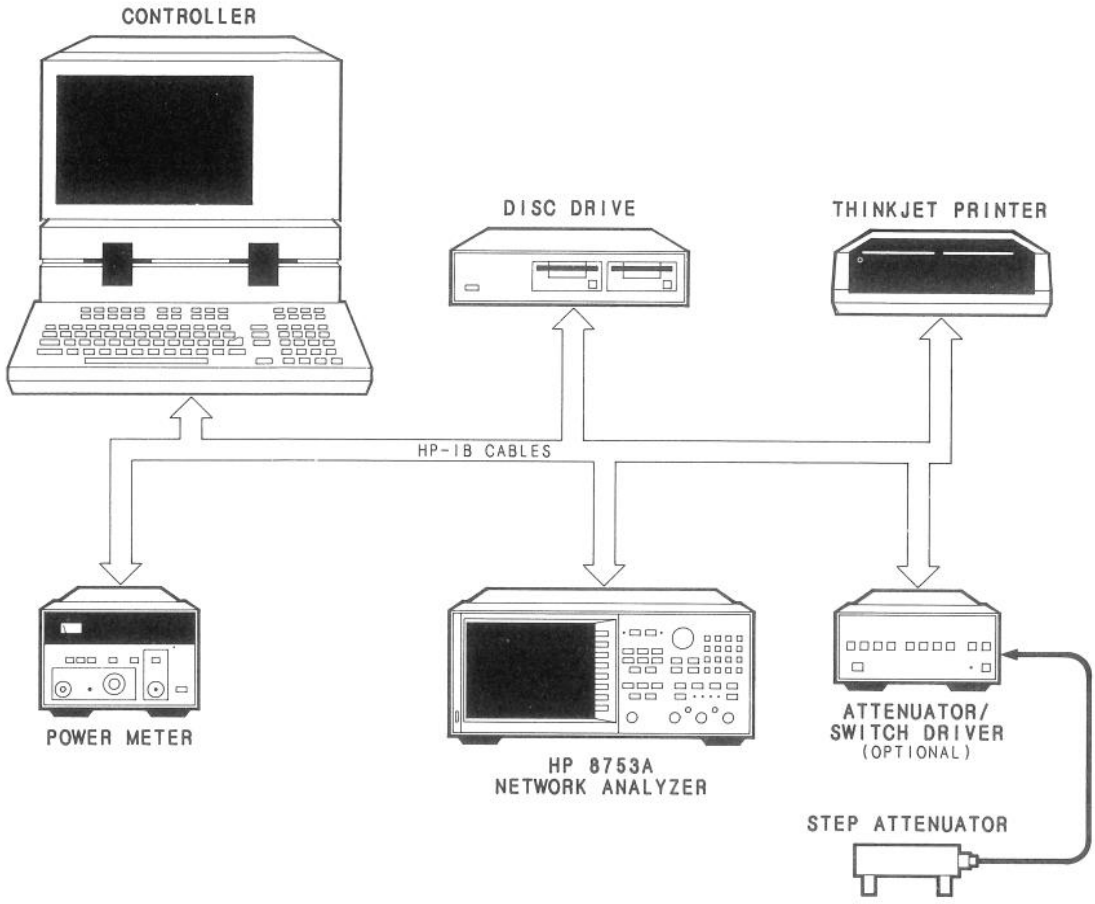


Figure 21. System Configuration for Dynamic Accuracy Tests

PROCEDURE

1. Set up equipment as shown in Figure 21. When using a manual attenuator, HP 8496A, eliminate the HP 11713A attenuator/switch driver. When using a programmable attenuator, HP 8496G, the HP 11713A is required. The program looks for the HP 11713A. If it is not on the HP-IB bus, the program assumes the use of a manual attenuator and will prompt the operator to change the attenuation step at the appropriate time.

2. Refer to GETTING STARTED at the beginning of this section for instructions on loading the BASIC system and the performance test software. Use GETTING STARTED to work your way through the HP 8753A System Configuration Menu.

3. From the HP 8753A performance test menu, select **Dynamic Accuracy**. The program will perform setup routines such as asking for power sensor and attenuator calibration factors. Refer to GETTING STARTED and follow the instructions for this menu.

4. When you arrive at the HP 8753A Dynamic Accuracy Tests Menu, you must select among individual tests. Each test requires a different setup.

   NOTE: The low power measurements made during this test are extremely sensitive to crosstalk. Configure the test setups as shown taking care to separate RF cables to avoid crosstalk paths.

   NOTE: The cables in Figure 24 are numbered 1 through 3 in **INITIAL SETUP**. Cable number 2 is not used in the **MEASUREMENT SETUP**. These cable numbers are intended to clarify which specific cable is to be removed.

   NOTE: The test configurations titled Initial Setup are used to set the power level of the HP 8753A precisely. This is a low level measurement that requires a long settling time from the power meter ($\cong$10 seconds). Be patient. If the power meter does not settle in the time that routine allows, an error message will be displayed. Press **[REPEAT]** to run that routine again. If the power meter still does not settle, check your test setup.

   You may execute the tests in any order. The order in which they appear in the test menu requires the least number of test setup changes from test to test.

5. Tests may be repeated as many times as you wish.

6. Press **[DONE]** to return to the dynamic accuracy test main menu. Select **RESULTS** to output the test data. This test provides output in tabular format (test record) and also provides data plots for each input, similar to the plots used in the specification (see Specification above).

IN CASE OF DIFFICULTY

Noise and crosstalk can severely impact the measurement of very small signals. Always repeat a failed test, paying careful attention to the test setup connections and the lay of the cables. Verify that attenuator values are input correctly and that the attenuator calibration is current.

If an input fails in the compression region (−10 to 0 dBm input), suspect the associated input sampler. Verify that the power meter and power sensor are working properly.

Failures at lower power levels are usually due to the A10 digital IF board. Dynamic accuracy error is largely due to non-linearities in the analog-to-digital converter (ADC) and preceding gain stages. The A, B, and R input signals follow individual IF paths (gain stages). However, all inputs are digitized by a multiplexing ADC. Non-linearities in the ADC impact all inputs, whereas non-linearities in the gain stages impact the associated input only. Refer to the Adjustment and Correction Constants section and perform the Analog-to-Digital Linearity Correction Constant routine and the IF Amplifier Correction Constant routine.

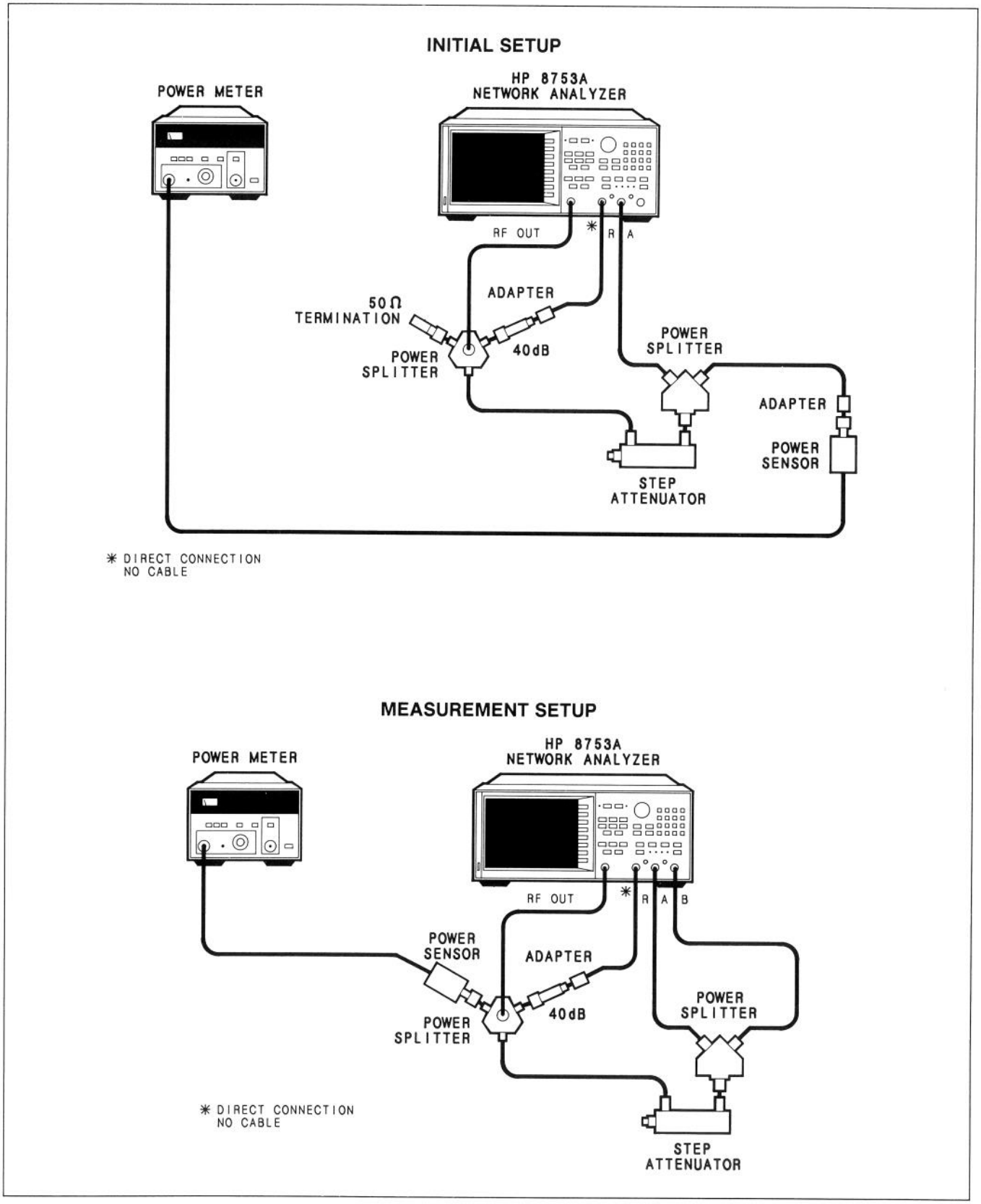


Figure 22. Low Level Magnitude Dynamic Accuracy; Inputs A and B

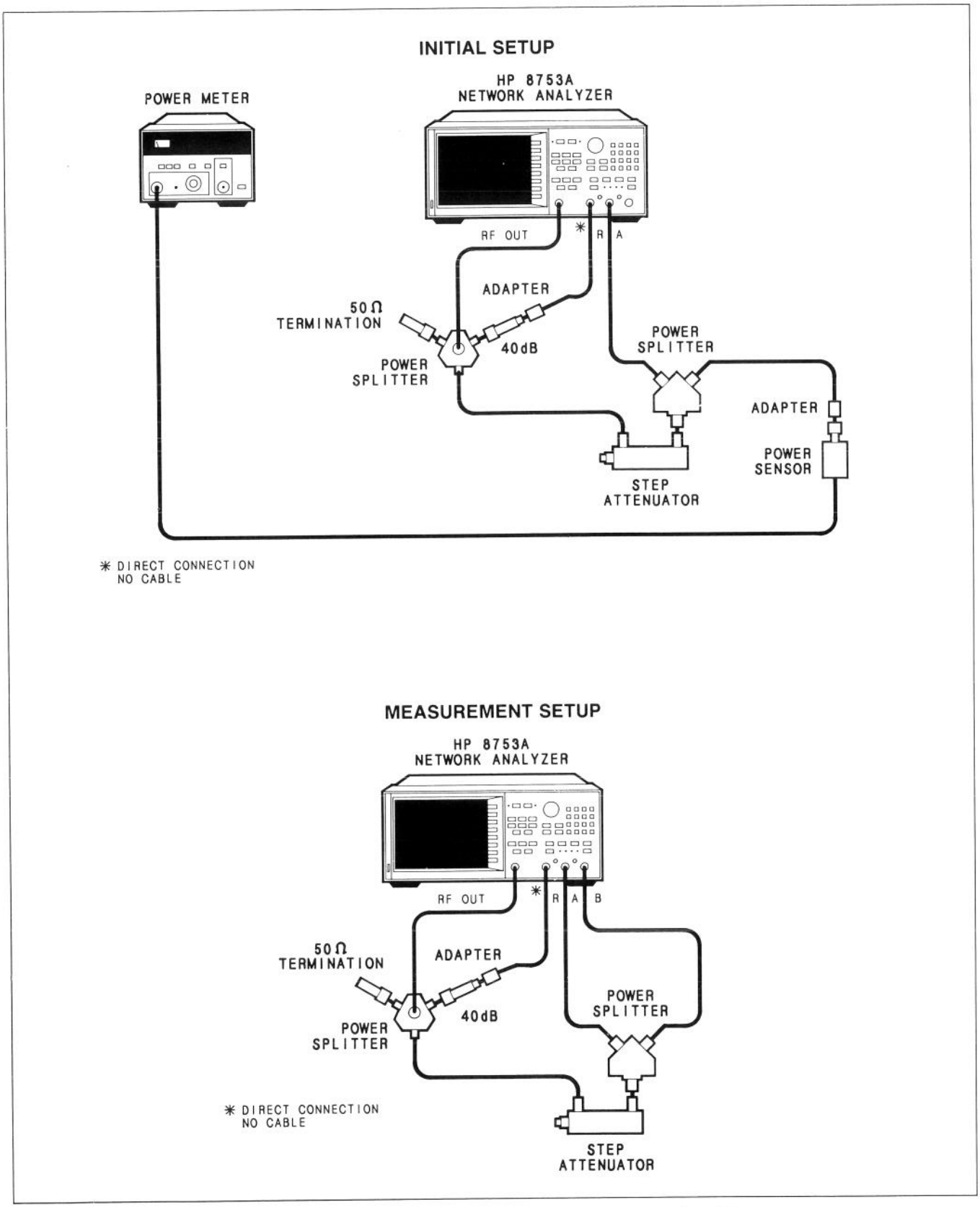


Figure 23. Low Level Phase Dynamic Accuracy; Inputs A and B

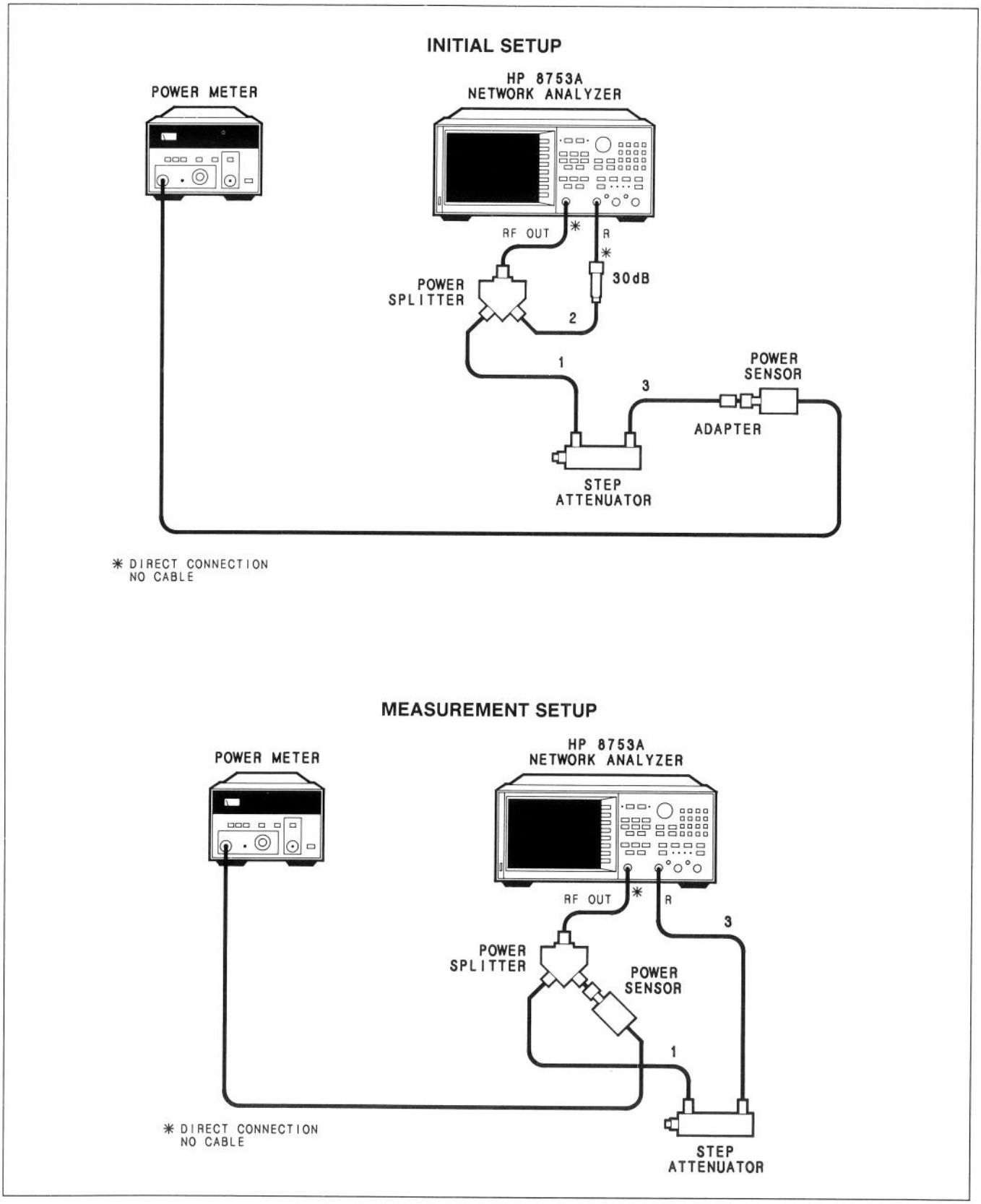
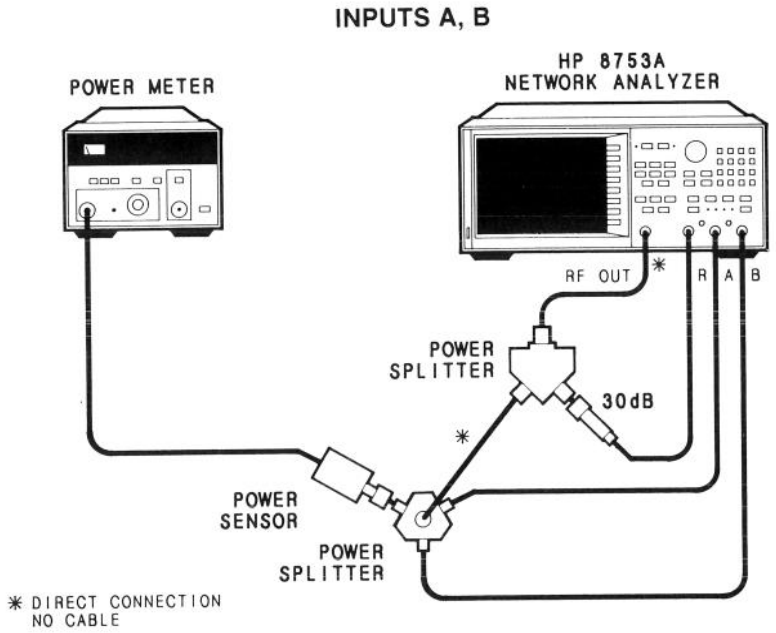


Figure 24. Low Level Magnitude Dynamic Accuracy; Input R



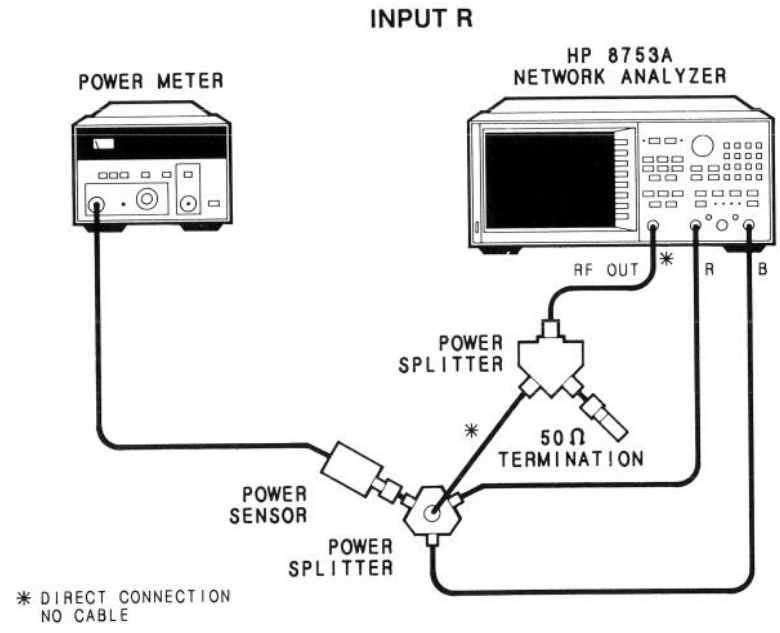


Figure 25. High Level Dynamic Accuracy

Adjustments and Correction Constants

INTRODUCTION

The accuracy of the HP 8753A is achieved and maintained through mechanical adjustments and correction constants. The mechanical adjustments include inductors, potentiometers and capacitors. The correction constants are empirically derived data stored in memory and recalled as required to refine the instrument's measurements of power and phase and to define its operation.

For example, the output power correction constants result from comparisons of power measured by a power meter and set by the network analyzer itself. If the HP 8753A measures a power level 0.03 dB less at 50 MHz than the power meter, for instance, the analyzer stores a correction constant of +0.03 dB at 50 MHz. Not every frequency between 300 kHz and 3 GHz is measured to generate a correction constant. For frequencies without stored correction constants, correction factors are automatically interpolated as required from the stored correction constants. Thus amplitude and phase accuracy is enhanced across the entire frequency band.

Some of the correction constants, like the display intensity and focus correction constants, affect the HP 8753A's operation only and require no equipment or output signal to be generated. Some of the correction constants are generated by internal routines and require only a signal to the R input for phase lock. Other semi-automated correction constant routines require more extensive instrumentation and operator participation.

All of the correction constants are stored in EEPROM on the A9 CPU board. Thus, any time the CPU board is replaced, all of the correction constants must be regenerated and stored on the new board. Refer to the table of Related Service Procedures in the Troubleshooting Reference to see when specific correction constants must be regenerated.

A list of recommended test equipment is provided in the General Introduction section. Other equipment may be used as long as it meets or exceeds the critical specifications listed.

ORDER OF ADJUSTMENTS

This is the order of the adjustment and correction constants procedures:

Display Intensity and Focus Correction Constants
Display Image Size, Position and Trace Alignment Adjustment
Serial Number Correction Constants
Option Numbers Correction Constants
Analog Bus Correction Constants
ADC Linearity Correction Constants
Fractional-N Frequency Range Adjustment
Source Pretune Correction Constants
Frequency Accuracy Adjustment
High/Low Band Transition Adjustment
Fractional-N Spur and FM Sideband Adjustment
Source Spur Avoidance Tracking Adjustment
Sampler Diode Bias Adjustment
Sampler Magnitude and Phase Correction Constants
RF Output Power Correction Constants
IF Amplifier Correction Constants
Cavity Oscillator Correction Constants

CORRECTION CONSTANT JUMPER POSITION

To guard against inadvertant correction constant changes, the A9 CPU board includes a jumper which must be in the correct position to enable the HP 8753A to load new correction constants in memory. The instrument is shipped with the jumper in the no-load position. This position is recommended for normal operation.

Figure 1 shows the lower (no-load) and upper (load) position of the jumper on the A9 CPU board. The message "Correction constants not stored" at the end of a correction constant routine means that the correction constant jumper was in the lower (no-load) position. Perform the following procedure to change the position of the jumper.

Jumper Reposition Procedure

NOTE: Turn off power before removing or installing boards.

1. Remove the top cover of the HP 8753A by unscrewing the upper rear panel feet, loosening the captive screw in the middle of the rear edge of the cover and sliding the cover back and off.
2. Remove the PC board stabilizer (a plastic bar) by loosening the screw, carefully pulling up the left end of the bar, and pivoting it off the boards.
3. Remove the A9 CPU board by pulling upward on its white extractors and lifting the board out of its cavity. See the Location Diagram on the underside of the top cover.

4. Pull the jumper off the pins in the lower position and push it on the upper position pins as shown in Figure 1 to enable the instrument to load correction constants.
5. Replace the A9 board in its cavity. Make sure that all of the pins on the lower edge are engaged and that it is seated securely.
6. Replace the top cover and run the correction constant routine(s) as required.
7. Reverse this procedure when finished loading correction constants.

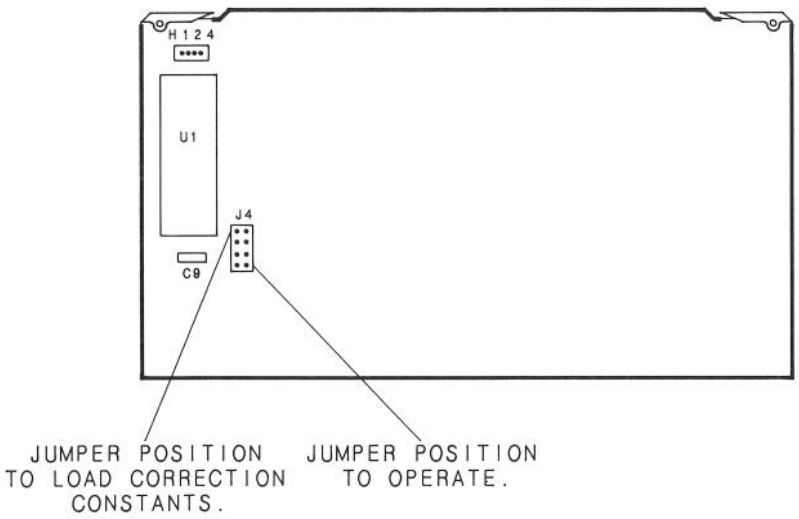


Figure 1. Correction Constant Jumper Location.

DISPLAY INTENSITY AND FOCUS CORRECTION CONSTANTS

NOTE: When installing a display in the HP 8753A, immediately check the power supply voltages as outlined in the Service section.

DESCRIPTION

This procedure stores the intensity and focus settings as correction constants. Both settings are adjusted through the front panel controls for values of 0% through 100%. Intensity, for example, is minimum at 0% and maximum at 100%.

EQUIPMENT

None

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper position as explained in "Correction Constant Jumper Position."

1. Turn on the instrument, press **[PRESET]** and allow 5 minutes warm-up time.
2. In the RESPONSE area of the front panel, press **[DISPLAY]** and **[MORE]** (bottom softkey) to access the CRT adjustment menu. The top five softkeys (which may not be legible) are:

   [SPLIT DISPLAY ON off]
   [BEEP DONE ON off]
   [BEEP WARN on OFF]
   [INTENSITY]
   [FOCUS].

3. Press **[INTENSITY]** (fourth softkey from the top) and rotate the RPG knob clockwise to increase the intensity of the display; counterclockwise, to decrease.
4. Press **[FOCUS]** (fifth softkey from the top) and rotate the RPG knob for best focus.
5. Because the intensity and focus adjustments are slightly interactive, repeat steps 3 and 4 as required.
6. Press **[SYSTEM] [SERVICE MENU] [TESTS] [4] [9] [x1]** to access the Focus and Intensity Correction Constant routine. The display should show "Foc/Int Cor".

7. Press **[EXECUTE TEST]** to begin the routine.
8. Press **[YES]** at the prompt to store the intensity and focus correction constants.
9. The display should now indicate "Foc/Int Cor: DONE". This concludes the intensity and focus adjustments.

DISPLAY IMAGE SIZE, POSITION AND TRACE ALIGNMENT ADJUSTMENT

DESCRIPTION

The horizontal and vertical gain and position adjustments are made with four potentiometers on the A18A1 board. The trace alignment potentiometer is on the same board, as shown in Figure 2. This board is located underneath the CRT and is accessible by removing the HP 8753A bottom cover. To perform any other display adjustments, refer to the HP 1349A/D operating and service manual

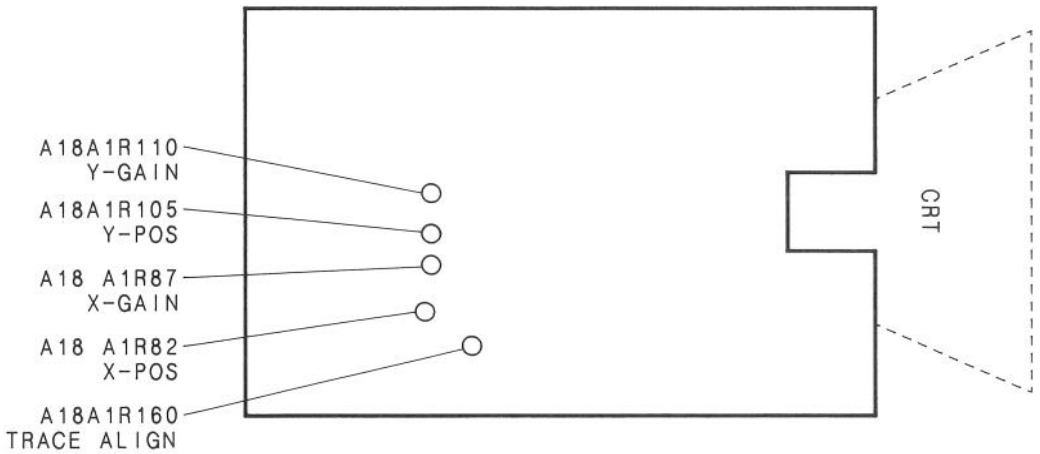


Figure 2. Gain, Position and Alignment Adjustment Locations.

PROCEDURE

1. Turn on the HP 8753A, press **[PRESET]** and allow five minutes for warm-up.
2. The initial screen should show a measurement display area 13.5 cm (5.25 in) wide and 11.4 cm (4.5 in) high. The display area should not be centered on the screen because the notations which appear on the four sides of the measurement display area differ in size. The display area should appear level, not slanted.
3. If you can read all of the screen notations and if the measurement display area is the proper size and not slanted (see step 2), no adjustments for image position, size or alignment are required.
4. To reposition, resize or align the display image, turn off the instrument and remove the top cover and the A9 CPU board. Position the HP 8753A on its left side and remove the bottom cover. Turn on the instrument.

5. The CRT should display a primary test pattern 17 cm (6.75 in) wide and 12 cm (4.75 in) high, centered on the screen and level. If it does not, make the following adjustments as required:

Reference Designator	Adjustment Name	Description
A18A1R110	Y-gain	adjust for a 12 cm high display
A18A1R105	Y-position	adjust to vertically center image
A18A1R87	X-gain	adjust for a 17 cm wide display
A18A1R82	X-position	adjust to horizontally center image
A18A1R160	trace align	adjust for level image

6. When done with these adjustments, turn off the instrument, replace the bottom cover, reinstall the A9 board, and replace the top cover. This concludes the adjustment procedures for the display.

7. If the adjustments can not be done, refer to the Service section.

SERIAL NUMBER CORRECTION CONSTANT

DESCRIPTION

The serial number of the HP 8753A is stored as a correction constant in EEPROM on the A9 CPU assembly. Performing this procedure customizes the replacement A9 CPU assembly by storing the instrument's unique serial number on it.

Perform this procedure *only* if the A9 CPU assembly has been replaced.

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper (load) position as explained in "Correction Constant Jumper Position."

1. Turn on the instrument and press **[PRESET]**.
2. Press **[MENU] [TRIGGER MENU] [HOLD] [ENTRY OFF]** to put the instrument in the hold mode and clear the display.
3. Note the ten character serial number on the identification label on the rear panel of the HP 8753A.
4. Press **[DISPLAY] [MORE] [TITLE] [ERASE TITLE]** to access the title menu and erase the HP logo. Rotate the knob to position the arrow below the first character of the serial number of the instrument. Then press **[SELECT LETTER]** to enter that character. Repeat for each character in the serial number. You *must* enter a total of ten characters: four digits, one letter, and five final digits.

   CAUTION

   Carefully examine the serial number entered. It must be an exact duplicate of the serial number on the instrument's rear panel. The instrument can perform this procedure only once. Mistakes can not be corrected after successfully performing step 6.

   Press **[BACKSPACE]** or **[ERASE TITLE]** to correct errors. When the title is complete and correct, press **[DONE]**.
5. Press **[SYSTEM] [SERVICE MENU] [TESTS] [5] [5] [x1]** to access the serial number save routine. When the display shows "Serial Cor", press **[EXECUTE TEST]** to run the routine.
6. Press **[YES]** at the prompt to alter the correction constant.

7. The test status indicator "DONE" signals the successful conclusion of this correction constant procedure.

8. If this procedure did not end with "DONE", either the serial number entered did not conform to the required format or a valid serial number was already stored. In either case, press **[DISPLAY] [MORE] [TITLE]** to examine the serial number which appears in the title area of the display. If the number is correct, no further action is needed. If the number is incorrect, repeat this procedure. Contact HP if you are still unable to enter the correct serial number.

OPTION NUMBERS CORRECTION CONSTANT

DESCRIPTION

Special information is stored on the A9 CPU assembly of instruments with Option 010 (time domain). It is crucial for the time domain feature to function. Thus if the A9 assembly ever needs to be replaced, this procedure must be performed to customize the replacement assembly to the host instrument.

Perform this procedure *only* if
(1) the instrument has option 010 (time domain) and
(2) the A9 CPU assembly has been replaced and
(3) the Serial Number Correction Constant procedure has been performed.

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper (load) position as explained in "Correction Constant Jumper Position."

1. Call your local HP Sales and Service office to obtain the option registration number for your HP 8753A. Be prepared to tell HP the correct, full serial number on the rear panel of the instrument.

2. Turn on the instrument and press **[PRESET]**.

3. Press **[MENU] [TRIGGER MENU] [HOLD] [ENTRY OFF]** to put the instrument in hold mode and clear the display.

4. Press **[DISPLAY] [MORE] [TITLE] [ERASE TITLE]** to access the title menu and erase the HP logo. Then rotate the knob to position the arrow below the first character of the option registration number. Press **[SELECT LETTER]** to enter that character in the title area of the display. Enter each character of the option registration number.

Carefully examine the number entered. It must be an exact duplicate of the option resistration number provided. The instrument can perform this procedure only once. After step 6 is performed successfully, mistakes can not be corrected.

Press **[BACKSPACE]** or **[ERASE TITLE]** to correct errors. When the title is complete and correct, press **[DONE]**.

5. Press **[SYSTEM] [SERVICE MENU] [TESTS] [5] [6] [x1]** to access the option number save routine. When the display shows "Option Cor", press **[EXECUTE TEST]** to run the routine.

6. Press **[YES]** at the prompt to alter the correction constants.

7. The test status indicator "DONE" signals the successful conclusion of this correction constant procedure.

8. If this procedure did not end with "DONE", either the option registration number entered did not conform to the required format, or a valid option number was stored already, or the option registration number was not valid. Repeat this entire procedure. If still unsuccessful, contact your local HP Sales and Service office.

ANALOG BUS CORRECTION CONSTANTS

DESCRIPTION

Four correction constants allow the analog bus to measure both small and large voltage signal levels. The analog bus circuitry is different for small and large signals. For small signals (high resolution) an amplifier is used while for large signals (low resolution) an attenuator is switched into the circuit. By using three reference voltages (ground, +0.37 and +2.5V), slope and offset values can be derived to linearly characterize the response of both circuits. The four derived correction constants are then stored in EEPROM.

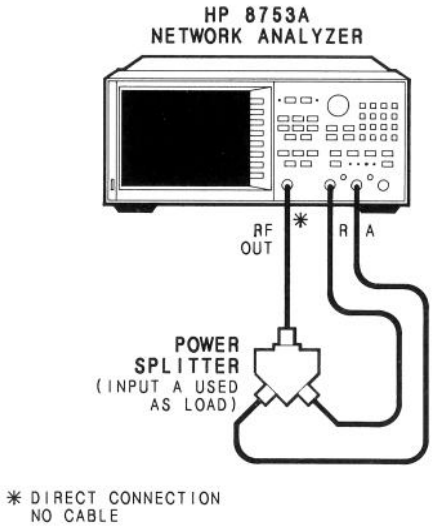


Figure 3. Analog Bus Correction Constant Setup.

EQUIPMENT

Power splitter	HP 11667A option 001
RF cable set	HP 11851B

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper position as explained in "Correction Constant Jumper Position."

1. Turn on the instrument press **[PRESET]** and allow 30 minutes warm-up time.
2. Connect the instrument as shown in Figure 3.
3. Press **[SYSTEM] [SERVICE MENU] [TESTS] [4] [6] [x1]** to access the analog bus resolution correction constants menu. When the display shows "ABUS Cor", press **[EXECUTE TEST]** to enter the routine.
4. Press **[YES]** at the prompt to alter the correction constants.
5. The test status indicator "DONE" signals the successful conclusion of this correction constant procedure.
6. If this procedure did not end with "DONE", refer to the Service section.

ADC LINEARITY CORRECTION CONSTANTS

DESCRIPTION

The ADC Linearity Correction Constants shift small signals to the most linear part of the ADC quantizing curve. This reduces noise and quantizing errors at low power levels and thereby improves dynamic accuracy at low levels.

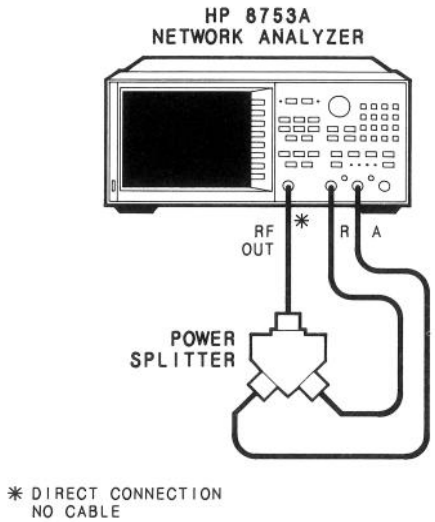


Figure 4. ADC Linearity Correction Constants Setup.

EQUIPMENT

Power splitter	HP 11667A option 001
RF cable set	HP11851B

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper position as explained in "Correction Constant Jumper Position."

1. Turn on the analyzer and allow 30 minutes warm-up.
2. Connect the power splitter to the HP 8753A RF output and inputs R and A as shown in Figure 4.
3. Press **[PRESET] [SYSTEM] [SERVICE MENU] [TESTS] [5] [2] [x1]** to access the ADC linearity correction constants menu.
4. Press **[EXECUTE TEST]** at the "ADC Ofs Cor" title to enter the routine.
5. Press **[YES]** at the prompt to alter the correction constants. The HP 8753A will generate and load the correction constants, in a few minutes.
6. When the test status indicator "DONE" appears, the procedure is finished.
7. In case of difficulty, refer to the Service section.

FRACTIONAL-N FREQUENCY RANGE ADJUSTMENT

DESCRIPTION

The purpose of this adjustment is to center the fractional-N voltage-controlled oscillator (VCO) in its tuning range. This is accomplished by setting the HP 8753A to generate a particular CW frequency. That frequency sets the fractional-N VCO to its maximum frequency. Adjusting the tuning voltage within the limits specified, ensures that two varactor diodes will have sufficient range for reliable operation of the instrument.

Note that this adjustment may be performed either with the analog bus feature or with a digital voltmeter.

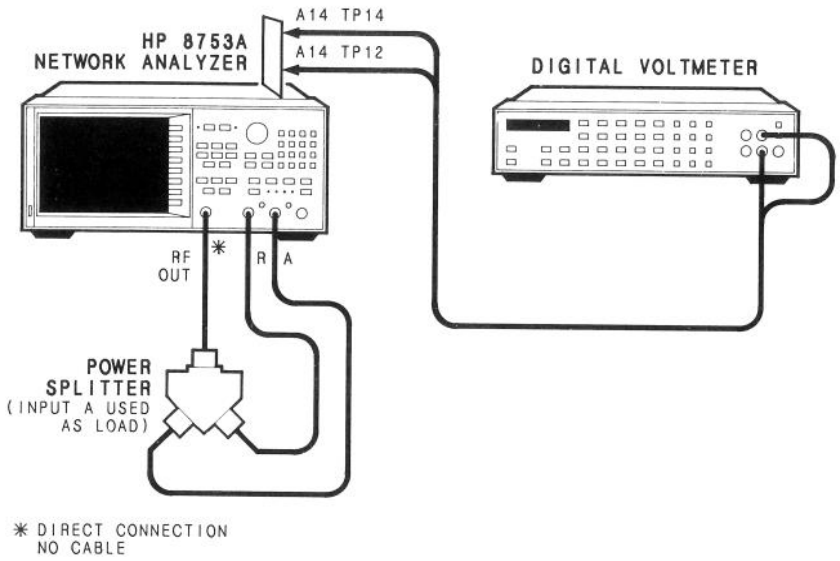


Figure 5. A14 Fractional-N Digital VCO Board Adjustment Setup.

EQUIPMENT

Digital voltmeter	HP 3456A
Power splitter	HP 11667A option 001
Extender board	HP part number 08753-60018
RF cable set	HP 11851B
BNC/alligator clip adapter	HP part number 8120-1292
BNC cable	HP 11086A

ANALOG BUS PROCEDURE

1. Remove the top cover and circuit board stabilizer of the HP 8753A. Install the A14 board (see the Location Diagram) on the extender as shown in Figure 5.

2. Connect the power splitter as shown in Figure 5 and turn on the network analyzer. Allow 30 minutes for warm-up.

3. Press **[PRESET] [SYSTEM] [SERVICE MENU] [ANALOG BUS ON]** to turn on the analog bus feature. Then press **[MEAS] [S PARAMETERS] [ANALOG IN] [2] [9] [x1] [FORMAT] [REAL]** to display the fractional-N tune voltage.

4. Press **[MENU] [CW FREQ] [6] [0] [.] [9] [9] [9] [9] [9] [9] [M/u]** to output a CW frequency of 60 MHz.

5. Press **[SCALE REF] [REFERENCE VALUE] [-] [3] [.] [3] [1] [x1]** to set the reference value to −3.31 Vdc. Then press **[SCALE/DIV] [.] [0] [1] [4] [x1]** to set the scale.

6. If necessary, use a nonmetallic tool to adjust A14L1 (see Figure 6) for a reading of −3.31 ± 0.07 Vdc. The correct adjustment positions the trace on the screen.

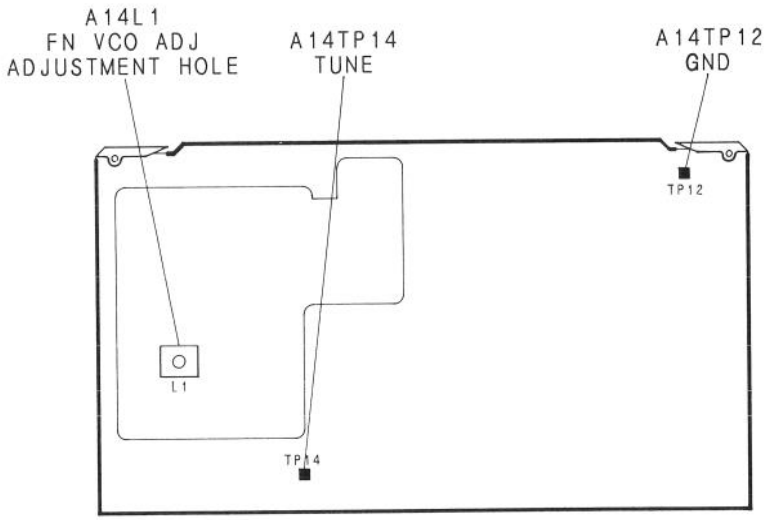


Figure 6. A14 Adjustment Location Diagram.

7. If you were unable to adjust A14L1 as specified, refer to the Service section.

8. Turn off the HP 8753A, remove the extender board and reinstall the A14 board, stabilizer bar and top cover.

DIGITAL VOLTMETER PROCEDURE

9. Remove the top cover and circuit board stabilizer of the HP 8753A. Install the A14 board (see the Location Diagram) on the extender as shown in Figure 5. Use SMB extender cables as required.

10. Connect the equipment as shown in Figure 10 and turn on the network analyzer. Allow 30 minutes for warm-up.

11. Press **[PRESET] [MENU] [CW FREQ] [6] [0] [.] [9] [9] [9] [9] [9] [9] [M/u]** to generate a CW frequency of 60.999999 MHz.

12. Connect DVM HI (center conductor) to A14TP14 (TUNE). Connect DVM LO (shield) to A14TP12 (GND). Refer to Figure 6 as required. The casting need not be removed for measurement or adjustment.

13. If necessary, adjust variable inductor L1 with a non-metallic tool for a DVM reading of -5.00 ± 0.1 Vdc. L1 is adjustable through the hole of the casting.

14. If you were unable to adjust A14L1 as specified, refer to the Service section.

15. Turn off the HP 8753A, remove the extender board and reinstall the A14 board, stabilizer bar and top cover.

SOURCE PRETUNE CORRECTION CONSTANTS

DESCRIPTION

The Source Pretune adjustment consists of generating and loading a number of pretune voltages as correction constants. Each pretune voltage presets the economy YIG oscillator close to and above the corresponding desired frequency. Pretuning insures that the correct harmonic will be locked onto and harmonic skip prevented. Not every frequency has (or needs) a pretune voltage correction constant, since frequency-specific pretune voltages can be derived by interpolation as required.

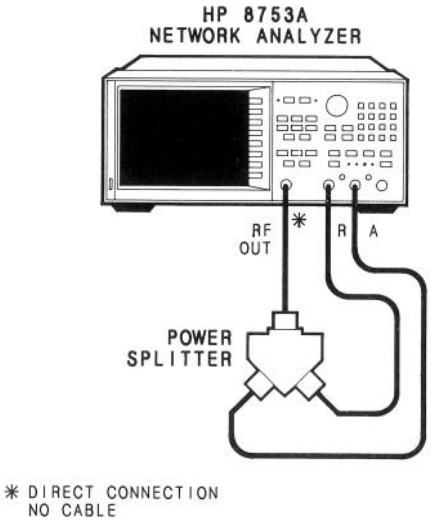


Figure 7. Source Pretune Correction Constants Setup.

EQUIPMENT

Power splitter	HP 11667A option 001
RF cable set	HP 11851B

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper position as explained in "Correction Constant Jumper Position."

1. Connect the equipment as shown in Figure 7, turn on the HP 8753A and allow 30 minutes warm-up time.
2. Press **[PRESET] [SYSTEM] [SERVICE MENU] [TESTS] [4] [8] [x1]** to access the "Pretune Cor" menu. Then press **[EXECUTE TEST]** to begin the Source Pretune Correction Constants routine.
3. Press **[YES]** when the query "CAUTION: OK TO ALTER CORRECTION CONSTANTS?" appears. The instrument will attempt to generate and store the correction constants.
4. When the message "DONE" appears, the correction constants have been generated and stored **unless** accompanied by the "CORRECTION CONSTANTS NOT STORED" warning. This concludes the Source Pretune procedure.
5. If "CORRECTION CONSTANTS NOT STORED" appears, refer to "Correction Constant Jumper Position" at the beginning of this section.
6. If the routine does not end with the "DONE" message, refer to "Source Functional Group Troubleshooting" in the Service section of this manual.

FREQUENCY ACCURACY ADJUSTMENT

DESCRIPTION

The Frequency Accuracy adjustment sets the voltage-controlled crystal oscillator (VCXO) frequency. Since the VCXO serves as the fundamental frequency reference for the HP 8753A, this adjustment determines the basic frequency accuracy of the instrument.

Note that this adjustment can be performed with either a frequency counter or a frequency source standard (1, 2, 5 or 10 MHz) and the HP 8753's analog bus feature. The source/analog bus procedure begins at step 7. Perform the procedure which uses the equipment most easily available to you.

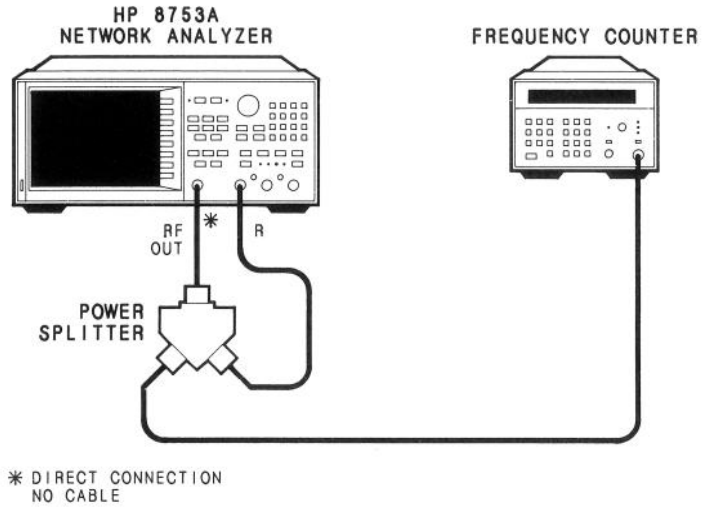


Figure 8. Frequency Accuracy Adjustment Setup.

EQUIPMENT

Frequency Counter Procedure

Power splitter	HP 11667A option 001
Frequency counter	HP 5343A

Source/Analog Bus Procedure

Power splitter	HP 11667A option 001
Synthesizer or signal generator	any source capable of: frequency: 1, 2, 5 or 10 MHz accuracy: 2 ppm power: 0 ± 10 dBm

PROCEDURE

Frequency Counter Procedure

1. Connect the equipment as shown in Figure 8.
2. Turn on the instruments and allow 30 minutes warm-up time.
3. Press **[PRESET] [MENU] [CW FREQ] [5] [0] [M/u]** to set the HP 8753A to a CW frequency of 50 MHz.
4. If the frequency counter indicates a reading of 50 MHz ±500 Hz, the frequency accuracy is within specifications and adjustment is unnecessary. Note that the instrument can easily be adjusted to within 10 Hz.
5. To adjust the frequency accuracy of the HP 8753A, first remove the top cover.
6. Adjust A12R10, VCXO ADJ, (see Figure 9) for a frequency counter reading of 50 MHz ±10 Hz. Successfully performing this adjustment concludes this procedure. If you are not able to adjust the frequency as specified, refer to "Source Troubleshooting" in the Service section of this manual.

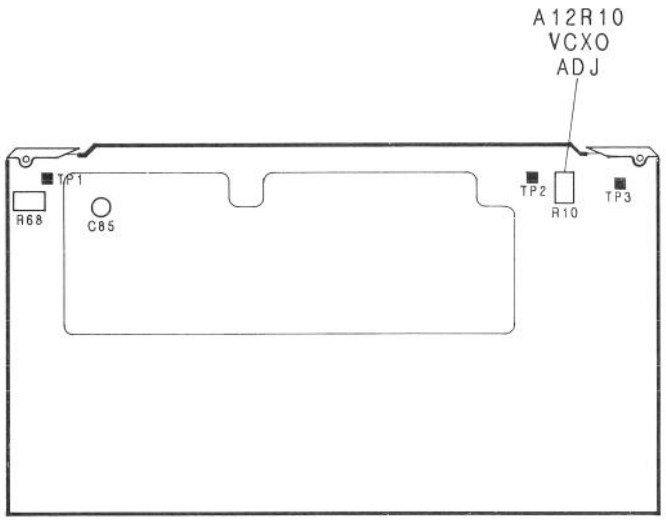


Figure 9. A12 Reference Assembly Adjustment Locations.

Source/Analog Bus Procedure

7. Connect the source to the EXT REF IN connector on the rear panel of the HP 8753A, turn on the HP 8753A and allow 30 minutes warm-up time.
8. Set the source to generate 1 MHz, 2 MHz, 5 MHz or 10 MHz at a power level of 0±10 dBm.
9. On the HP 8753A press **[PRESET] [SYSTEM] [SERVICE MENU] [ANALOG BUS ON]** to turn on the analog bus mode.

10. Press **[MEAS] [S PARAMETERS] [ANALOG IN Aux Input] [2] [7] [x1] [FORMAT] [REAL] [AVG] [AVERAGING ON]** to measure the VCXO Tune voltage.

11. Adjust the scale and reference value to observe the trace. Use a marker if desired. Note the tuning voltage produced by the source frequency and then disconnect the source from the EXT REF IN connector.

12. Set the HP 8753A to generate the same CW frequency as the source. If necessary, adjust A12R10 (see Figure 9) for the same reading as noted in step 10 $\pm$10 mV. Although component variations preclude establishing a strict Hz/mV relationship, a 10 mV variation corresponds to less than 10 Hz. This completes the Frequency Accuracy adjustment.

13. If you are not able to adjust the frequency as specified, refer to "Source Troubleshooting" in the Service section of this manual.

HIGH/LOW BAND TRANSITION ADJUSTMENT

DESCRIPTION

The High/Low Band Transition Adjustment centers the voltage-controlled oscillator (VCO) for both high band and low band operation. Centering the VCO ensures that it can slew to the proper frequency during the RF blanking period of the high/low band switch. Note that this adjustment may be performed using an oscilloscope or using the analog bus of the HP 8753A. The analog bus procedure begins at step 10.

EQUIPMENT

Oscilloscope Procedure

Oscilloscope	HP 1740A
Power splitter	HP 11667A option 001
Extender board, large	part of tool kit HP part number 08753-60023
BNC cable	HP 11086A
RF cable set	HP 11851B
BNC/alligator clip adapter	HP part number 8120-1292

Analog Bus Procedure

Power splitter	HP 11667A option 001
Extender board, large	part of tool kit HP part number 08753-60023
RF cable set	HP 11851B

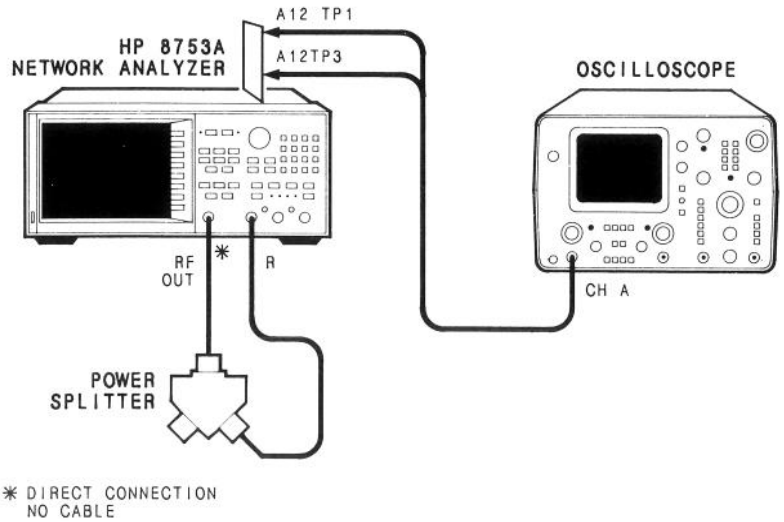


Figure 10. High/Low Band Transition Adjustment Setup.

PROCEDURE

Oscilloscope Procedure

1. Remove the top cover of the HP 8753A, connect the equipment as shown in Figure 10, turn on the HP 8753A and allow 30 minutes warm-up. Note that you need not install the A12 board on the extender board now. Then press **[PRESET] [MENU] [CW FREQ] [1] [0] [M/u]** to set the HP 8753A to a CW frequency of 10 MHz (low band).

2. Connect the oscilloscope to A12TP1 (VCO TUNE) and ground the probe on A12TP3 (GND) (see Figure 11). Set the oscilloscope to 0.1V/division and about 0.05 usec/division. The time setting is not crucial; you need not trigger on the actual waveform but merely center the trace. The oscilloscope should display the trace at 0.0 ± 2.0 Vdc.

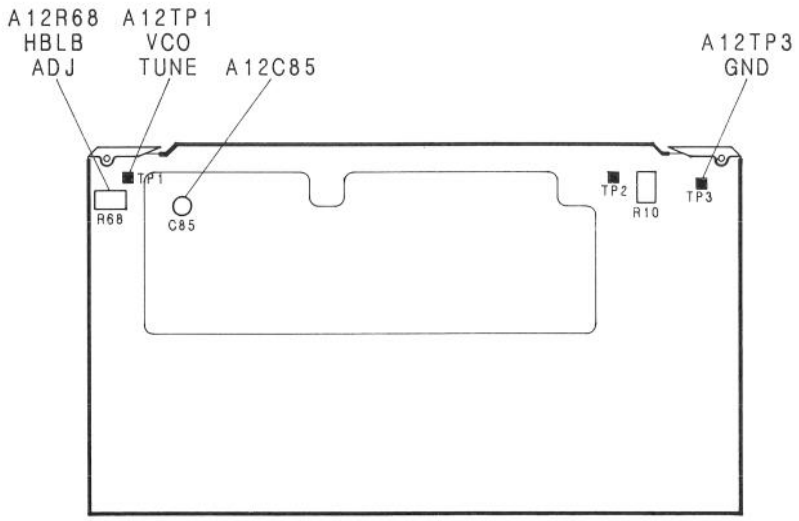


Figure 11. A12 Reference Assembly Adjustment Locations.

3. On the HP 8753A, press **[2] [0] [M/u]** to generate a CW frequency of 20 MHz (high band).

4. The trace should now be 200 to 400 mVdc **higher** than the previous reading.

5. If the oscilloscope displays the proper traces in both low band and high band, the VCO is centered and the High/Low Band Transition Adjustment is finished.

6. If the readings were not as specified, turn off the HP 8753A. Install the A12 reference board on the extender board to gain access to A12C85. Use SMB cables as required. Turn on the HP 8753A again.

7. Set the HP 8753A to generate 10 MHz CW and adjust A12C85 for an oscilloscope reading of 0.0 ± 0.25 Vdc. Set the HP 8753A to generate 20 MHz CW and adjust A12R68, HBLB ADJ, for an oscilloscope reading of 0.30 ± 0.05 Vdc **higher** than the previous reading. Refer to Figure 11 as required.

8. Turn off the HP 8753A and reinstall the A12 board in the instrument. Refer to the Location Diagram on the underside of the top cover to properly reconnect the cables. Replace the top cover and tighten the captive screw.

9. This completes the High/Low Band Transition Adjustment procedure. If you are unable to adjust this board as specified, refer to "Source Troubleshooting" in the Service section of the manual.

Analog Bus Procedure

10. Turn on the HP 8753A and allow 30 minutes for warm-up. Press **[PRESET] [SYSTEM] [SERVICE MENU] [ANALOG BUS ON]** to use the analog bus feature. Then press **[START] [1] [1] [M/u] [STOP] [2] [1] [M/u]** to observe part of both the low and high bands.

11. Press **[MEAS] [S PARAMETERS] [ANALOG IN Aux Input] [2] [2] [x1] [FORMAT] [REAL]** to measure the "A12 GND 1" on the analog bus. Then press **[DISPLAY] [DATA→MEM] [DATA-MEM]**to subtract the ground voltage from the next measurement.

12. Press **[MEAS] [S PARAMETERS] [ANALOG IN] [2] [3] [x1]** to select the VCO Tune voltage. Then press **[SCALE REF] [AUTO SCALE]** to observe the trace.

13. The trace on the left half of the CRT should indicate 0 ± 1000 mVdc. The right half of the trace should be 100 to 200 mVdc **higher** than the left half. If the two values are as specified, this adjustment procedure is finished. Otherwise continue with the following steps.

14. Turn off the HP 8753A, remove the top cover of the instrument, place the A12 board on an extender board (using SMB extension cables as required), and turn on the analyzer again.

15. Repeat steps 10 through 12. Adjust A12C85 (see Figure 11) to position the left side of the trace to 0 ± 125 mV. Then adjust A12R68 to position the right side of the trace 125 to 175 mV **higher** than the left side. Turn off the instrument, remove the extender board and reinstall the A12 reference board. Replace the top cover.

16. If you are unable to position the trace as specified, refer to "Source Troubleshooting" in the Service section of this manual.

FRACTIONAL-N SPUR AND FM SIDEBAND ADJUSTMENT

INTRODUCTION

The fractional-N spur and FM sideband adjustment consists of an automated routine that requires an HP 9000 series 200/300 desktop computer, associated peripherals and the software provided on disc in this manual. This adjustment does require operator interaction and is best described as semiautomated.

NOTE: Read the next few pages before attempting to run the adjustment software. This will avert most problems before they arise.

This adjustment procedure is organized as follows:

SETTING UP THE SYSTEM: This provides hardware and software model numbers for proper system configuration. It also provides instructions for loading the operating system.

SOFTWARE BACK-UP: This defines the files provided with the adjustment software, and also provides instructions for disc copying.

INSTRUMENT ADDRESSES: This provides information on setting the HP-IB addresses of the instruments used in this adjustment to conform to the addresses assigned in the adjustment software.

ADJUSTMENT PROCEDURE: This includes a description and a step-by-step procedure for running the adjustment software. An adjustment setup diagram and location diagram are provided.

SETTING UP THE SYSTEM

System Hardware Configuration

Refer to Figure 12, which shows the fractional-N spurs and FM sideband adjustment setup.

Controllers. The HP 9000 series 200/300 controllers listed below can be used to run the adjustment. Other controllers not listed here may work.

Table 1. HP 9000 Controller Models

Series 200:	216, 226, 236, 220
Series 300:	310

Peripherals

The automated adjustment requires mass storage and a printer. The required measurement instrumentation is listed in the adjustment procedure.

There are many compatible disc drives. The following drives are recommended as a convenience only. Most HP drives will work.

Table 2. Compatible Disc Drives

Model Number	Command Set
HP 9121D	AMIGA
HP 9133A	AMIGA
HP 9133B	AMIGA
HP 9133V/XV	AMIGA
HP 9122D	CS80
HP 9133D/H	CS80
HP 9153A	CS80

A printer is not required but can be used to record adjustment results, output in graph format. This requires a printer capable of accepting raster data (dump graphics) from the controller. Printers that are known to have this capability are listed below.

Table 3. Compatible Printers

HP 2225A ThinkJet
HP 2671G/2673A Thermal Printer
HP 9876A Thermal Line Printer

Adjustment Program Software

Software is provided on a 3.5 inch floppy disc, formatted single sided so it will be usable in either single or double sided disc drives. This adjustment software is on DISC 1 of the HP 8753A Performance Test and Adjustment Programs disc (HP part number 08753-10010) supplied in this manual.

System Software Requirements

The HP 8753A adjustment software requires BASIC version 3.0 or 4.0.

To load the BASIC system, locate the BASIC System Disc (not included in this manual). Insert the disc into the disc drive and power on the computer. The computer will locate the BASIC operating system and load it into memory.

BASIC versions 3.0 and 4.0 provide a modular operating system architecture. The core of the system is provided on the operating system disc. Additional computation and IO capability is available through the use of code modules called binaries. Binaries are separated into two groups: Language Extensions and Drivers. The HP 8753A Performance Test and Adjustment Program software requires the following binaries.

Table 4. Required Binaries

Language Extensions	ERR GRAPH IO KBD MAT MS
Drivers	CS80 or DISC (depends on disc) HPIB CRTA or CRTB (depends on CRT)

If you already have a pre-configured BASIC system, you can verify whether or not it contains all of the above binaries. Type:

`LIST BIN` and press **[ENTER]** or **[RETURN]** to execute the command.

All binaries currently contained in memory will be listed to the screen. If any of the required binaries are missing, insert the Drivers disc provided with the system and load the Configure program. Type:

```
LOAD ''CONFIGURE''
```

Press **[RUN]** to start the configure program.

This program lets you select the necessary binary modules and loads them for you. Simply follow the prompts. The program tells you to load the appropriate disc, lists the binaries available on that disc and links that binary into the system upon your command.

You must know what type of disc drive you are using and the command set it uses to select the correct mass storage driver. Drives using CS80 or SS/80 command set require the CS80 binary; most drives which read double-sided media use CS80 command set. Other discs use the AMIGA protocol and require the DISC binary. Table 2 lists the command set used by several HP disc drives. If you are unsure, load both binaries.

Refer to the BASIC user's documentation for more comprehensive instructions on loading the operating system and binaries.

SOFTWARE BACKUP

Disc Files

The files contained on the software discs provided are as follows:

DISC 1

PERFTEST	:	main performance test program
MS_CONFG	:	mass storage configuration file
DEV_CONFG	:	device configuration file
API_ADJ	:	fractional-N spur and FM sideband adjustment program

DISC 2

power_test	:	output power performance test subprograms
spur_test	:	spectral purity performance test subprograms
dyaccytest	:	dynamic accuracy performance test subprograms
HP436A	:	HP 436A subprograms (performance tests)
HP438A	:	HP 438A subprograms (performance tests)

Making Working Copies

NOTE: Before doing anything else, make working copies of these discs!

The master discs are shipped from the factory write-protected and cannot be written to or initialized in this mode. We recommend you maintain these discs in write-protect mode. During execution, the performance test program must read from and write to one of these discs, therefore it must not be write protected in normal use. You must copy the master discs to working copies using the instructions below. If the working copy is damaged or lost, the master is always available.

NOTE: The files contained on Disc 1 must reside on the same mass storage medium. Likewise, the files on Disc 2 must reside on the same mass storage medium.

To copy the master disc, you must initialize a blank disc. Insert a blank disc into the disc drive and type:

```
INITIALIZE ":msus"
```

where *msus* is the address of the drive containing the disc to be initialized. The initialization process takes approximately 60 seconds.

To copy the contents of the master disc to the working disc, follow the instructions below:

Copying to a Hard Disc or Double-Sided Flexible Disc

If you copy both master discs to a storage medium of a larger size, you will have to perform a file-by-file copy instead of copying the entire volume at once. To perform a file copy, follow the instructions below. After typing a command from the keyboard, press **[ENTER]** or **[RETURN]** to execute the command.

1. Insert the master disc into the drive and obtain a directory listing. Type:

   ```
   CAT ":msus"
   ```

   where *msus* is the mass storage unit specifier of the drive containing the master disc.

2. If you are copying to a flexible disc, insert the initialized working disc into the second drive. Type:

   ```
   COPY "^lename:master msus"   TO   "^lename:destination msus"
   ```

   where *master msus* is the mass storage unit specifier of the disc drive containing the master disc and *destination msus* is the mass storage unit specifier of the flexible or hard disc drive containing the working storage media.

   Perform step 2 for each file in the master disc directory listing, for each master disc.

An example: Your system includes an HP 9133H disc drive at HP-IB address 700. The hard disc is unit 0 and the floppy drive is unit 1 (the hard disc can be configured as one large volume or several). To file copy from the master disc in the floppy drive to volume 3 of the hard disc, the copy command syntax is:

```
COPY "PERFTEST:,700,1"   TO   "PERFTEST:,700,0,3"
```

Copying Flexible Discs with Two Drives

1. Insert the master disc into one drive and the initialized working disc into the other drive.

2. Type:

   ```
   COPY ":source msus"   TO   ":destination msus"
   ```

   where *source msus* is the mass storage unit specifier of the drive containing the disc you want to copy, and *destination msus* is the mass storage unit specifier of the drive containing the initialized working disc.

   An example: With an HP 9122D dual disc drive at address 700, the master disc in the left drive, and the working disc in the right drive, the copy command syntax is:

   ```
   COPY ":,700,0"   TO   ":,700,1"
   ```

Copying Flexible Discs with One Drive

When only one drive is available, disc contents must first be copied into memory, then from memory to the destination disc.

1. Type:

   ```
   INITIALIZE ":MEMORY,0"
   ```

2. Insert the master disc into the disc drive.

3. Type:

   ```
   COPY ":msus"    TO    ":MEMORY,0"
   ```

   where *msus* is the mass storage unit specifier of the disc drive.

4. When the copying is done, remove the master disc from the disc drive and insert an initialized disc into the drive.

5. Type:

   ```
   COPY ":MEMORY,0"    TO    ":msus"
   ```

   where *msus* is the mass storage unit specifier of the disc drive.

INSTRUMENT ADDRESSES

Use the following text as an aid in making sure the HP-IB addresses of the various instruments used in this adjustment match the addresses set for them in the adjustment software program.

The adjustment software assumes that each instrument is set to the recommended default address assigned at the factory. Instruments used in this adjustment and their factory-set HP-IB addresses with a select code of 7 are listed below.

HP 8753A	716
SPECTRUM ANALYZER	718
PRINTER	701

Check the addresses on all instruments to make sure they conform to the addresses above. We recommend that you change the address on each instrument itself, if necessary, to comply with these factory recommended defaults. Refer to the individual instrument manuals for instructions on checking and changing these HP-IB addresses.

If an instrument address other than those shown above must be used, the address in the adjustment software program must be modified. In this case, perform the following procedure:

Type:

```
EDIT HPIB_ADDRESSES
```

Press **[RETURN]** or **[ENTER]** to execute the command.

This command displays the lines of code containing addresses of the spectrum analyzer, network analyzer, and printer, respectively. They look like this:

```
ASSIGN @sa_66 TO 718
ASSIGN @Vna TO 716
DUMP DEVICE IS 701                    ! printer address
```

Using the cursor control keys, position the cursor under the address numbers to be changed (718, 716, or 701). Type the new address and press **[RETURN]** or **[ENTER]**. Be sure that the address set at the instrument matches the address just assigned in program code.

Adjustment Procedure

DESCRIPTION

The A13 fractional-N board assembly has four analog phase interpolator (API) adjustments, and one 100 kHz adjustment. The API adjustments optimize spurious responses on the fractional-N signal, which are generated by API currents turning on and off. The 100 kHz adjustment reduces the FM sideband on the fractional-N signal, caused by the 100 kHz reference slightly modulating the fractional-N signal at the phase detector on A13.

First, this routine optimizes these five adjustments for the lowest spurious signal content at a single frequency.

Second, the spurious content is measured over the fractional-N frequency range (30 to 60 MHz), and a composite plot is generated. Any "fine" adjustments to API1 or 100 kHz can be made to optimize the spurious response over this frequency range. Of the four API potentiometers, API1 has the most effect.

Spectral purity is improved by making these adjustments.

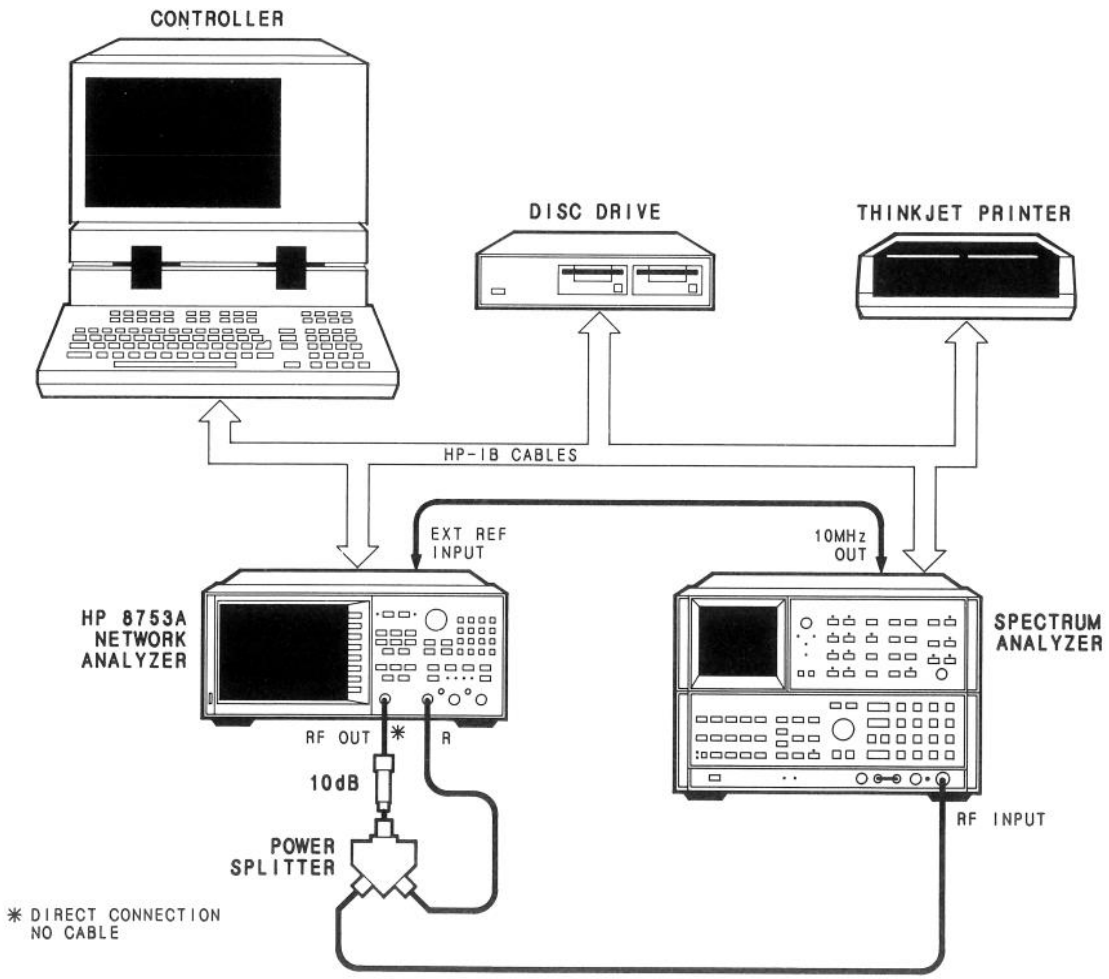


Figure 12. Fractional-N Spur and FM Sideband Adjustment Setup.

EQUIPMENT

Spectrum analyzer	HP 8566A/B
Power splitter	HP 11667A option 001
10 dB attenuator	HP 8491A option 10
RF cable set	HP 11851B
BNC cable	HP part number 8120-1840

PROCEDURE

1. Connect the equipment as shown in Figure 12.
2. Turn on the equipment and allow 30 minutes warm-up time.
3. Load the BASIC operating system. Refer to the preceding pages for detailed instructions of this procedure, if necessary.
4. Insert DISC 1 into the disc drive. Set the MSI to the mass storage unit specifier of the disc drive containing DISC 1. Type:

   MSI ":*msus*"

   where *msus* is the mass storage unit specifier of the drive containing DISC 1.
5. Type:

   `LOAD "API_ADJ"` to load the adjustment software. Press **[ENTER]** or **[RETURN]** to execute the command.
6. Press **[RUN]** to execute the program. A menu showing the software revision will appear on the computer display.
7. Continue the program by pressing any key on the computer. The program will perform a calibration.

   NOTE: When making adjustments in the following steps, the spurious signal to be nulled will always be in the center of the spectrum analyzer display. Disregard any other signals not appearing in the center of the display.
8. Refer to Figure 13 for adjustment locations. When prompted, adjust API1 on the A13 fractional-N analog board assembly for minimum signal amplitude while viewing the center of the spectrum analyzer display. Press any key on the computer to continue the program.

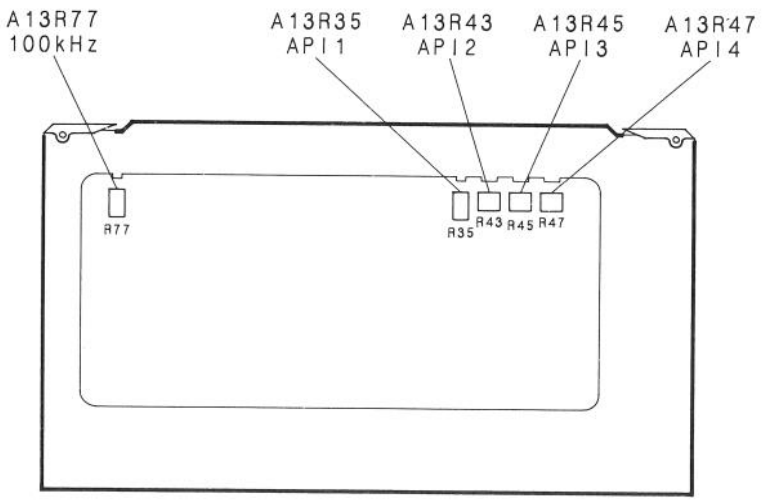


Figure 13. Fractional-N Spur and FM Sideband Adjustment Locations

9. Repeat step 7 to adjust API2, API3, API4, and 100 kHz.

10. A composite plot of API spurs (amplitude versus frequency) will appear on the computer display approximately one minute after the 100 kHz adjustment is completed. This data trace must be below the specification trace, which is also plotted on the display.

11. The plot allows three choices of softkeys:

    [RE-PLOT] A new plot is initiated.

    [NEXT] The program is continued.

    [HRDCOPY] A hardcopy of the plot is printed.

    NOTE: Whenever **[RE-PLOT]** is pressed, the newest data will be plotted. The specification trace and the data trace plotted last will remain, but the oldest of any two data traces will be deleted from the display.

    If the data trace is out of specification, or it is desired to optimize the spurs across the band even though specification has been met, continue with this step.

    Adjust API1 one-half turn counter-clockwise, and press **[RE-PLOT]**.

    NOTE: Do not use the response on the spectrum analyzer display to make this adjustment because you are now adjusting for an overall optimized data trace, and not to optimize the spur on any specific frequency.

    If the data trace is worse than the previous one, adjust API1 one full turn clockwise, and re-plot the result. Iterate the adjustment in this manner by turning the potentiometer in varying amounts until the data trace is optimized.

12. Press **[NEXT]** to continue the program. A plot of calculated 100 kHz spurs (amplitude versus frequency) will appear on the computer display. This response trace must be below the specification trace, which is also plotted on the display.

13. Repeat step 11 for the 100 kHz adjustment, using the 100 kHz adjust in place of API1.

14. Press **[NEXT]** to complete the fractional-N spur and FM sideband adjustment.

SOURCE SPUR AVOIDANCE TRACKING ADJUSTMENT

DESCRIPTION

The cavity oscillator adjustment optimizes tracking between the YIG oscillator (YO) and the cavity oscillator when they are frequency offset to avoid spurs. Spurs are known to be generated in the mixing process at particular frequencies and can be avoided by shifting the frequency of the YO and cavity oscillator by the same amount. This shift effectively removes the spurs from the frequency of interest while maintaining the desired output frequency. Optimizing YO-cavity oscillator tracking reduces the perturbations to the phase-locked loop.

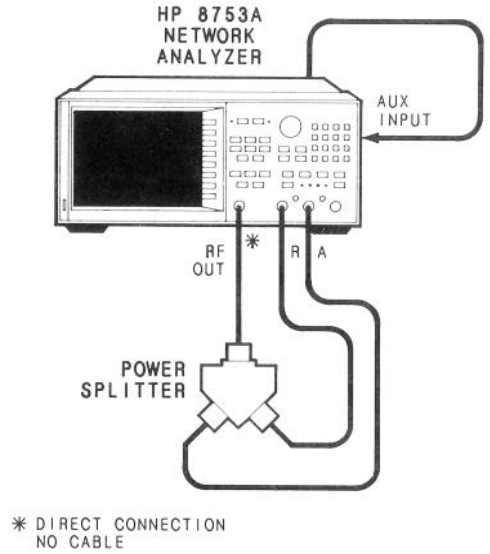


Figure 14. Cavity Oscillator Adjustment Setup.

EQUIPMENT

Power splitter	HP 11667A option 001
RF cable set	HP 11851B
BNC/alligator clip adapter	HP part number 8120-1292
BNC cable	HP 11086A

PROCEDURE

1. Connect the equipment as shown in Figures 14 and 15. The BNC center conductor alligator-clip should be connected to A11TP10 (labeled D ERR); the shield clip to A11TP1 (GND).

2. Set the LINE switch to ON and allow 30 minutes warm-up time.

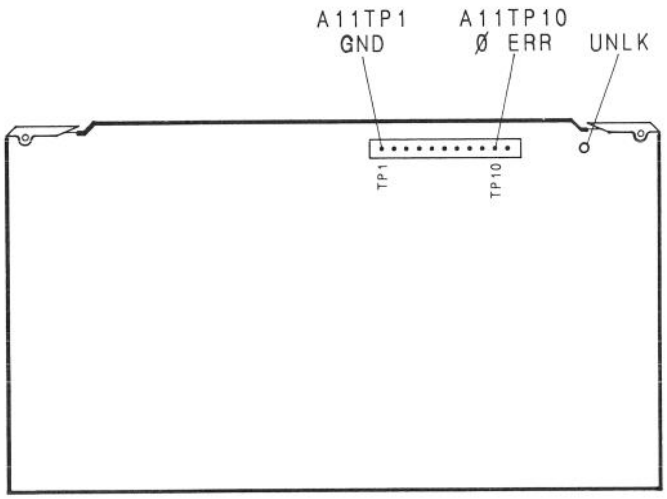


Figure 15. Part of A11 Board.

3. On the HP 8753A press **[PRESET] [CENTER] [4] [0] [0] [M/u] [SPAN] [5] [0] [M/u]** to generate a sweep from 375 MHz to 425 MHz.

4. Press **[SYSTEM] [SERVICE MENU] [ANALOG BUS ON] [MEAS] [S PARAMETERS] [ANALOG IN] [1] [1] [x1]** to turn on the analog bus and measure the phase-locked loop's error voltage at node number 11.

5. Press **[FORMAT] [REAL] [SCALE REF] [1] [0] [k/m] [MARKERREFERENCE]** to format and scale the CRT.

6. Adjust the CAV ADJ potentiometer (see Figure 16) on the A3 source bias to eliminate spikes on the CRT (see Figure 17).

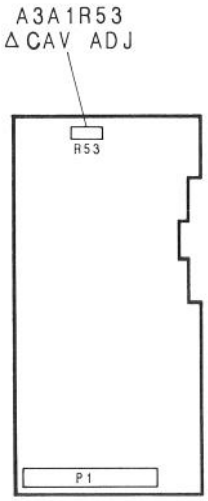


Figure 16. Location of "CAV ADJ" adjustment.

7. Refer to the Service section of this manual if visible spikes persist.

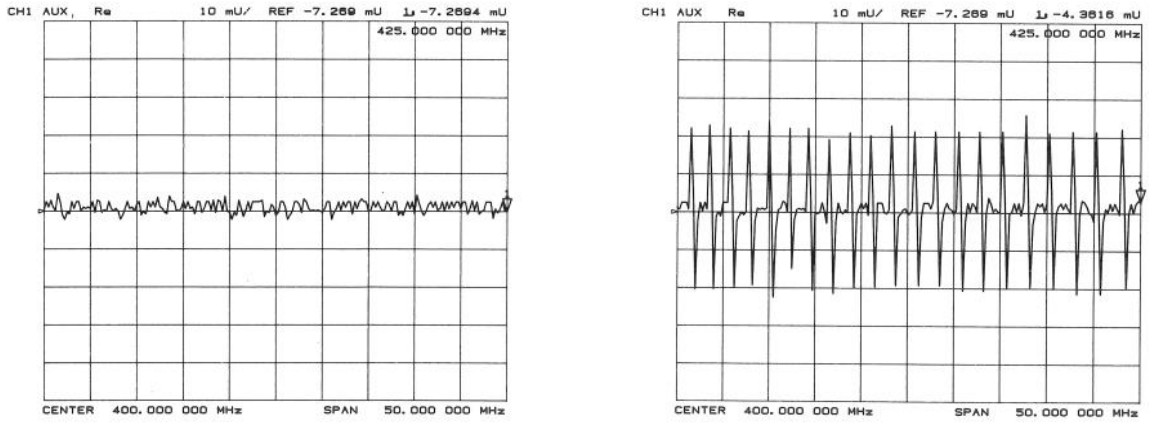


Figure 17. Display of Acceptable versus Excessive Spikes.

8. This concludes the Source Harmonics Adjustment procedure.

SAMPLER DIODE BIAS ADJUSTMENT

DESCRIPTION

The sampler/mixer board potentiometer adjusts the bias of the sampler diodes. This adjustment affects the length of time that the sampler diodes are turned on. Changing the diode conduction interval changes the band step size, the IF level and the high frequency amplitude response (rolloff). The following procedure balances the band step size and the rolloff for optimum performance.

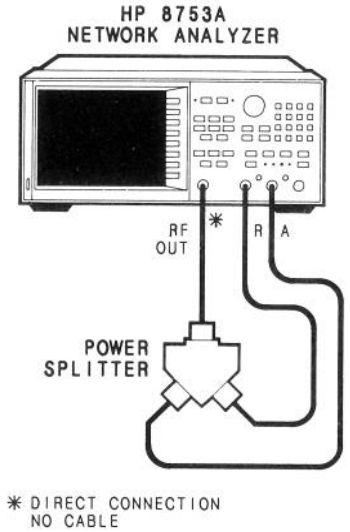


Figure 18. Sampler Diode Bias Measurement Setup.

EQUIPMENT

Power splitter	HP 11667A option 001
RF cable set	HP 11851B
Extender board, small	part of tool kit 08753-60023
Rigid cable SMA (m)	HP part number 08753-20028 (part of tool kit 08753-60023)
Adapter SMA (f)/N (m)	HP part number 1250-1250 (part of tool kit 08753-60023)
Adapter N (f)/N (f)	HP part number 1250-1472

NOTE: In this procedure, input R is used as an example. Substitute A or B as required.

PROCEDURE

1. Set the LINE switch to ON and allow 30 minutes warm-up time.
2. Connect the equipment as shown in Figure 18.
3. On the HP 8753A press **[PRESET] [SYSTEM] [SERVICE MENU] [SERVICE MODES] [MORE] [SAMPLR COR OFF] [CH 2] [SAMPLR COR OFF]** to turn off the sampler correction feature for both channels.
4. Press **[MENU] [COUPLED CH OFF] [CH 1] [MEAS] [R]** to measure the uncoupled response of the sampler.
5. Press **[START] [3] [5] [M/u] [STOP] [9] [5] [M/u]** to observe the sampler band step size. Then press **[SCALE REF] [.] [5] [x1] [MARKER→REFERENCE]** to set up channel 1 to display the sampler band step size. The band step size should be 0.2 to 0.8 dB as shown in Figure 19.

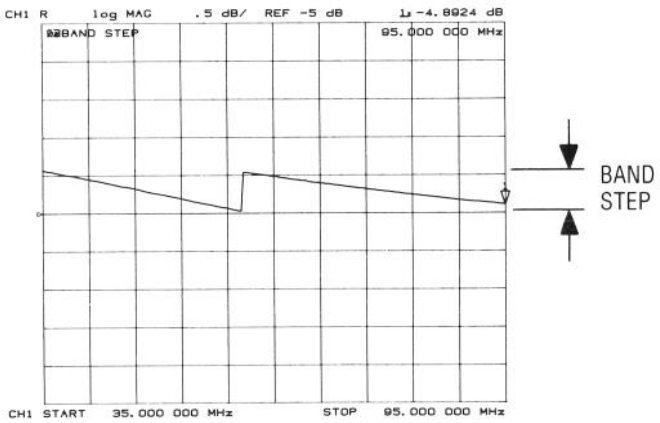


Figure 19. Band Step Size

6. Press **[DISPLAY] [DUAL CHAN ON]** to view both channels simultaneously. Then press **[CH 2] [MEAS] [R] [START] [4] [5] [M/u] [x1]** to set up channel 2 to display the sampler rolloff. Adjust the scale and reference to display the trace on the screen. The sampler rolloff should be 1.5 to 3.5 dB as shown in Figure 20.

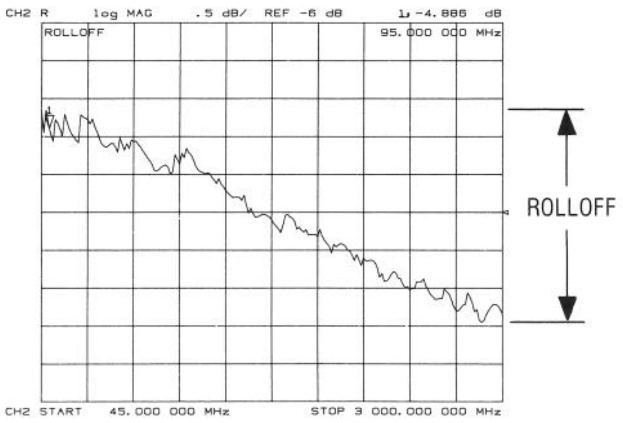


Figure 20. Rolloff.

7. If the band step size and the sampler rolloff are within the limits of steps 5 and 6, no adjustment is required and this procedure is finished.

8. If adjustment is required, turn off the HP 8753A.

9. Remove the top cover of the instrument by loosening the captive screw in the middle of the rear edge and sliding it back and off.

10. Remove the four screws that fasten the cover of the sampler board. Unplug the flexible SMB cable(s) (the R sampler has 2 SMB cables, the A and B samplers, 1). Unscrew and detach the rigid SMA cable. Withdraw the sampler board (A4, A5 or A6).

11. Place the sampler board on the small extender board and reconnect the flexible SMB cable(s). Use extension cable(s) as required. Disconnect the cable on the front panel input R and reconnect it to the SMA connector of the sampler. Use the rigid extender cable, an SMA (f)/type-N (m) adapter and a type-N (f)/type-N (f) adapter as illustrated in Figure 21.

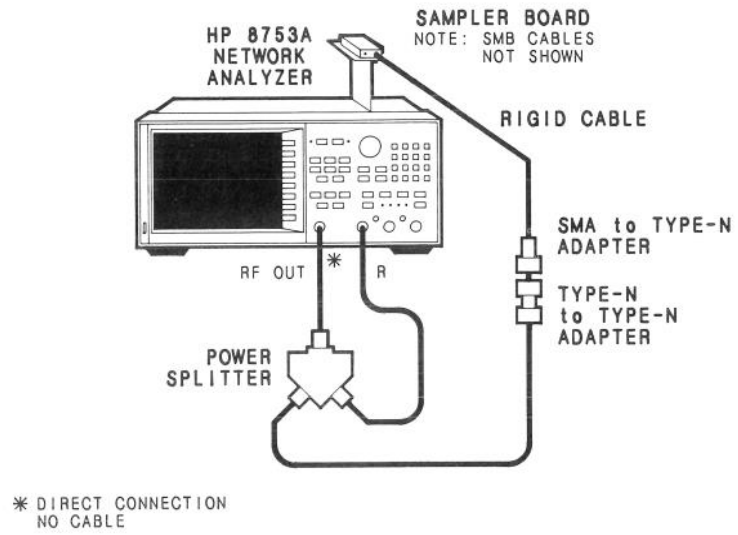


Figure 21. Cable Connections with Sampler on Extender Board.

12. Turn on the HP 8753A and perform steps 3 through 6 to observe the band step and rolloff of the sampler.

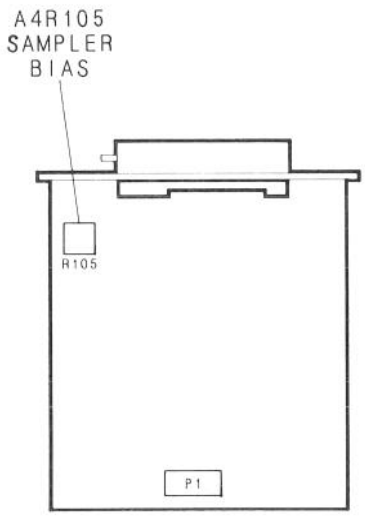


Figure 22. Sampler Diode Bias Adjustment Location.

13. Adjust the sampler bias potentiometer (see Figure 22) so that the band step is between 0.2 and 0.8 dB and the rolloff is between 1.5 and 3.5 dB (similar to Figures 19 and 20).
14. When the adjustment is done, turn off the instrument, remove the extender boards and cables and reassemble the instrument. Make sure the four sampler board cover screws are reinstalled tight enough (very tight) to prevent leakage and cross-talk.
15. Following this procedure you should perform the Sampler Magnitude and Phase Correction adjustment.
16. If you were unable to meet the specifications, refer to the Service section.
17. This completes the Sampler Diode Bias Adjustment.

SAMPLER MAGNITUDE AND PHASE CORRECTION CONSTANTS

DESCRIPTION

After the Sampler Diode Bias Adjustment is performed, the magnitude and phase response of the sampler must be corrected. This is done with a semi-automated HP 8753A routine and a power meter. Due to the scheme of phase locking through input R, the setup for generating the R sampler correction constants differs from the setup for inputs A and B. The power detected by the power meter is compared to the R sampler response. The difference is the correction constant value that is then loaded in the HP 8753A. "Cabling" from the power splitter to the power sensor and to input R must therefore be as direct and as lossless as possible. Points are taken at the edges of each band.

The setup for the A and B samplers requires only a power splitter and assumes that input R has been corrected already. High-quality, identical, short cables from the power splitter to input R and A or B are crucial. The routine compares the magnitude and phase of inputs A and B to input R for the same frequencies checked in the R routine. The differences are then stored in EEPROM as the correction constants. Note that if the R sampler is replaced or assigned new correction constants, both A and B must be re-corrected.

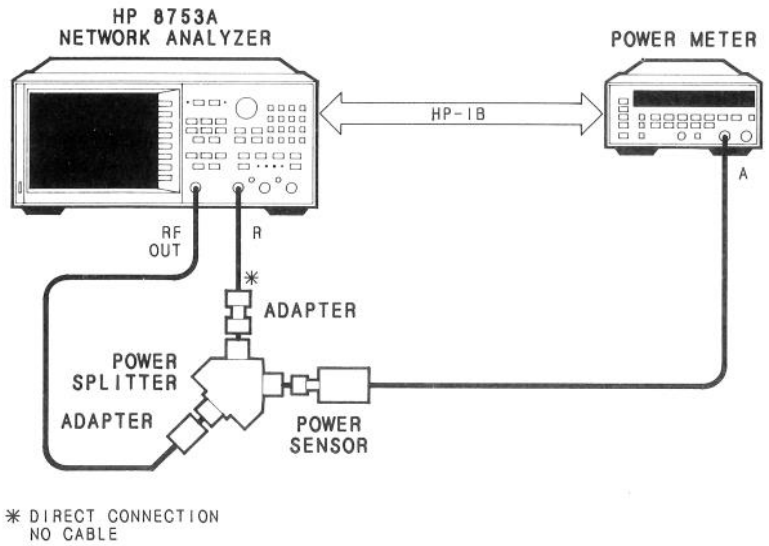


Figure 23. Input R Sampler Correction Setup.

EQUIPMENT

Power meter	HP 436A option 002 or HP 438A
Power sensor	HP 8482A
Power splitter	HP 11667A option 001
Cables (2)	HP 11500B (2 identical, high quality cables)
Adapter N(f)/N(f)	HP part number 1250-1472
Adapter N(m)/N(m)	HP part number 1250-1475

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper position as explained in "Correction Constant Jumper Position."

1. Turn on the HP 8753A and allow 30 minutes for warm-up.
2. Press **[PRESET] [LOCAL] [SYSTEM CONTROLLER]** to give the HP 8753A control of the bus and the power meter.
3. Press **[SET ADDRESSES] [ADDRESS: POWER MTR]** to see the address at which the analyzer expects to find the power meter (the default address is 13). The power meter must be set to the address indicated on the HP 8753A CRT. Refer to the power meter manual as required to observe or change its address. Note that the key labeled **[POWER MTR: 438A]** toggles between 438A and 436A and must match your power meter model number. PRESET returns this selector to 438A. When connecting the power sensor to the HP 438A, use channel A.

Power Sensor Calibration Factor Entry

4. On the HP 8753A press **[SYSTEM] [SERVICE MENU] [TEST OPTIONS] [POWER SENSOR]** to access the calibration factor routine. (To enter accurate correction constants in this procedure, you must take into account the calibration factor for the power sensor of the power meter.)
5. In this menu you can build a table of up to twelve points (twelve frequencies with their cal factors). Frequency can be input as GHz or MHz by pressing the appropriate entry key. Cal factor percentages must be input as whole numbers (for example, enter CAL FACTOR 98% as 98). The cal factor and frequency values are found on the back of the HP 8482A power sensor.
6. If calibration factors have not been entered previously, the CRT displays "EMPTY". To add a point to the table, for example 1 GHz with a cal factor of 99%, press **[ADD] [FREQUENCY] [1] [G/n] [CAL FACTOR] [9] [9] [x1] [DONE]**.
7. When the table has two or more points (lines of data), the cursor indicates the point that you can **[EDIT]** or **[DELETE]**. Use the **[SEGMENT]** softkey and the RPG knob or any key in the ENTRY area to review the table and position the cursor. Press **[DONE]** when you have finished entering the calibration factor data.
8. Zero and calibrate the power meter (refer to its manual as required).

Sampler Correction Constant Routine

9. On the HP 8753A press **[LOCAL] [SET ADDRESSES]** to confirm that the power meter model number displayed is correct. Then press **[SYSTEM] [SERVICE MENU] [TESTS] [5] [3] [x1]** to enter the sampler correction constant routine. When the CRT displays "Sampler Cor", press **[EXECUTE TEST]** to begin the routine.
10. Press **[YES]** at the prompt to alter the correction constants. At the next prompt, connect the RF OUT of the HP 8753A to the input of the power splitter, one splitter output to input R and the other splitter output to the power sensor as shown in Figure 23. Then press **[CONTINUE]** to run the test. It takes a few minutes to run.
11. When prompted, connect the power splitter directly to RF OUT and connect the output ports to inputs R and A as shown in Figure 24. Use two cables of equal electrical length. Press **[CONTINUE]** to proceed with the input A routine.

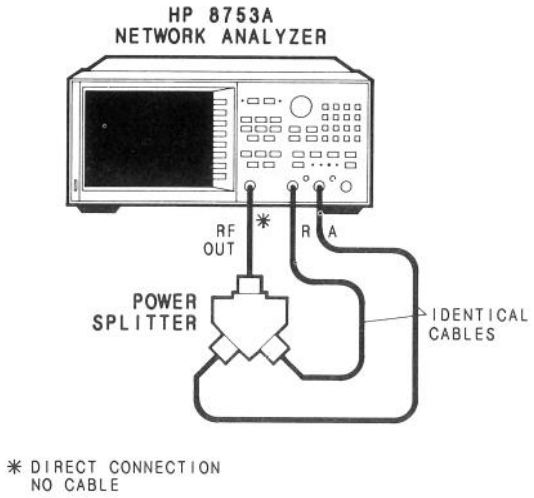


Figure 24. Input A Sampler Correction Constant Setup.

12. Move the cable from input A to B as shown in Figure 25 when prompted. Press **[CONTINUE]** to continue with the input B routine.

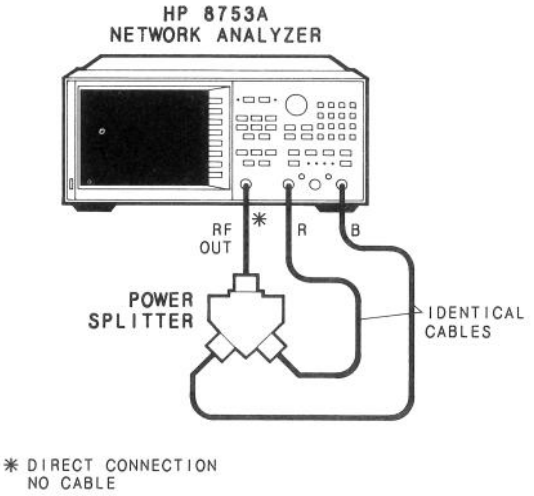


Figure 25. Input B Sampler Correction Constant Setup.

13. When the routine finishes, the display should indicate "DONE". If the display indicates "FAIL", refer to "Receiver Troubleshooting" in the Service section.

14. This concludes the Sampler Magnitude and Phase Correction Constant procedure.

Optional Check Procedure

15. To observe the effect of the sampler correction constant on input R, connect a cable from RF OUT to input R. Then press **[PRESET] [MEAS] [R] [SCALE REF] [AUTO SCALE] [SYSTEM] [SERVICE MENU] [SERVICE MODES] [MORE]**. Toggle **[SAMPLR COR on/off]**. The display should appear similar to Figure 26. Otherwise refer to "Receiver Troubleshooting" in the Service section.

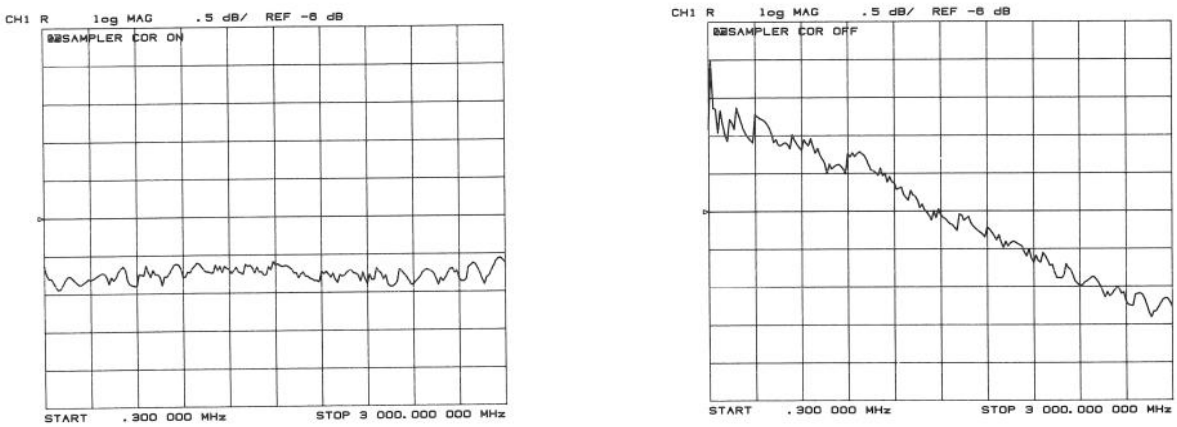


Figure 26. Effect of Sampler Correction Constants.

RF OUTPUT POWER CORRECTION CONSTANTS

DESCRIPTION

Several correction constants improve the output power level accuracy of the source by compensating for hardware variables that would otherwise affect power accuracy. More specifically, the source correction constants relate to power level, power slope, power slope offset, and several breakpoints.

Theoretically, in the HP 8753A, a linear relationship exists between the number input to the power level DAC and the power level output by the source. This linear power level relationship is defined by a 0 dBm offset correction constant and a slope correction constant.

Two other correction constants characterize the power slope function in terms of the number input to the power slope DAC and the power slope out of the source. Other correction constants compensate for low frequency power shift due to slope, ALC rolloff, the breakpoint for the square-law/linear region, and low power detector buffer inaccuracies. The semi-automated procedure for loading these correction constants follows.

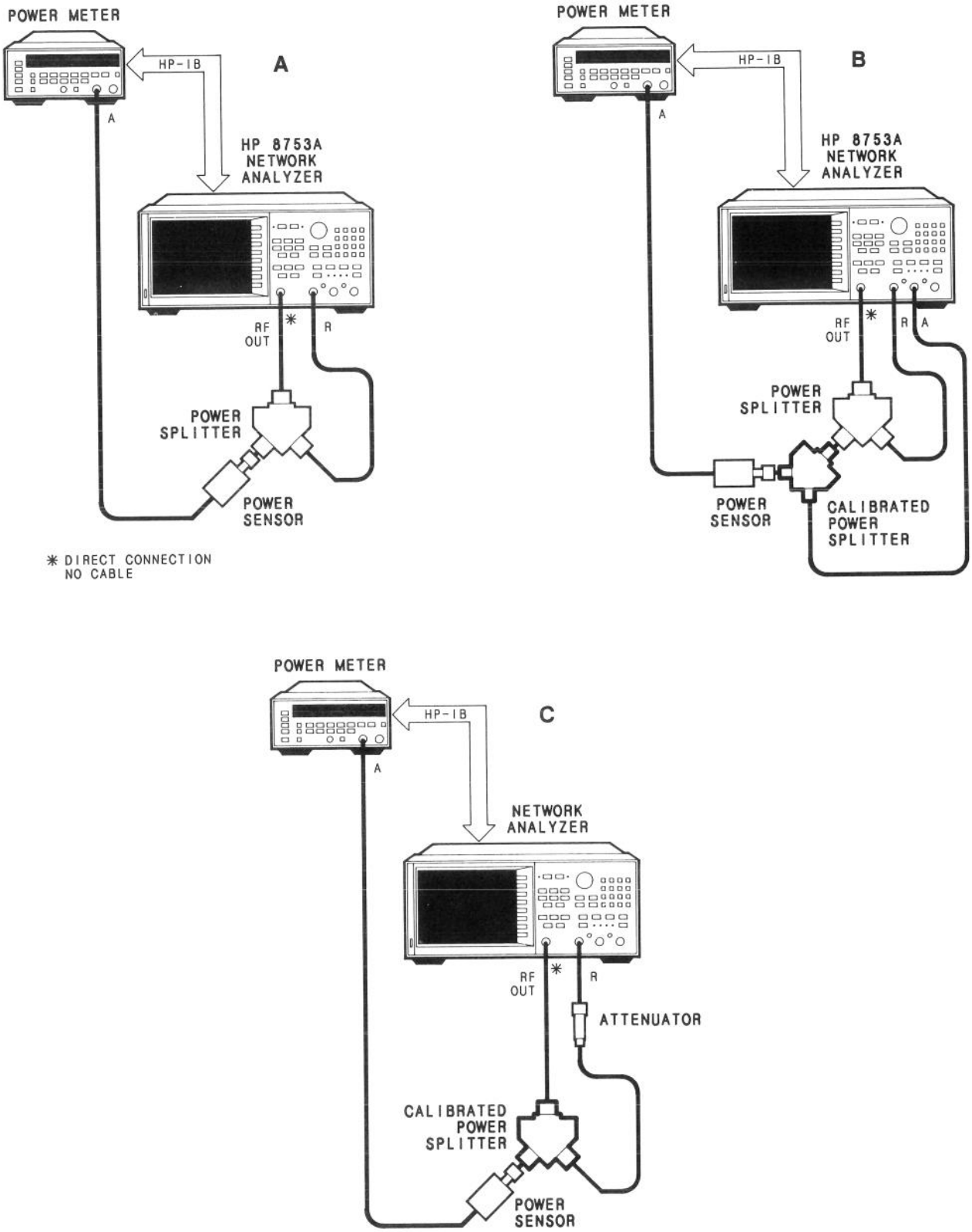


Figure 27. HP 8753A Source Adjustment Setups

EQUIPMENT

Power splitters (2)	HP 11667A option 001
Power meter	HP 436A option 022 or HP 438A
Power sensor	HP 8482A
RF cable set	HP 11851B
Attenuator (20 dB)	HP 8491A option 020

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper position as explained in "Correction Constant Jumper Position."

1. Set the LINE switch to on and allow the equipment 30 minutes to warm up.

2. On the HP 8753A press **[PRESET] [MEAS] [R]** to measure input R. Then press **[LOCAL] [SYSTEM CONTROLLER]** to control the power meter.

3. Press **[SET ADDRESSES] [ADDRESS: POWER MTR]** to see the address at which the analyzer expects to find the power meter (the default address is 13). The power meter must be set to the address indicated on the HP 8753A CRT. Refer to the power meter manual as required to observe or change its address. The HP 8753A key labeled **[POWER MTR: 438A]** toggles between 438A and 436A and **must** match your power meter model number. PRESET returns the selector to 438A. When connecting the power sensor to the HP 438A, use channel A.

Power Sensor Calibration Factor Entry

4. On the HP 8753A press **[SYSTEM] [SERVICE MENU] [TEST OPTIONS] [POWER SENSOR]** to access the calibration factor menu. (To enter accurate correction constants in this procedure, you must take into account the calibration factor for the power sensor of the power meter.)

5. In this menu you can build a table of up to twelve points (twelve frequencies with their cal factors). Frequency can be input as GHz or MHz by pressing the appropriate entry key. Cal factor percentages must be input as whole numbers (for example, enter CAL FACTOR 98% as 98). The cal factor and frequency values are found on the back of the HP 8482A power sensor.

6. If calibration factors have not been entered previously, the CRT will display "EMPTY". To add a point to the table, for example 1 GHz with a cal factor of 99%, press **[ADD] [FREQUENCY] [1] [G/n] [CAL FACTOR] [9] [9] [x1] [DONE]**.

7. When the table has two or more points (lines of data), the cursor will indicate the point which you can **[EDIT]** or **[DELETE]**. Use the **[SEGMENT]** softkey and the RPG knob or any key in the ENTRY area to review the table and position the cursor. Press **[DONE]** when you have finished entering the calibration factor data.

Power Loss through Power Splitter Determination

8. Zero and calibrate the power meter (refer to its manual as required).

9. Power splitters may present different attenuation at different frequencies. To increase the accuracy of the HP 8753A, measure the power loss between the input and the output of the power splitter to be connected to the power meter.

10. Connect the equipment as indicated in Figure 27 (a).

11. On the HP 8753A press **[MENU] [CW FREQ] [3] [0] [0] [k/m]** to generate a CW frequency of 300 kHz. Record the power meter reading in the first column, below.

Setup **A** Reading (First Reading)	Setup **B** Reading (Second Reading)	Power Loss (Enter in HP 8753A)
300 kHz: _____dB	minus _____dB	equals _____dB
50 MHz: _____dB	minus _____dB	equals _____dB
1.5 GHz: _____dB	minus _____dB	equals _____dB

12. Repeat the preceding step at 50 MHz and 1.5 GHz.

13. Reconfigure the equipment as shown in Figure 27 (b).

14. Repeat the measurements and note the power readings at 300 kHz, 50 MHz and 1.5 GHz in the second column, above.

15. Subtract the second column at each frequency from the first column and enter the difference (a positive number) in the third column.

16. On the HP 8753A press **[SYSTEM] [SERVICE MENU] [TEST OPTIONS] [POWER LOSS]** and enter the power loss data in the same way you entered the calibration factors.

Source Correction Routine

17. Press **[LOCAL] [SET ADDRESSES]** to confirm that the power meter model number displayed is correct. Press **[SYSTEM] [SERVICE MENU] [TESTS] [4] [7] [x1]** to display "Source Cor" on the CRT. Then press **[EXECUTE TEST]** to enter the source correction routine and begin the procedure.

18. Press **[YES]** at the prompt to alter the correction constants. Connect the equipment as shown in Figure 27 (c) when prompted.

19. Press **[CONTINUE]** to run the test.

20. At the prompt, use the RPG knob to position the marker at the point (or knee) where the power begins to roll off more quickly than at the lower frequencies. To see the effect of this adjustment position the marker anywhere on the center line and press **[CONTINUE]**. You can reposition the marker as many times as required to achieve the flattest line. If there is no appreciable roll-off, position the marker at 3 GHz.

21. Press **[SELECT]** to select the marker position which most effectively flattens the trace.

22. The test status indicator "DONE" signals the successful conclusion of this routine. The test status indicator "FAIL" is best handled by performing this procedure again. In case of continued failure, refer to "Source Troubleshooting" in the Service section of this manual.

IF AMPLIFIER CORRECTION CONSTANTS

DESCRIPTION

An IF amplifier boosts signal levels of inputs A and B. For signal levels greater than −30 dBm, attenuation is switched in. This switchable amplifier extends the instrument's dynamic range but can introduce a discontinuity. The IF amplifier correction constants compensate for this possible discontinuity.

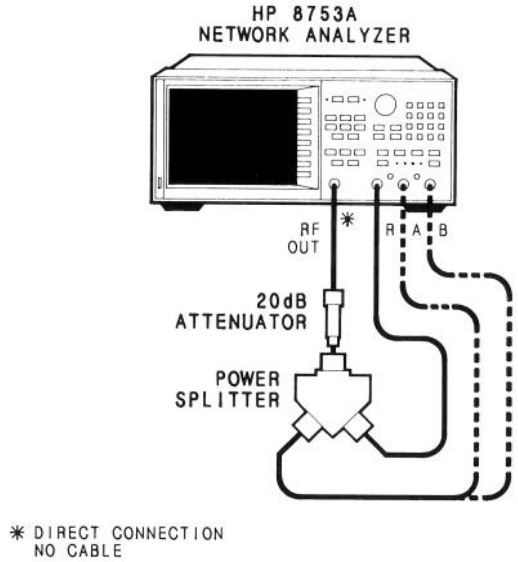


Figure 28. IF Amplifier Correction Constants Setup.

EQUIPMENT

Power splitter	HP 11667A option 001
Attenuator	HP 8491A option 020
RF cable set	HP 11851B

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper position as explained in "Correction Constant Jumper Position."

1. Turn on the instrument, press **[PRESET]** and allow 30 minutes warm-up time.
2. Connect the equipment as illustrated in Figure 28, with the power splitter connected to inputs R and A.

3. Press **[SYSTEM] [SERVICE MENU] [TESTS] [5] [1] [x1]** to enter the IF amplifier correction constants menu. Then press **[EXECUTE TEST]** when "IF Step Cor" appears to begin the routine.
4. Press **[YES]** at the prompt to alter the correction constants.
5. At the next prompt, connect the splitter to inputs R and A as illustrated in Figure 28. Then press **[CONTINUE]**.
6. At the following prompt, disconnect the cable from input A and connect it to input B. Then press **[CONTINUE]**.
7. The "DONE" test status indicator means that the IF amplifier correction constants have been stored.
8. Refer to the Service section in case of difficulty.
9. This concludes the IF Amplifier Correction Constant procedure.

CAVITY OSCILLATOR FREQUENCY CORRECTION CONSTANTS

DESCRIPTION

The frequency of the cavity oscillator varies with temperature. This procedure determines the precise frequency of the cavity oscillator at a particular temperature. The instrument accomplishes this by sweeping through 5 MHz spans to display known spurs. When the operator identifies the target spur, the network analyzer is able to calculate the frequency of the cavity oscillator as a correction constant. The target spur's apparent nominal frequency is 2.982 GHz.

This procedure *should* be performed with one of the recommended filters. The filter makes spur identification substantially faster and more reliable. With the filter, the operator need distinguish between only two spurs, each of which should be 10 dB to 20 dB (3 to 4 divisions) above the trace noise.

Without the filter, the target spur is one of four or five spurs, each of which may be 0.002 to 0.010 dB (invisible to 2 divisions) **above or below** the trace noise. If the recommended filters are not available, try to use a filter with at least 50 dB rejection at 2.9 GHz and a passband at 800 MHz.

NOTE: Use a filter if at all possible. Perform the first seven steps of the procedure at least once for familiarization before trying to select the target spur (especially if you lack a filter or prior experience).

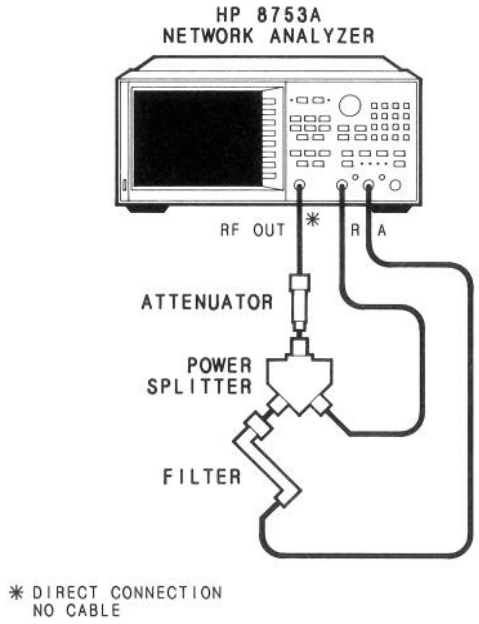


Figure 29. Cavity Oscillator Frequency Correction Constant Setup.

EQUIPMENT

Attenuator (20 dB)	HP 8491A option 020
Power splitter	HP 11667A option 001
Low-pass filter	HP 360B/C (fc=1.2/2.2 GHz)
RF cable set	HP 11851B

PROCEDURE

NOTE: To store correction constants in the HP 8753A, put the A9 CPU board jumper in the upper position as explained in "Correction Constant Jumper Position."

1. Connect the equipment as shown in Figure 29, turn on the HP 8753A and press **[PRESET]**. Allow 30 minutes for warm-up.
2. Press **[SYSTEM] [SERVICE MENU] [TESTS] [5] [4] [x1]** to access the cavity oscillator correction constant menu.
3. Press **[EXECUTE TEST]** to enter the routine. Then press **[YES]** at the prompt to alter the correction constants with new data.
4. During this adjustment routine, you will see several softkeys:

   [CONTINUE] sweeps the current frequency span with a set of three consecutive sweeps and then holds. May be pressed repeatedly for additional looks at the current frequency span.

   [NEXT] sweeps a frequency span 2 MHz higher than the current span. Press this key to observe the next frequency span.

   [SELECT] identifies the spur after the marker has been positioned on it by use of the front panel knob. The marker is automatically placed in the center of the display and need only be moved as desired.

   [ABORT] exits the routine.

5. Press **[CONTINUE]** to sweep the first frequency span. Note that **[CONTINUE]** sweeps the current span three times to increase the visibility of the spurs. This repetition is especially important when searching for the spurs without a filter. Note too that each new span overlaps the previous span by 3 MHz (the center frequency increases by 2 MHz; the span is 5 MHz). Thus anything visible on the right half of the display on one set of sweeps will appear on the left half or center of the display on the "NEXT" set of sweeps.
6. Press **[NEXT]** repeatedly. Watch the trace on each sweep and try to spot the target spur. With the filter, the target spur will be one of two obvious spurs (see Figure 30). Without the filter (not recommended), it will be one of four or five less distinct spurs as shown in Figures 31, 32, and 33. When the center frequency increases to 2994.999 MHz, "Cav Osc Cor FAIL" will appear on the display.
7. If you think you spotted the target spur, continue with step 8 (filter procedure) or step 12 (filterless procedure). Otherwise repeat steps 3 through 6.

Spur Search Procedure with Filter

8. Press **[EXECUTE TEST] [YES]** and **[CONTINUE]** to reenter the cavity oscillator frequency routine. Then press the softkeys as required to observe and mark the target spur. With the filter, the target spur will appear to the right of a second spur, similar to Figure 30.

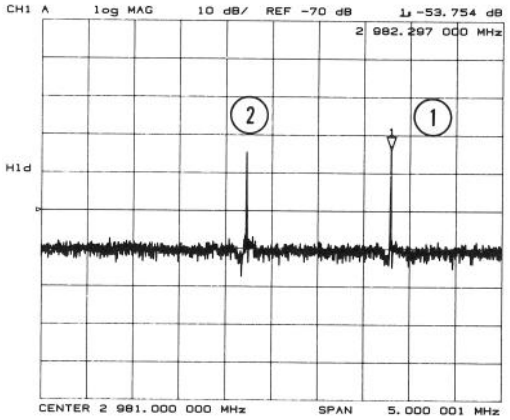


Figure 30. Typical Display of Spurs with Filter.

9. Rotate the RPG knob to position the marker on the spur. Then press **[SELECT]** to select the frequency of the marker as a correction constant and enter it in memory.

10. The test status indicator "DONE" signals the successful conclusion of this procedure.

11. If "DONE" does not appear or if "FAIL" or "Correction Constants not stored" does appear, refer to the Service section.

Spur Search Procedure without Filter

12. Press **[EXECUTE TEST] [YES]** and **[CONTINUE]** to reenter the cavity oscillator frequency routine. Then press the softkeys as required to observe and mark the target spur.

13. Without the filter the target spur will appear in a variety of disguises. Often it will be difficult to identity positively; ocassionally it will be nearly impossible to identify. Do not hesitate to press **[CONTINUE]** as many times as necessary to thoroughly inspect the current span.

    Without the filter, the target spur usually appears as one of a group of **four evenly spaced** spurs, as in Figure 31. The target spur is the right-most spur (fourth from the left). On any particular sweep one, any or all of the spurs may be large, small, visible, invisible, above or below the reference line.

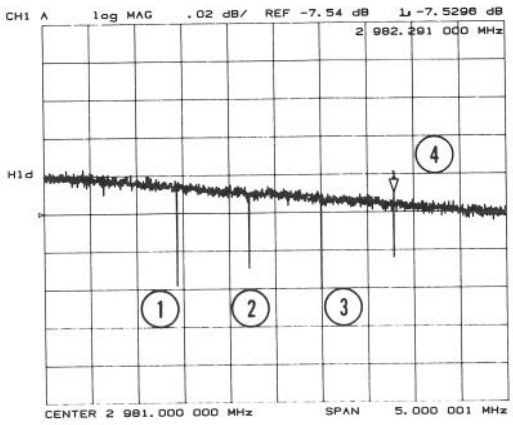


Figure 31. Typical Display of Four Spurs without Filter.

On occasion the target spur appears as one of a group of **five evenly spaced** spurs, as in Figure 32. The target spur is again the fourth from the left (not the fifth, right-most spur).

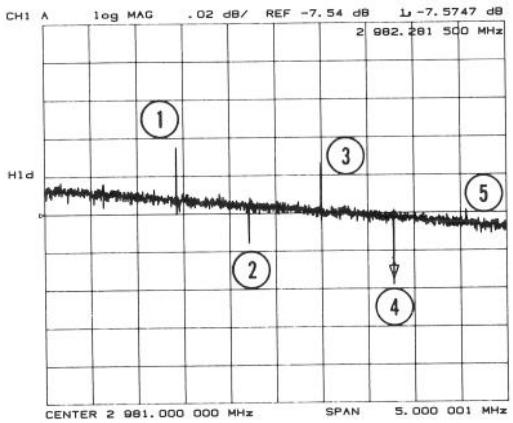


Figure 32. Typical Display of Five Spurs without Filter.

Figure 33 shows another variation of the basic four spur pattern: some up, some down and the target spur itself almost indistinguishable.

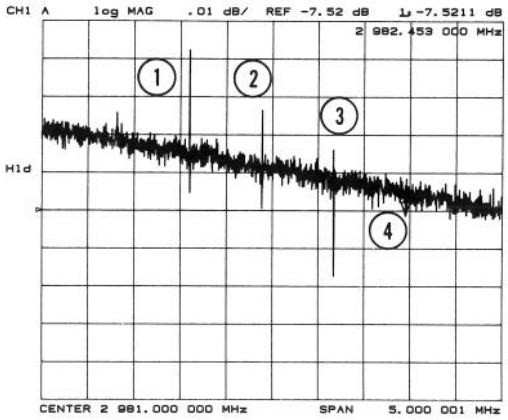


Figure 33. Variation of Display of Four Spurs without Filter.

14. Rotate the RPG knob to position the marker on the target spur. Then press **[SELECT]** to select the frequency of the marker as a correction constant and enter it in memory.

15. The test status indicator "DONE" signals the successful conclusion of this procedure.

16. If "DONE" does not appear or if "FAIL" or "Correction Constants not stored" does appear, refer to the Service section.

Replaceable Parts

INTRODUCTION

This section contains information for ordering replaceable parts. HP 8753A replaceable parts include major assemblies and all chassis hardware. In general, parts of major assemblies are not included. Table 1 lists major reference designations and abbreviations to help interpret part descriptions in the replaceable parts lists that follow. Table 1 also contains names and addresses that correspond to manufacturer code numbers listed after each replaceable part.

REBUILT-EXCHANGE ASSEMBLIES

Under the rebuilt-exchange assembly program, certain factory-repaired and tested modules (assemblies) are available on a trade-in basis. These assemblies are offered for lower cost than a new assembly, but meet all factory specifications required of a new assembly.

The defective assembly must be returned for credit under the terms of the rebuilt-exchange assembly program. Any spare assembly stock desired should be ordered using the new assembly part number. Figure 1 illustrates the module exchange procedure. Figure 2 shows all major assemblies, including those that can be replaced on an exchange basis.

REPLACEABLE PARTS LIST

Figures 2 through 18 assist in location and identification of all HP 8753A replaceable parts. Table 2 is a list of miscellaneous replaceable accessories. Figures 2 through 18 include corresponding lists that provide the following information:

1. Hewlett-Packard part number.
2. Part number check digit (CD).
3. Part quantity as shown in the corresponding figure. There may or may not be more of the same part located elsewhere in the instrument.
4. Part description, using abbreviations in Table 1.
5. A typical manufacturer of the part in a five-digit code (refer to the Manufacturers Code List in Table 1 for addresses).
6. The manufacturer's part number.

ORDERING INFORMATION

To order a part listed in the replaceable parts lists, quote the Hewlett-Packard part number (with the check digit), indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts lists, include the instrument model number, complete instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

Table 1. Reference Designations, Abbreviations, and Manufacturers Code List (1 of 2)

REFERENCE DESIGNATIONS

A . . . . . Assembly
AT . . . . . Attenuator, Isolator, Limiter, Termination
B . . . . . Fan, Motor
C . . . . . Capacitor
CP . . . . . Coupler
CR . . . . . Diode, Diode Thyristor, Step Recovery Diode (SCR), Varactor
DS . . . . . Annunciator, Lamp, Light Emitting Diode (LED), Signaling Device (Audible or Visible)
E . . . . . Miscellaneous Electrical Part
F . . . . . Fuse
FL . . . . . Filter
H . . . . . Hardware
J . . . . . Electrical Connector (Stationary Portion), Jack
K . . . . . Relay
L . . . . . Coil, Inductor
M . . . . . Meter
MP . . . . . Miscellaneous Mechanical Part
P . . . . . Electrical Connector (Movable Portion), Plug
Q . . . . . Silicon Controlled Rectifier (SCR), Transistor, Triode Thyristor
R . . . . . Resistor
RT . . . . . Thermistor
S . . . . . Switch
T . . . . . Transformer
TB . . . . . Terminal Board
TP . . . . . Test Point
U . . . . . Integrated Circuit, Microcircuit
V . . . . . Electron Tube
VR . . . . . Breakdown Diode (Zener), Voltage Regulator
W . . . . . Cable, Transmission Path, Wire
X . . . . . Socket
Y . . . . . Crystal Unit (Piezoelectric, Quartz)
Z . . . . . Tuned Cavity, Tuned Circuit

ABBREVIATIONS

A

ADJ . . . . . Adjust, Adjustment
AL . . . . . Aluminum
AMP . . . . . Amperage
ANDZ . . . . . Anodized

B

BCKT . . . . . Bracket
BD . . . . . Board, Bundle
BNC . . . . . Type of Connector

C

C . . . . . Capacitance, Capacitor, Center Tapped, Centistoke, Ceramic, Cermet, Circular Mil Foot, Closed Cup, Cold, Compression
CBL . . . . . Cable
CER . . . . . Ceramic
CHAM . . . . . Chamfer
CHAN . . . . . Channel
COM . . . . . Commercial, Common
CONN . . . . . Connect, Connection, Connector
CONT . . . . . Contact, Continuous, Control, Controller
CRP . . . . . Crepe, Crimp
CTR . . . . . Center
CURRNT . . . . . Current

D

D . . . . . Deep, Depletion, Depth, Diameter, Direct Current
DB . . . . . Decibel, Double Break
DBL . . . . . Double
DEG . . . . . Degree

E

EXCL . . . . . Excluding, Exclusive
EXT . . . . . Extended, Extension, External, Extinguish

F

F . . . . . Fahrenheit, Farad, Female, Film (Resistor), Fixed, Flange, Flint, Fluorine, Frequency
FDTHRU . . . . . Feed Through
FF . . . . . Flange, Female Connection; Flip Flop
FL . . . . . Flash, Flat, Fluid
FLEX . . . . . Flexible
FLG . . . . . Flange
FLTR . . . . . Filter, Floater
FT . . . . . Current Gain Bandwidth Product (Transition Frequency); Feet, Foot
FXD . . . . . Fixed

G

GEN . . . . . General, Generator
GHZ . . . . . Gigahertz
GP . . . . . General Purpose Group
GRN . . . . . Green
GRV . . . . . Grooved

H

H . . . . . Henry, Hermaphrodite, High, Hole Diameter, Hot, Hub Inside Diameter, Hydrogen
HD . . . . . Hand, Hard, Head, Heavy Duty
HEX . . . . . Hexadecimal, Hexagon, Hexagonal
HGT . . . . . Height

I

ID . . . . . Identification, Inside Diameter
IN . . . . . Inch, Indium
INS . . . . . Insert, Inside, Insulation, Insulator
INT . . . . . Integral, Intensity, Internal
INTL . . . . . Internal, International

K

K . . . . . Kelvin, Key, Kilo, Potassium
KB . . . . . Knob

Table 1. Reference Designations, Abbreviations, and Manufacturers Code List (2 of 2)

L

LED .... Light Emitting Diode
LG ..... Length, Long
LKG ..... Leakage, Locking
LKWR ..... Lockwasher

M

M ..... Male, Maximum, Mega, Mil, Milli, Mode, Momentary, Mounting Hole Centers, Mounting Hole Diameter
MA ..... Milliampere
MIN ..... Miniature, Minimum, Minor, Minute
MLD ..... Mold, Molded
MM ..... Magnetized Material (Restricted Articles Code), Millimeter
MO ..... Metal Oxide, Millionce, Molybdenum
MOM ..... Momentary, Motherboard
MTG ..... Mounting
MTLC ..... Metallic
MULTR ..... Multiplier
MW ..... Milliwatt

N

NB ..... Niobium
NCH ..... Notched
NEG ..... Negative
NH ..... Nanohenry
NM ..... Nanometer, Nonmetallic
NS ..... Nanosecond, Non-Shorting, Nose
NYL ..... Nylon (Polyamide)

O

OD ..... Olive Drab, Outside Diameter Amplifier

P

PAN-HD ..... Pan Head
PC ..... Picocoulomb, Piece, Printed Circuit
P.C. ..... Printed Circuit
PCB ..... Printed Circuit Board
PD ..... Pad, Palladium, Pitch Diameter, Power Dissipation
PF ..... Picofarad; Pipe, Female Connection; Power Factor
PKG ..... Package
PL-MTG ..... Plate Mounting
PLSTC ..... Plastic
PN ..... Part Number
POLYC ..... Polycarbonate
POLYE ..... Polyester
POLYI ..... Polyimide
POS ..... Position, Positive
POZI ..... Pozidrive Recess
PRCN ..... Precision
PRIM ..... Primary
PRL ..... Parallel
PRP ..... Purple, Purpose
P/S ..... Power Supply
PT ..... Part, Pint, Platinum, Point, Pulse Time
PVC ..... Polyvinyl Chloride

Q

QUAD ..... Set of Four

R

RBN ..... Ribbon
RCVR ..... Receiver
RECT .... Rectangle, Rectangular, Rectifier
RFI ..... Radio Frequency Interference
RND ..... Round
RVT ..... Rivet, Riveted

S

SCR ..... Screw, Scrub, Silicon Controlled Rectifier
SEC ..... Secondary
SER ..... Serial, Series
SGL ..... Single
SHFT ..... Shaft
SHLDR ..... Shoulder
SIG ..... Signal, Significant
SKT ..... Skirt, Socket
SLDR ..... Solder
SM ..... Samarium, Seam, Small, Square Meter, Sub Modular, Subminiature
SMB ..... Subminiature, B Type (Snap-On Connector)
SNP ..... Snap
SPCL ..... Special
SQ ..... Square
SST ..... Stainless Steel
STDF ..... Standoff
SZ ..... Size

T

T ..... Tab Width, Taper, Teeth, Temperature, Tera, Tesla, Thermoplastic (Insulation), Thickness, Time, Timed, Tooth, Turns Ratio, Typical
TA ..... Ambient Temperature, Tantalum
TC ..... Thermoplastic
TFE ..... Polytetrafluro - ethylene, Teflon
THD ..... Thread, Threaded
THK ..... Thick
TR ..... Rise Time, Truss
TRN ..... Turn, Turns

U

UCD ..... Microcandela

V

VDC ..... Volts, Direct Current

W

W ..... Watt, Wattage, White, Wide, Width, Wire
WD ..... Width, Wood

X

XSTR ..... Transistor

Y

YIG ..... Yytrium-iron-garnet

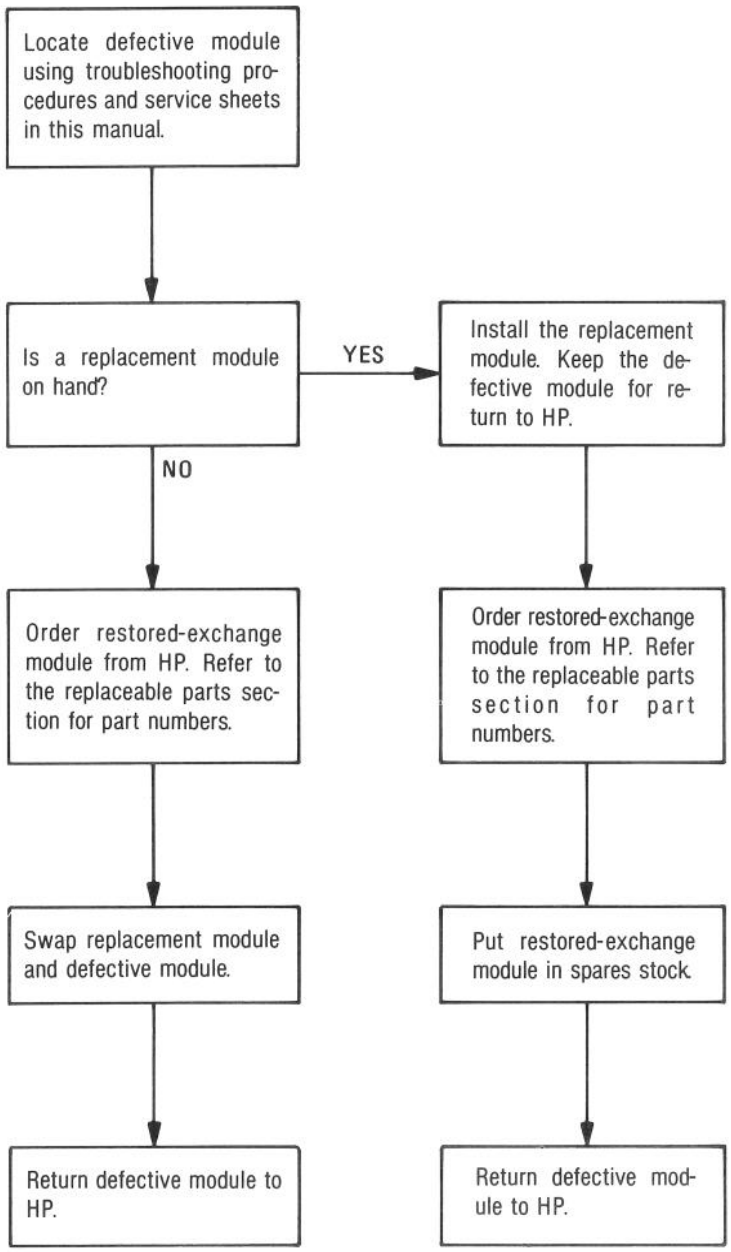
Z

ZN-P ..... Zinc Plate

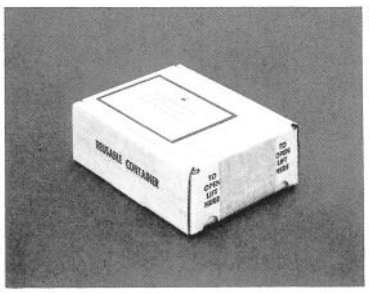
MANUFACTURERS CODE LIST

Mfr. Code	Manufacturer Name	Address		Zip Code
00000	Any Satisfactory Supplier			
06324	Glenair Inc.	Glendale	CA	91201
28480	Hewlett-Packard Company Corporate Hq.	Palo Alto	CA	94304

The module exchange program described here is a fast, efficient, economical method of keeping your Hewlett-Packard instrument in service.



A.



Restored-exchange modules are shipped individually in boxes like this. In addition to the circuit module, the box contains:

Exchange assembly failure report
Return address label

B.

Open box carefully - it will be used to return defective module to HP. Complete failure report. Place it and defective module in box. Be sure to remove enclosed return address label.

C.

Seal box with tape. Inside U.S.A.*, stick preprinted return address label over label already on box, and return box to HP. Outside U.S.A., do not use address label: instead address box to the nearest HP office.

*HP pays postage on boxes mailed in U.S.A.

Figure 1. Module Exchange Procedure

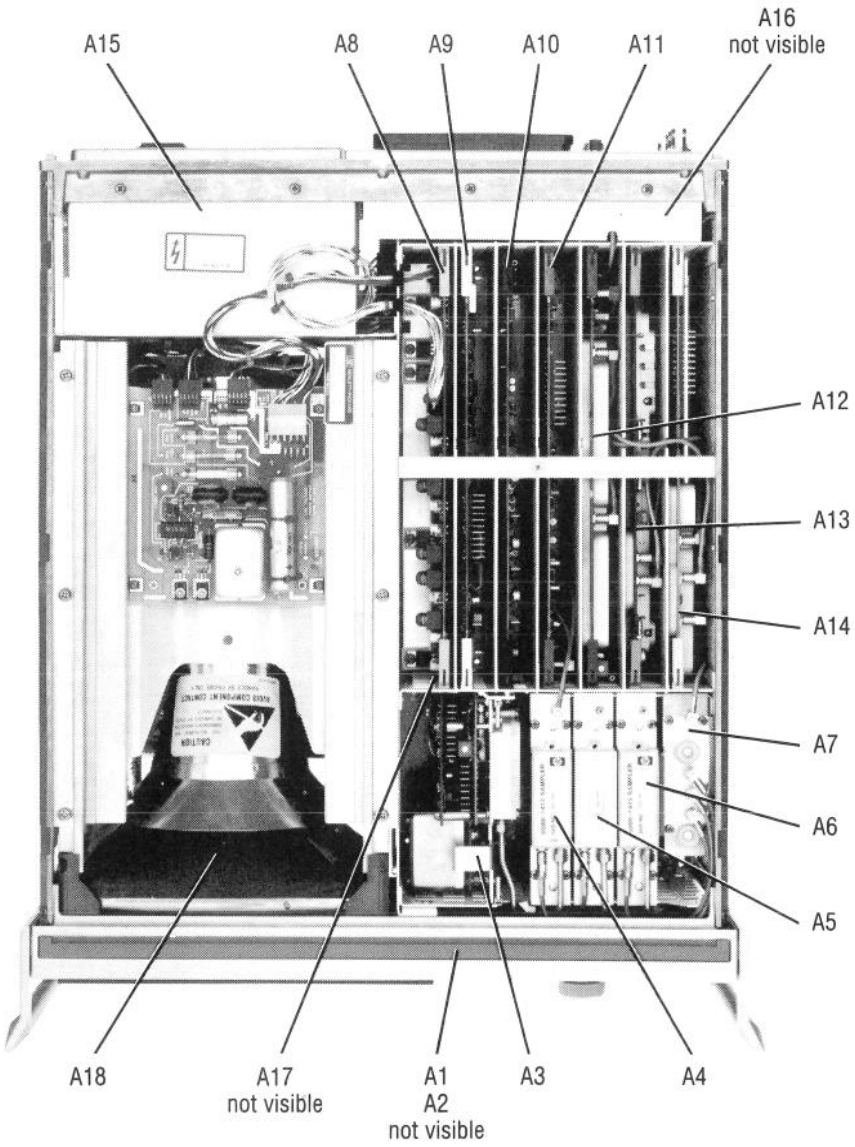


Figure 2. Major Assemblies (1 of 2)

Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
A1	08753-60001	9	1	FRONT PANEL KEYBOARD ASSEMBLY	28480	08753-60001
A1	08753-69001	7		FRONT PANEL KEYBOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69001
A2	08753-60002	0	1	FRONT PANEL INTERFACE BOARD ASSEMBLY	28480	08753-60002
A2	08753-69002	8		FRONT PANEL INTERFACE BOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69002
A3	08753-60003	1	1	SOURCE ASSEMBLY	28480	08753-60003
A3	08753-69003	9		SOURCE ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69003
A4	08753-60004	2	1	SAMPLER ASSEMBLY	28480	08753-60004
A4	08753-69004	0		SAMPLER ASSEMBLY (REBUILT-EXCHANGE) (INCLUDES SAMPLER/MIXER, BOARD, AND BOARD COVER)	28480	08753-69004
A5	08753-60004	2	1	SAMPLER ASSEMBLY	28480	08753-60004
A5	08753-69004	0		SAMPLER ASSEMBLY (REBUILT-EXCHANGE) (INCLUDES SAMPLER/MIXER, BOARD, AND BOARD COVER)	28480	08753-69004
A6	08753-60004	2	1	SAMPLER ASSEMBLY	28480	08753-60004
A6	08753-69004	0		SAMPLER ASSEMBLY (REBUILT-EXCHANGE) (INCLUDES SAMPLER/MIXER, BOARD, AND BOARD COVER)	28480	08753-69004
A7	08753-60007	5	1	PULSE GENERATOR BOARD ASSEMBLY	28480	08753-60007
A7	08753-69007	3		PULSE GENERATOR BOARD ASSEMBLY (REBUILT-EXCHANGE) (INCLUDES BOARD AND BOARD COVER)	28480	08753-69007
A8	08753-60108	7	1	POST-REGULATOR BOARD ASSEMBLY	28480	08753-60108
A8	08753-69108	5		POST-REGULATOR BOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69108
A9	08753-60009	7	1	CPU BOARD ASSEMBLY	28480	08753-60009
A9	08753-69009	5		CPU BOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69009
A10	08753-60010	0	1	DIGITAL IF BOARD ASSEMBLY	28480	08753-60010
A10	08753-69010	8		DIGITAL IF BOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69010
A11	08753-60060	0	1	PHASE LOCK BOARD ASSEMBLY	28480	08753-60060
A11	08753-69060	8		PHASE LOCK BOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69060
A12	08753-60012	2	1	REFERENCE BOARD ASSEMBLY	28480	08753-60012
A12	08753-69012	0		REFERENCE BOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69012
A13	08753-60013	3	1	FRACTIONAL N ANALOG BOARD ASSEMBLY	28480	08753-60013
A13	08753-69013	1		FRACTIONAL N ANALOG BOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-60013
A14	08753-60057	5	1	FRACTIONAL N DIGITAL BOARD ASSEMBLY	28480	08753-60057
A14	08753-69057	8		FRACTIONAL N DIGITAL BOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69057
A15	08753-60015	5	1	PREREGULATOR ASSEMBLY	28480	08753-60015
A15	08753-69015	3		PREREGULATOR ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69015
A16	08753-60016	6	1	REAR PANEL BOARD ASSEMBLY	28480	08753-60016
A16	08753-69016	4		REAR PANEL BOARD ASSEMBLY (REBUILT-EXCHANGE)	28480	08753-69016
A17	08753-60017	7	1	MOTHERBOARD ASSEMBLY (INCLUDES MOTHERBOARD RIVETED TO CAGE ASSEMBLY AND FRAME).	28480	08753-60017
A18	08753-60018	8	1	DISPLAY ASSEMBLY	28480	08753-60018

Figure 2. Major Assemblies (2 of 2)

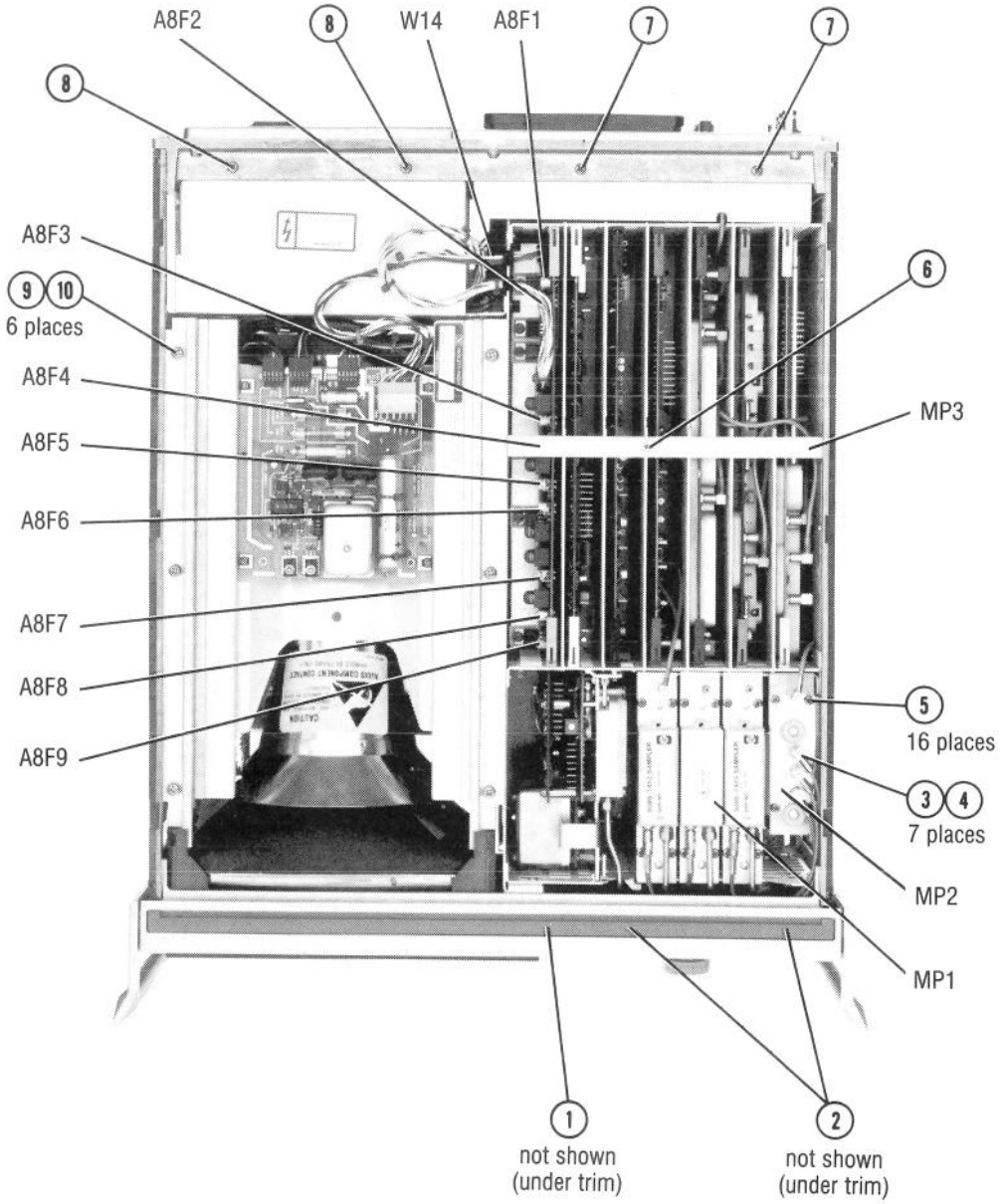


Figure 3. Top View, Attaching Hardware (1 of 2)

Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1*	0515-1331	5	1	SCREW-METRIC SPECIALTY M4 X 0.7 THD; 6		
2*	0515-1234	7	2	SCREW-MACH M3.5 X 0.6 8MM-LG	28480	0515-1234
3	2190-0124	4	7	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0124
4	2950-0078	9	7	NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	28480	2950-0078
5*	0515-0169	5	16	SCREW-MACHINE ASSEMBLY M3 X 0.5 10MM-LG	00000	Order by Desc.
6*	0515-1110	8	1	SCREW-MACH M3 X 0.5 12MM-LG PAN-HD	28480	0515-1110
7*	0515-1232	5	2	SCREW-MACH M3.5 X 0.6 8MM-LG PAN-HD	28480	0515-1232
8*	0515-1244	9	2	SCREW-MACHINE ASSEMBLY M3.5 X 0.6	28480	0515-1244
9*	0515-1368	8	6	SCREW-MACH M4 X 0.7 14MM-LG PAN-HD	28480	0515-1368
10*	3050-0893	9	6	WASHER-FL MTLC 4.0 MM 4.4-MM-ID	28480	3050-0893
A8F1	2110-0425	0	1	FUSE 2A 125V NTD .25X.27	28480	2110-0425
A8F2	2110-0424	9	1	FUSE .75A 125V NTD .25X.27	28480	2110-0424
A8F3	2110-0425	0	1	FUSE 2A 125V NTD .25X.27	28480	2110-0425
A8F4	2110-0424	9	1	FUSE .75A 125V NTD .25X.27	28480	2110-0424
A8F5	2110-0476	1	1	FUSE 4A 125V NTD .25X.27	28480	2110-0476
A8F6	2110-0425	0	1	FUSE 2A 125V NTD .25X.27	28480	2110-0425
A8F7	2110-0476	1	1	FUSE 4A 125V NTD .25X.27	28480	2110-0476
A8F8	2110-0047	2	1	FUSE 1A 125V NTD .25X.27	28480	2110-0047
A8F9	2110-0046	1	1	FUSE .5A 125V NTD .25X.27	28480	2110-0046
MP1	08753-00039	7	1	A5 ISOLATION GROUNDING CLIP	28480	08753-00039
MP2	08753-00040	0	1	A7 ISOLATION GROUNDING SHIELD	28480	08753-00040
MP3	08753-40004	0	1	PC BOARD STABILIZER	28480	08753-40004
W14				DISPLAY POWER CABLE ASSEMBLY – A8 TO A18 – SEE FIGURE 4		

* **CAUTION**: This hardware is metric. Use of other thread types is likely to damage threaded holes.

Figure 3. Top View, Attaching Hardware (2 of 2)

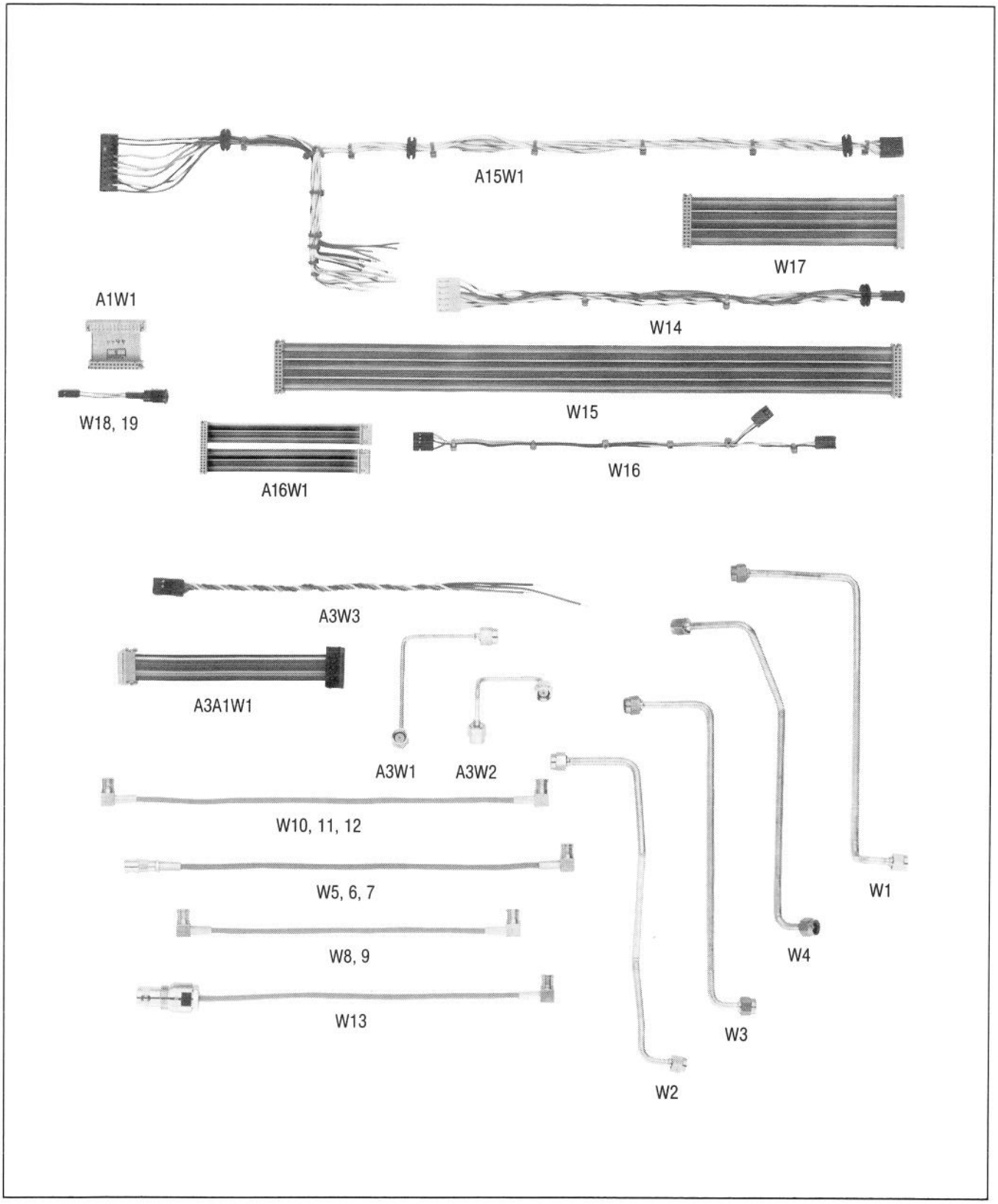
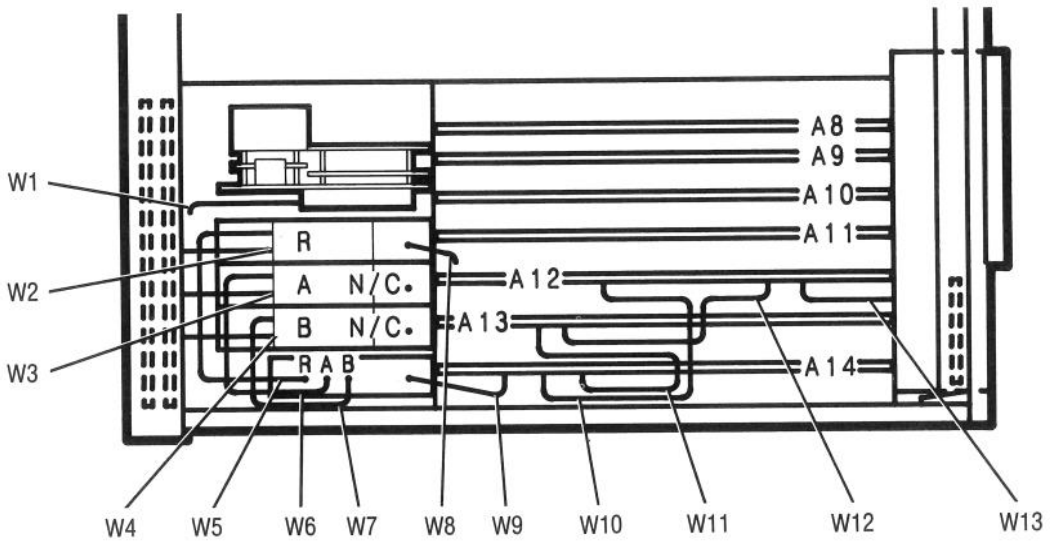
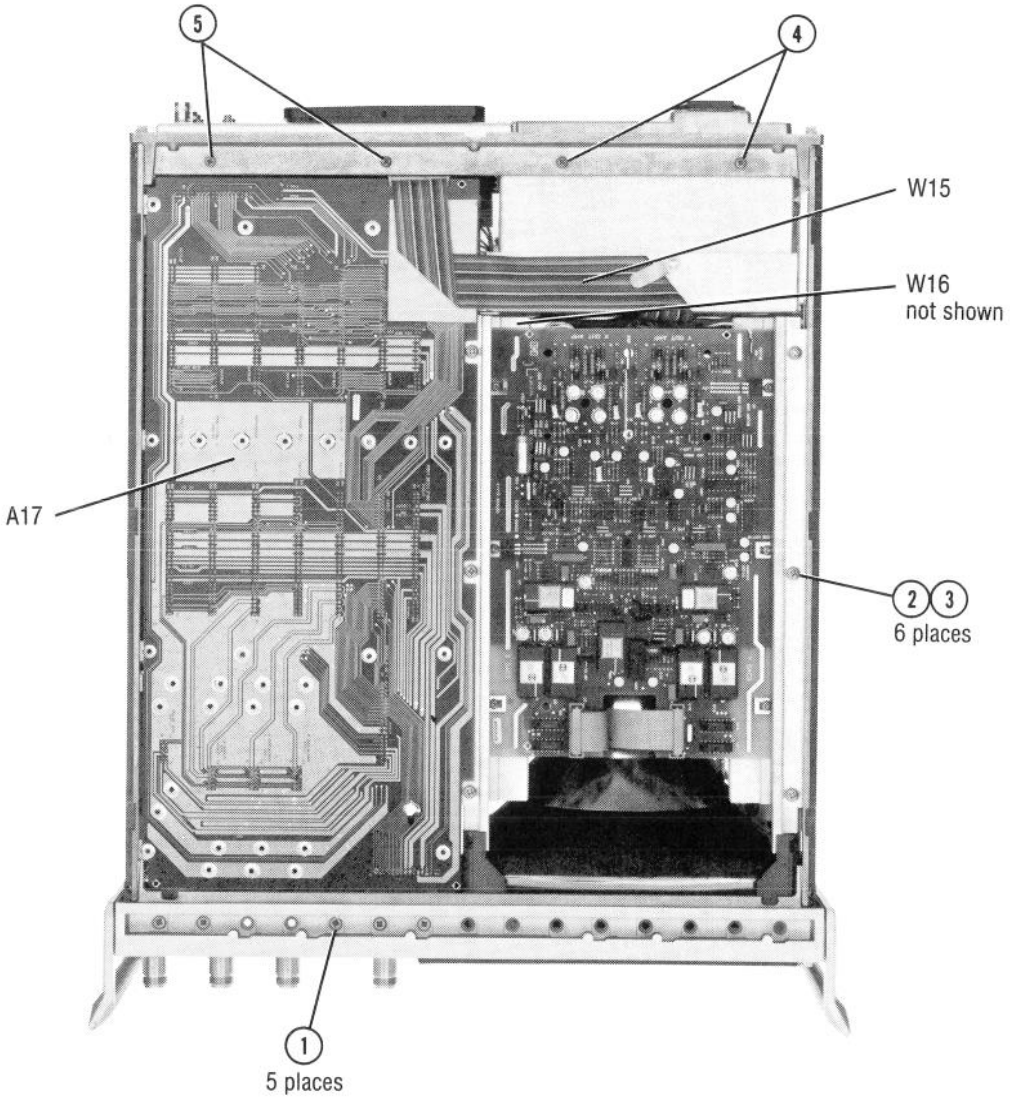


Figure 4. Cables (1 of 2)



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
A1W1	08753-60036	0	1	RIBBON CABLE ASSEMBLY – A1 TO A2 (PART OF A1)	28480	08753-60036
A3A1W1	08753-60034	8	1	RIBBON CABLE ASSEMBLY – YIG OSC. TO A3A1 (PART OF A3A1)	28480	08753-60034
A3W1	08753-20031	1	1	SEMI-RIGID CABLE ASSEMBLY – YIG OSC. OUTPUT	28480	08753-20031
A3W2	08753-20032	2	1	SEMI-RIGID CABLE ASSEMBLY – CAV. OSC. OUTPUT	28480	08753-20032
A3W3	08753-60035	9	1	CABLE ASSEMBLY – CAV. OSC. TO A3A1 (PART OF A3A4)	28480	08753-60035
A15W1	08753-60042	8	1	CABLE ASSEMBLY – A15 TO A8 AND A17 (PART OF A15)	28480	08753-60042
A16W1	08753-60033	7	1	RIBBON CABLE ASSEMBLY – A16 TO A17 (PART OF A16)	28480	08753-60033
W1	08753-20027	5	1	SEMI-RIGID CABLE ASSEMBLY – RF INPUT TO A3	28480	08753-20027
W2	08753-20028	6	1	SEMI-RIGID CABLE ASSEMBLY – R INPUT TO A4	28480	08753-20028
W3	08753-20029	7	1	SEMI-RIGID CABLE ASSEMBLY – A INPUT TO A5	28480	08753-20029
W4	08753-20030	8	1	SEMI-RIGID CABLE ASSEMBLY – B INPUT TO A6	28480	08753-20030
W5	08753-60027	9	1	FLEXIBLE RF CABLE ASSEMBLY – A4 TO A7	28480	08753-60027
W6	08753-60027	9	1	FLEXIBLE RF CABLE ASSEMBLY – A5 TO A7	28480	08753-60027
W7	08753-60027	9	1	FLEXIBLE RF CABLE ASSEMBLY – A6 TO A7	28480	08753-60027
W8	08753-60061	1	1	FLEXIBLE RF CABLE ASSEMBLY – A4 TO A11	28480	08753-60061
W9	08753-60061	1	1	FLEXIBLE RF CABLE ASSEMBLY – A7 TO A14	28480	08753-60061
W10	08753-60029	1	1	FLEXIBLE RF CABLE ASSEMBLY – A14 TO A12	28480	08753-60029
W11	08753-60029	1	1	FLEXIBLE RF CABLE ASSEMBLY – A14 TO A13	28480	08753-60029
W12	08753-60029	1	1	FLEXIBLE RF CABLE ASSEMBLY – A13 TO A12	28480	08753-60029
W13	08753-60026	8	1	FLEXIBLE RF CABLE ASSEMBLY – A12 TO REAR PANEL	28480	08753-60026
W14	08753-60044	0	1	DISPLAY POWER CABLE ASSEMBLY – A8 TO A18	28480	08753-60044
W15	08753-60038	2	1	RIBBON CABLE ASSEMBLY – A17 TO A18	28480	08753-60038
W16	08753-60041	7	1	FOCUS/INTENSITY CABLE ASSEMBLY – A17 TO A18	28480	08753-60041
W17	08753-60037	1	1	RIBBON CABLE ASSEMBLY – A2 TO A17	28480	08753-60037
W18	08753-60045	1	1	PROBE POWER CABLE ASSEMBLY – A2 TO FRONT PANEL (INCLUDES WIRES, CONNECTOR, AND JACK)	28480	08753-60045
W19	08753-60045	1	1	PROBE POWER CABLE ASSEMBLY – A2 TO FRONT PANEL (INCLUDES WIRES, CONNECTOR, AND JACK)	28480	08753-60045

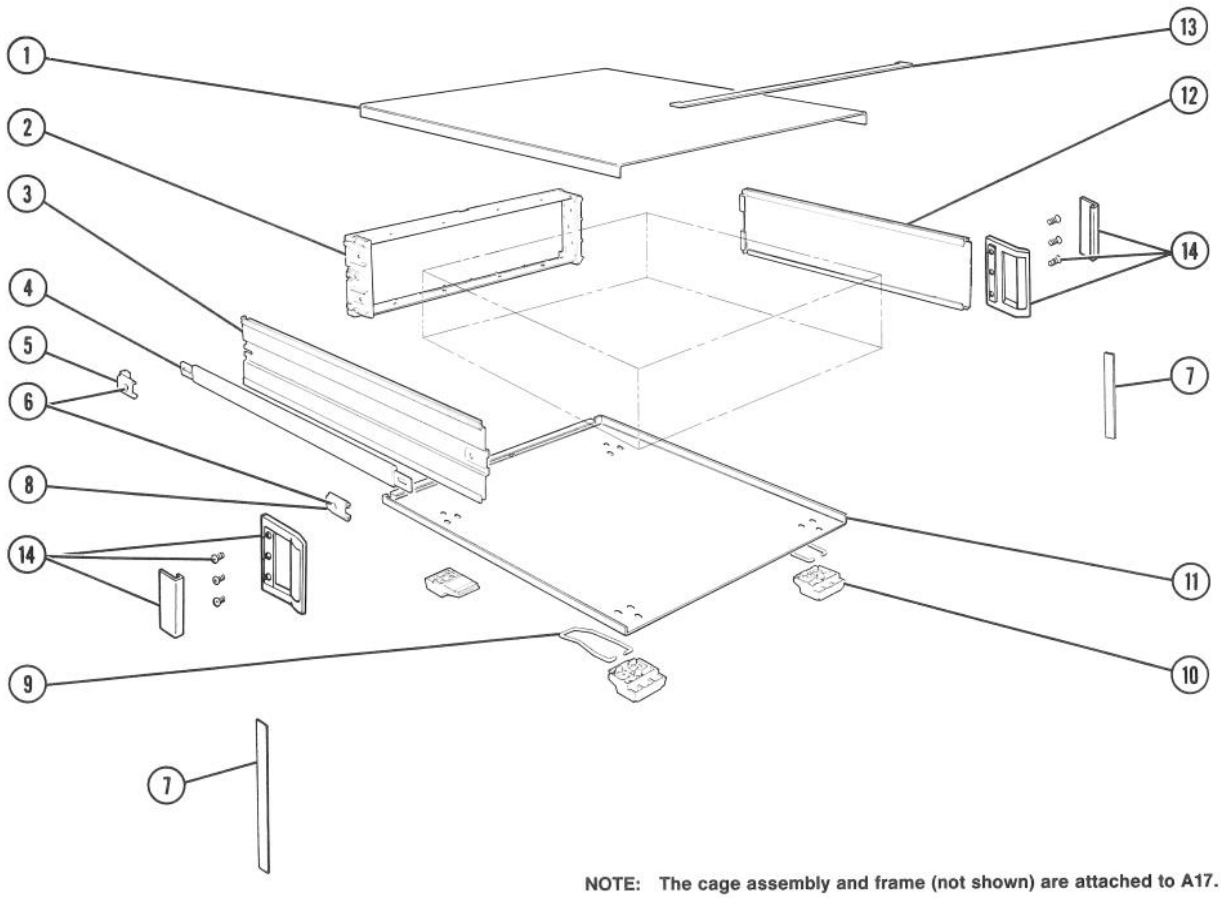
Figure 4. Cables (2 of 2)



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1*	0515-1234	7	5	SCREW-MACH M3.5 X 0.6 8MM-LG	28480	0515-1234
2*	0515-1368	8	6	SCREW-MACH M4 X 0.7 14MM-LG PAN-HD	28480	0515-1368
3*	3050-0893	9	6	WASHER-FL MTLC 4.0 MM 4.4-MM-ID	28480	3050-0893
4*	0515-1244	9	2	SCREW-MACHINE ASSEMBLY M3.5 X 0.6	28480	0515-1244
5*	0515-1232	5	2	SCREW-MACH M3.5 X 0.6 8MM-LG PAN-HD	28480	0515-1232
A17				MOTHERBOARD ASSEMBLY – SEE FIGURE 2		
W15				RIBBON CABLE ASSEMBLY – A17 TO A18 – SEE FIGURE 4		
W16				FOCUS/INTENSITY CABLE ASSEMBLY – A17 TO A18 – SEE FIGURE 4		

* **CAUTION**: This hardware is metric. Use of other thread types is likely to damage threaded holes.

Figure 5. Bottom View, Attaching Hardware

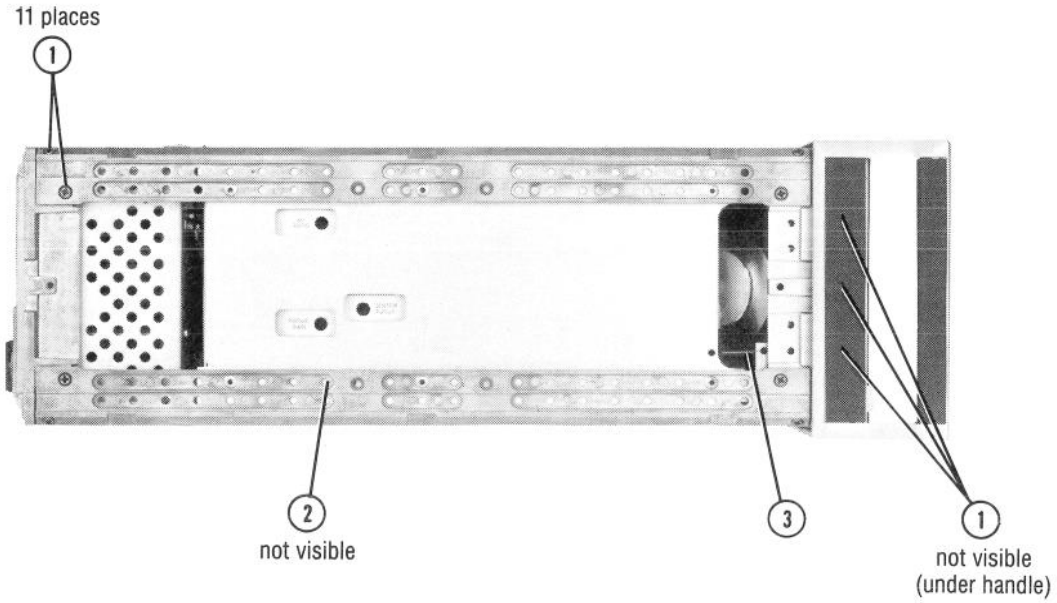


NOTE: The cage assembly and frame (not shown) are attached to A17.

Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1	5061-9435	8	1	COVER-TOP ASSY	28480	5061-9435
2	5021-5806	5	1	REAR FRAME	28480	5021-5806
3	5060-9942	0	1	COVER-SIDE-HANDLE	28480	5060-9942
4	5060-9804	3	1	STRAP HANDLE 18 IN.	28480	5060-9804
5	5041-6820	7	1	STRAP, HANDLE, CAP-REAR	28480	5041-6820
6*	0515-1132	4	2	SCREW-MACH M5 X 0.8 10MM-LG	28480	0515-1132
7	5001-0440	1	2	TRIM, SIDE (USED IF FRONT HANDLES ARE REMOVED)	28480	5001-0440
8	5041-6819	4	1	STRAP, HANDLE, CAP-FRONT	28480	5041-6819
9	1460-1345	5	2	TILT STAND SST	28480	1460-1345
10	5040-7201	8	4	FOOT (STANDARD)	28480	5040-7201
11	5061-9447	2	1	COV-BOTTOM ASSY	28480	5061-9447
12	5061-9517	7	1	COVER-SIDE-PERF	28480	5061-9517
13	5040-7202	9	1	TRIM, TOP	28480	5040-7202
14	5061-9690	7	1	FRONT HANDLE KIT	28480	5061-9690

* **CAUTION**: This hardware is metric. Use of other thread types is likely to damage threaded holes.

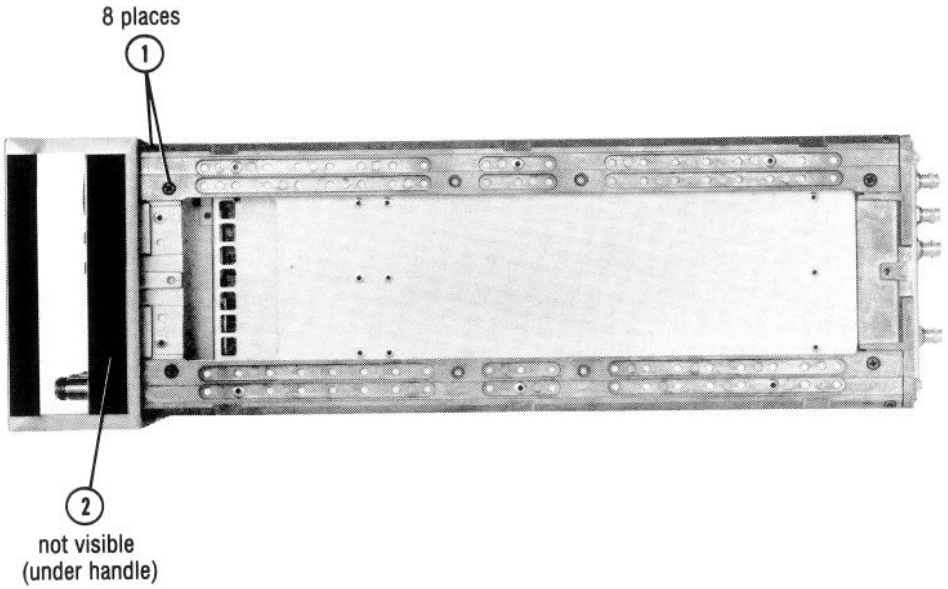
Figure 6. Chassis Parts



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1*	0515-1331	5	11	SCREW-METRIC SPECIALTY M4 X 0.7 THD; 6	28480	0515-1331
2*	0515-0886	3	1	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	28480	0515-0886
3	1460-1573	1	1	SPRING-EXT .138-IN-OD SST PSVT	28480	1460-1573

*** CAUTION:** This hardware is metric. Use of other thread types is likely to damage threaded holes.

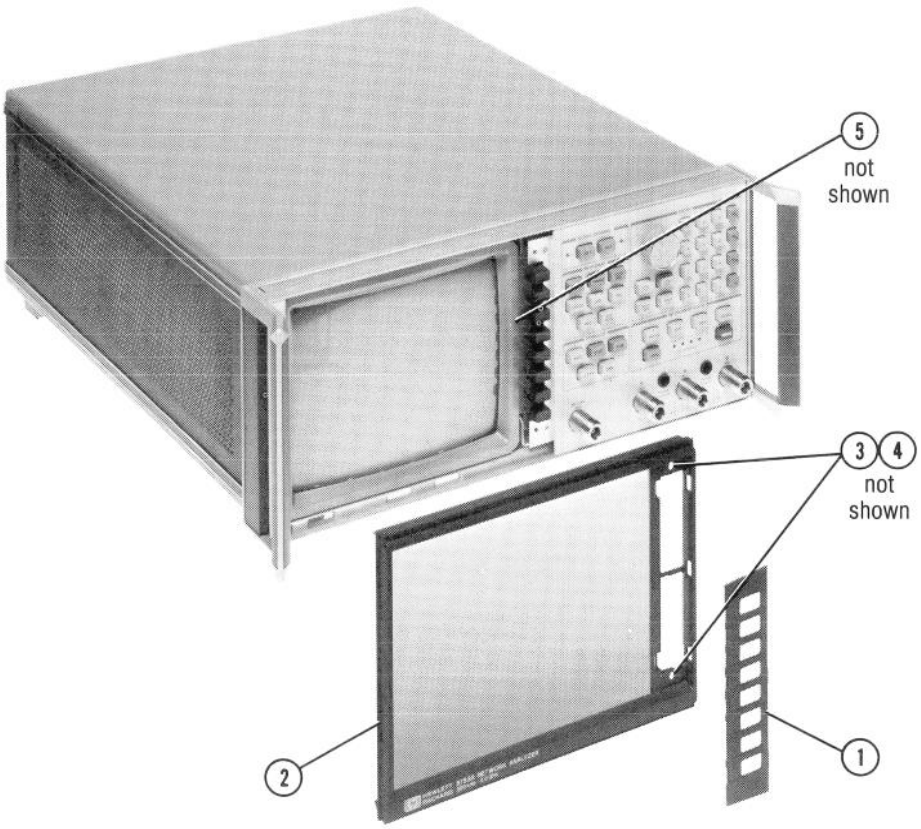
Figure 7. Left View, Attaching Hardware



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1*	0515-1331	5	8	SCREW-METRIC SPECIALTY M4 X 0.7 THD; 6	28480	0515-1331
2*	0515-1234	7	1	SCREW-MACH M3.5 X 0.6 8MM-LG	28480	0515-1234

* **CAUTION:** This hardware is metric. Use of other thread types is likely to damage threaded holes.

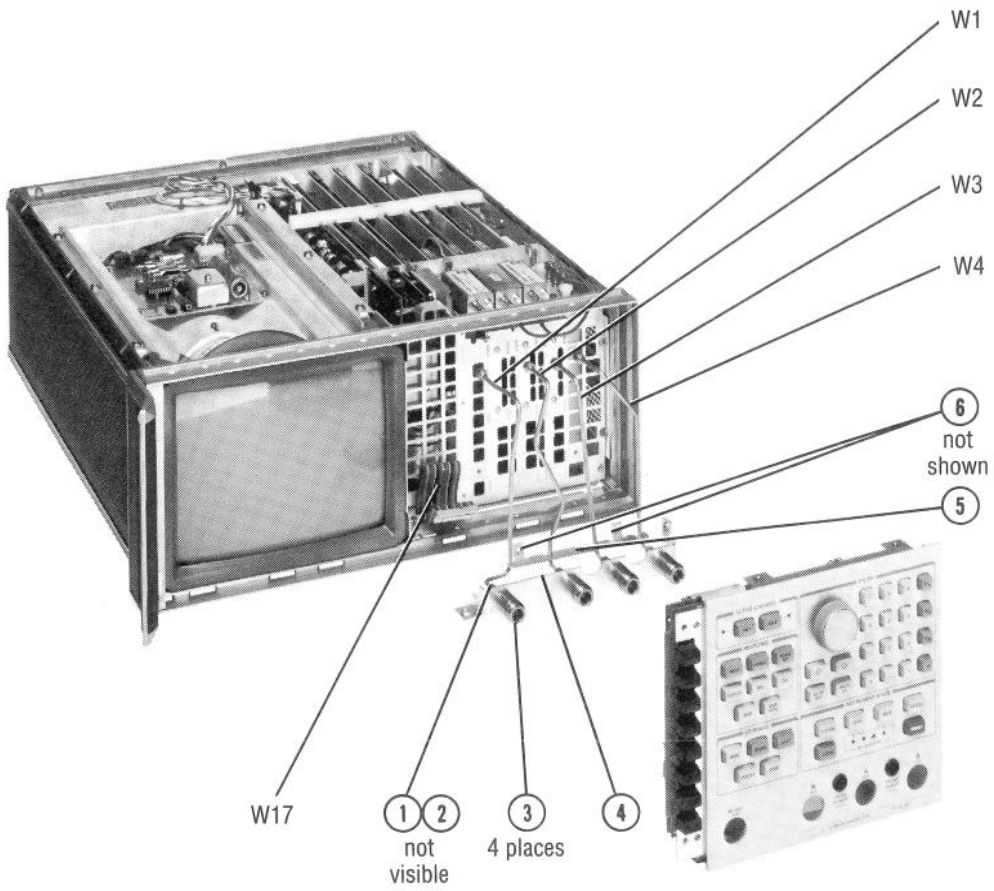
Figure 8. Right View, Attaching Hardware



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1	08753-40001	7	1	SOFTKEYS COVER	28480	08753-40001
2	08753-60046	2	1	DISPLAY BEZEL ASSEMBLY (INCLUDES GLASS)	28480	08753-60046
3	3050-1192	3	2	WASHER-FL MTLC 3.5 MM 3.8-MM-ID	28480	3050-1192
4*	0515-1232	5	2	SCREW-MACH M3.5 X 0.6 8MM-LG PAN-HD	28480	0515-1232
5				LABEL – PARALLAX SOFTKEY MENU – SEE FIGURE 18		

* **CAUTION:** This hardware is metric. Use of other thread types is likely to damage threaded holes.

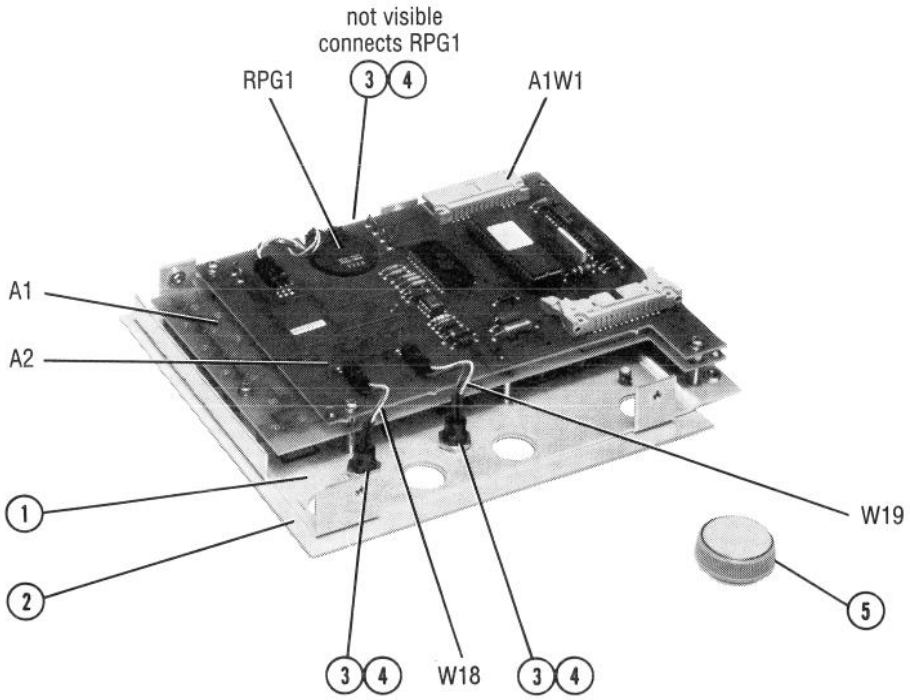
Figure 9. Display, Bezel Assembly



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1	2190-0104	0	4	WASHER-LK INTL T 7/16 IN .439-IN-ID	28480	2190-0104
2	2950-0132	6	4	NUT-HEX-DBL-CHAM 7/16-28-THD .094-IN-THK	00000	Order by Desc.
3	86290-60005	7	4	TYPE-N CONNECTORS	28480	86290-60005
4	08753-00003	5	1	TYPE-N CONNECTOR BRACKET	28480	08753-00003
5	08753-00021	7	1	CABLE SUPPORT BRACKET	28480	08753-00021
6*	0515-0886	3	2	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	28480	0515-0886
W1				SEMI-RIGID CABLE ASSEMBLY – RF INPUT TO A3 – SEE FIGURE 4		
W2				SEMI-RIGID CABLE ASSEMBLY – R INPUT TO A4 – SEE FIGURE 4		
W3				SEMI-RIGID CABLE ASSEMBLY – A INPUT TO A5 – SEE FIGURE 4		
W4				SEMI-RIGID CABLE ASSEMBLY – B INPUT TO A6 – SEE FIGURE 4		
W17				RIBBON CABLE ASSEMBLY – A2 TO A17 – SEE FIGURE 4		

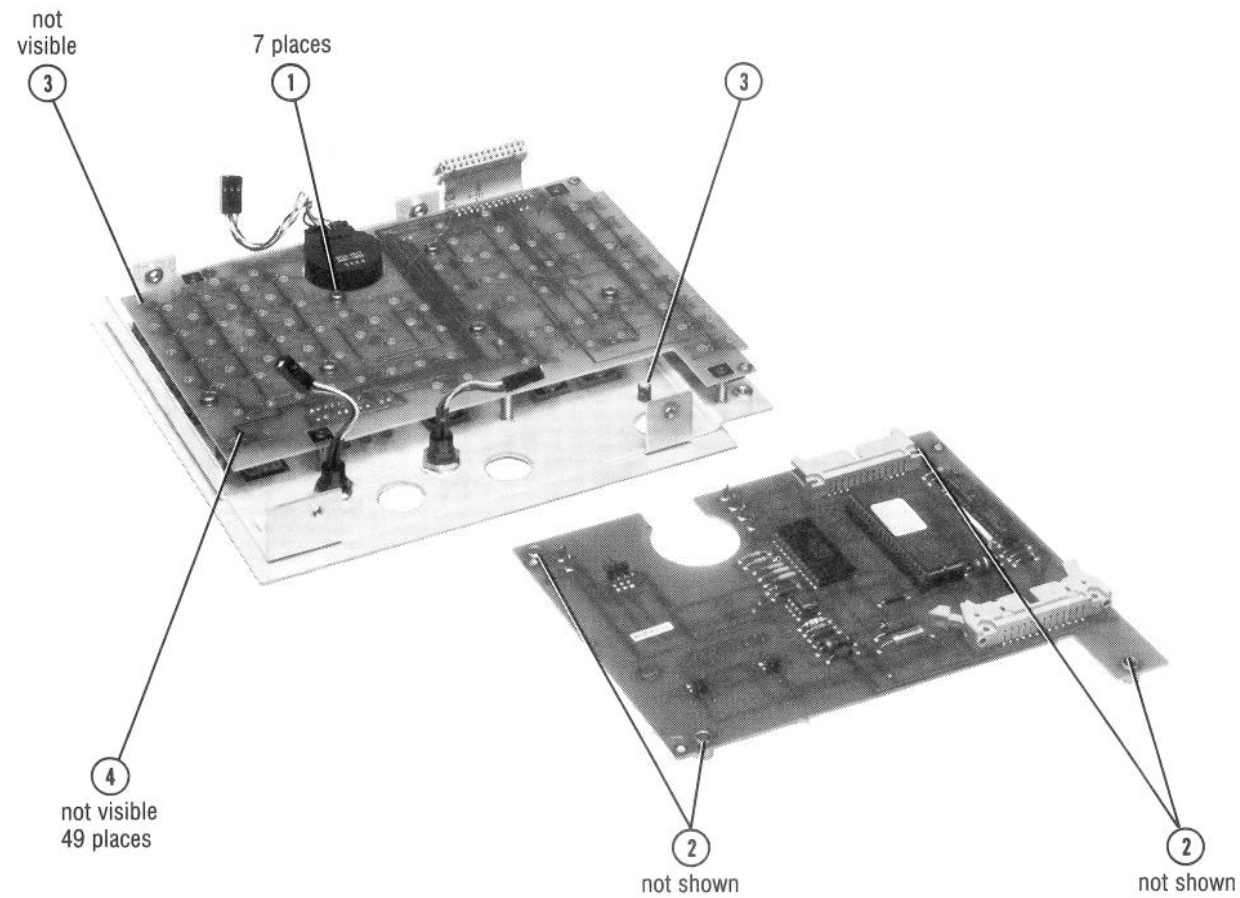
* **CAUTION**: This hardware is metric. Use of other thread types is likely to damage threaded holes.

Figure 10. Front Panel, RF Cables



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1	08753-00002	4	1	FRONT SUB-PANEL	28480	08753-00002
2	08753-00001	3	1	FRONT DRESS PANEL	28480	08753-00001
3	2190-0016	3	3	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
4	2950-0043	8	3	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	Order by Desc.
5	0370-2992	8	1	KNOB-BASE 1-1/8 JGK .252-IN-ID	28480	0370-2992
A1				FRONT PANEL KEYBOARD ASSEMBLY – SEE FIGURE 2		
A1W1				RIBBON CABLE ASSEMBLY – A1 TO A2 – SEE FIGURE 4		
A2				FRONT PANEL INTERFACE BOARD ASSEMBLY – SEE FIGURE 2		
RPG1	08757-60053	5	1	ROTARY PULSE GENERATOR (RPG)	28480	08757-60053
W18				PROBE POWER CABLE ASSEMBLY – A2 TO FRONT PANEL SEE FIGURE 4		
W19				PROBE POWER CABLE ASSEMBLY – A2 TO FRONT PANEL SEE FIGURE 4		

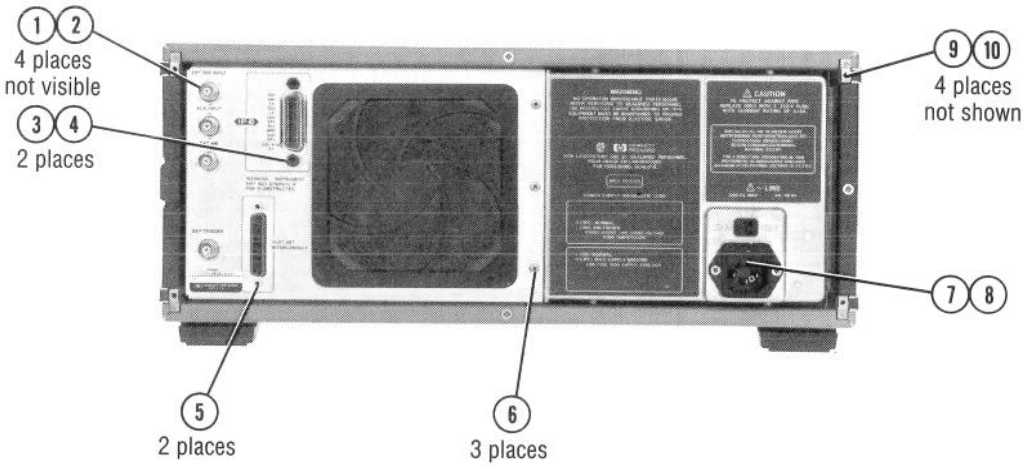
Figure 11. Front Panel, Assemblies



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1*	0515-0897	6	7	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD	28480	0515-0897
2*	0515-1112	0	4	SCREW-MACH M3 X 0.5 20MM-LG PAN-HD	28480	0515-1112
3	0510-1148	2	2	RETAINER-PUSH ON KB-TO-SHFT EXT	28480	0510-1148
4	5060-9436	7	49	SWITCH-PB SPST-NO MOM .1A 5 VDC	28480	5060-9436

* **CAUTION**: This hardware is metric. Use of other thread types is likely to damage threaded holes.

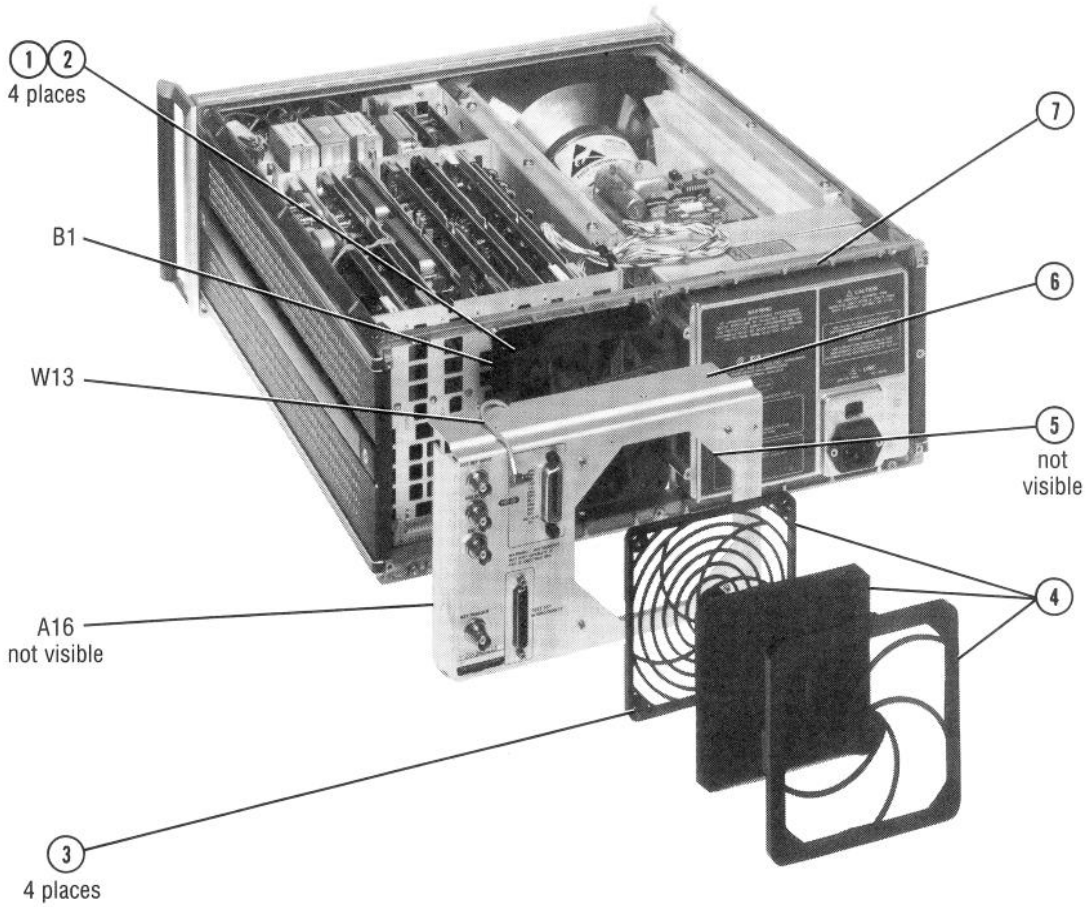
Figure 12. Front Panel, Attaching Hardware



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1	2190-0102	8	4	WASHER-LK INTL T 15/32 IN .472-IN-ID	28480	2190-0102
2	2950-0035	8	4	NUT-HEX-DBL-CHAM 15/32-32-THD	00000	Order by Desc.
3	2190-0586	2	2	WASHER-LK HLCL 4.0 MM 4.1-MM-ID	28480	2190-0586
4	0380-0643	3	2	STANDOFF-HEX .255-IN-LG 6-32THD	00000	Order by Desc.
5	1251-2942	7	2	LOCK-SUBMIN D CONN (INCLUDES LOCKWASHERS)	28480	1251-2942
6*	0515-0886	3	3	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	28480	0515-0886
7	9135-0265	5	1	FILTER-LINE OPERATING VOLTAGE:250 V MAX	06324	FN 365-4/05
8	2110-0655	8	0	FUSE 3.15A 250V NTD IEC (LISTED FOR REPLACEMENT PURPOSES. TWO ARE INCLUDED IN ITEM 7)	28480	2110-0655
9	5040-7221	2	4	FOOT, REAR	28480	5040-7221
10	0515-1232	5	4	SCREW-MACH M3.5 X 0.6 8MM-LG PAN-HD	28480	0515-1232

* **CAUTION**: This hardware is metric. Use of other thread types is likely to damage threaded holes.

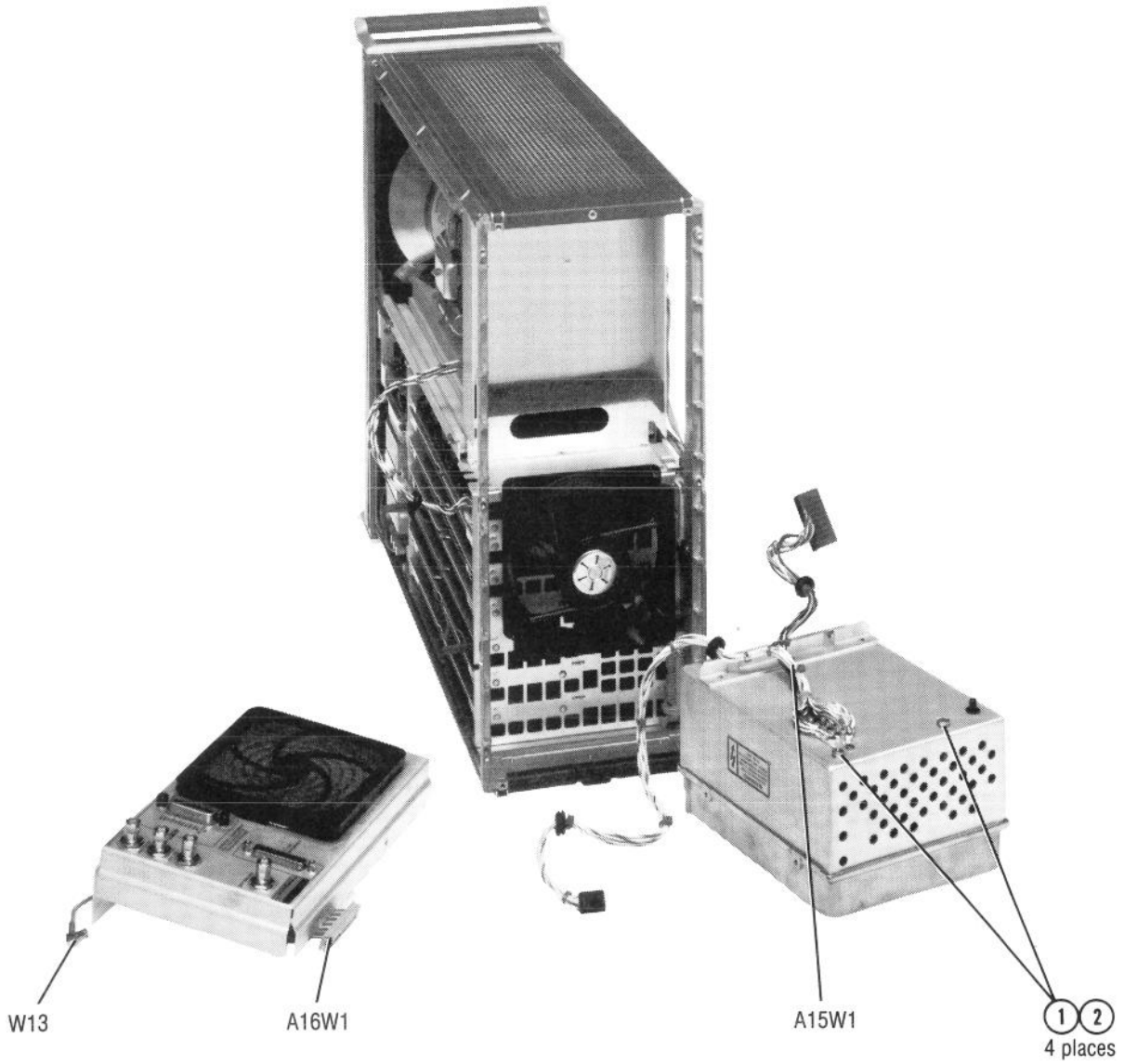
Figure 13. Rear Panel, Attaching Hardware



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1*	0515-0965	9	4	SCREW-SKT-HD-CAP M3 X 0.5 14MM-LG	28480	0515-0965
2	2190-0584	0	4	WASHER-LK HLCL 3.0 MM 3.1-MM-ID	28480	2190-0584
3*	0515-1054	9	4	SCREW-MACH M3 X 0.5 9MM-LG 90-DEG-FLH-HD	28480	0515-1054
4	3150-0484	6	1	FILTER, FILTER GUARD & RETAINER, 4.65	28480	3150-0484
5	08753-20040	2	1	FAN GASKET	28480	08753-20040
6	08753-00019	3	1	REAR PANEL	28480	08753-00019
7				REAR FRAME – SEE FIGURE 6		
A16	08753-60016	6	1	REAR PANEL BOARD ASSY (INCLUDES A16W1)	28480	08753-60016
A16W1				RIBBON CABLE ASSEMBLY – A16 TO A17 – SEE FIGURE 4		
B1	08753-60047	3	1	FAN (INCLUDES CONNECTING CABLE ASSY)	28480	08753-60047
W13				FLEXIBLE RF CABLE ASSEMBLY – A12 TO REAR PANEL SEE FIGURE 4		

*** CAUTION:** This hardware is metric. Use of other thread types is likely to damage threaded holes.

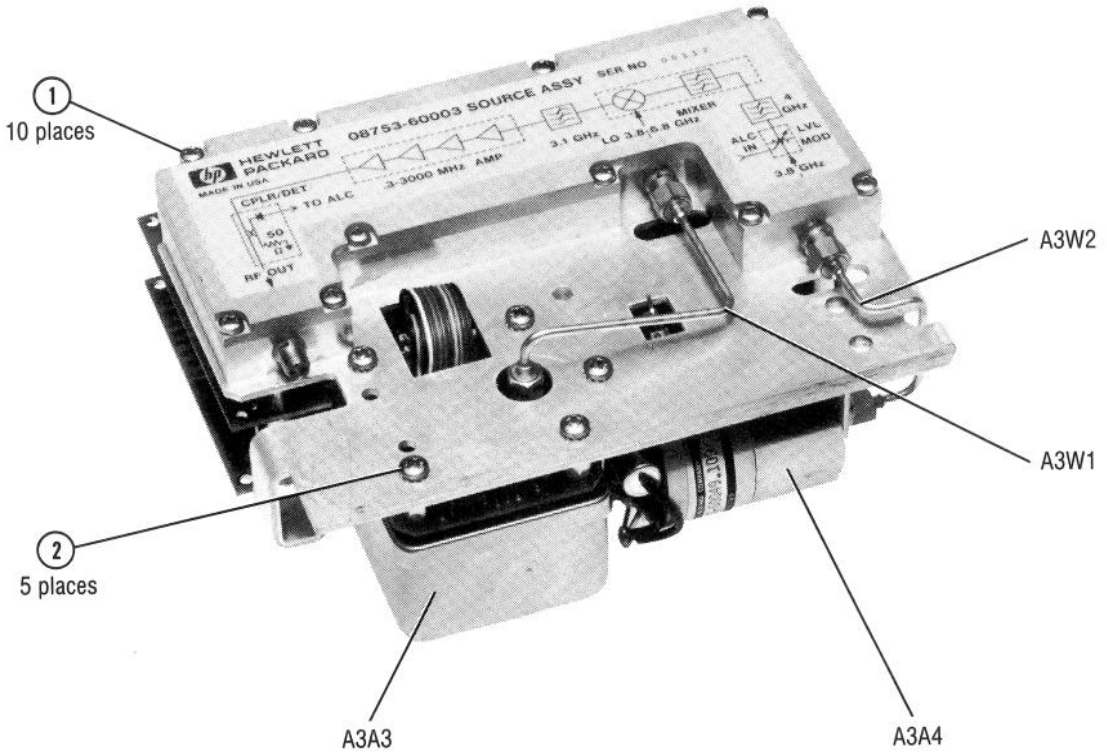
Figure 14. Rear Panel, Assemblies



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1*	0515-0443	8	4	SCREW-MACH M4 X 0.7 20MM-LG PAN-HD	28480	0515-0443
2	2190-0586	2	4	WASHER-LK HLCL 4.0 MM 4.1-MM-ID	28480	2190-0586
A15W1				CABLE ASSEMBLY – A15 TO A8 AND A17 – SEE FIGURE 4		
A16W1				RIBBON CABLE ASSEMBLY – A16 TO A17 – SEE FIGURE 4		
W13				FLEXIBLE RF CABLE ASSEMBLY – A12 TO REAR PANEL SEE FIGURE 4		

* **CAUTION**: This hardware is metric. Use of other thread types is likely to damage threaded holes.

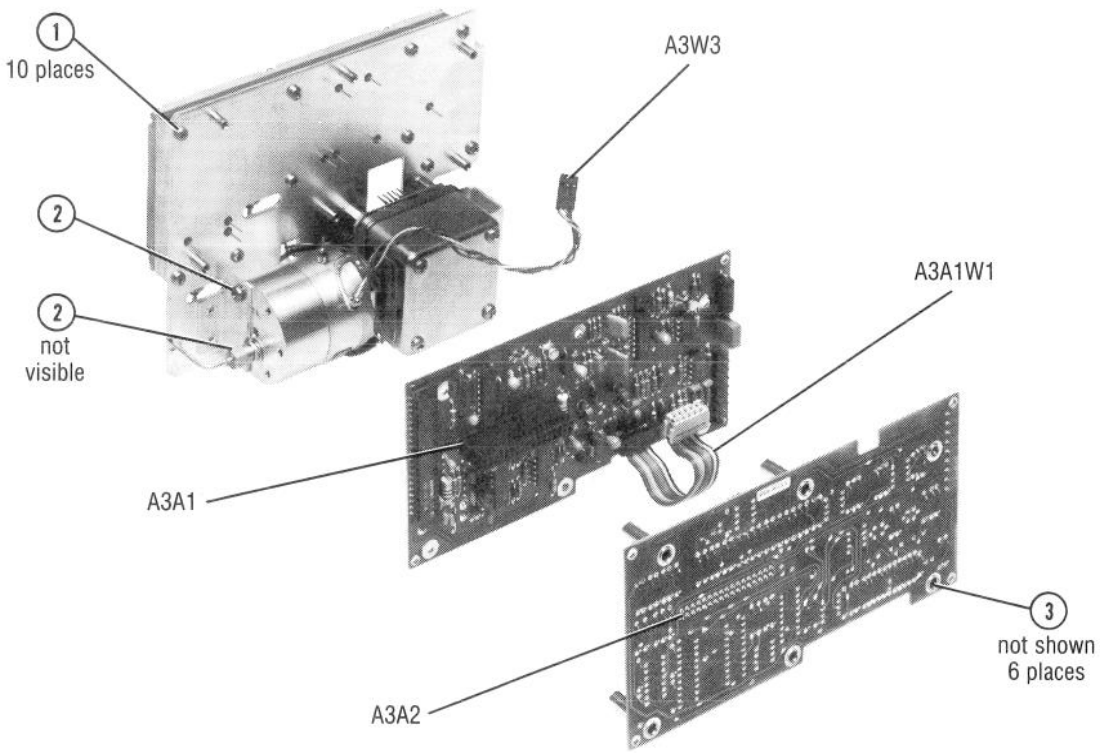
Figure 15. Rear Panel, Cables



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1*	0515-0897	6	10	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD	28480	0515-0897
2	2360-0113	2	5	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	Order by Desc.
A3A3				YIG OSCILLATOR – PART OF A3 – SEE FIGURE 2		
A3A4				CAVITY OSCILLATOR – PART OF A3 – SEE FIGURE 2		
A3W1				SEMI-RIGID CABLE ASSEMBLY – YIG OSC. OUTPUT SEE FIGURE 4		
A3W2				SEMI-RIGID CABLE ASSEMBLY – CAV. OSC. OUTPUT SEE FIGURE 4		

* **CAUTION:** This hardware is metric. Use of other thread types is likely to damage threaded holes.

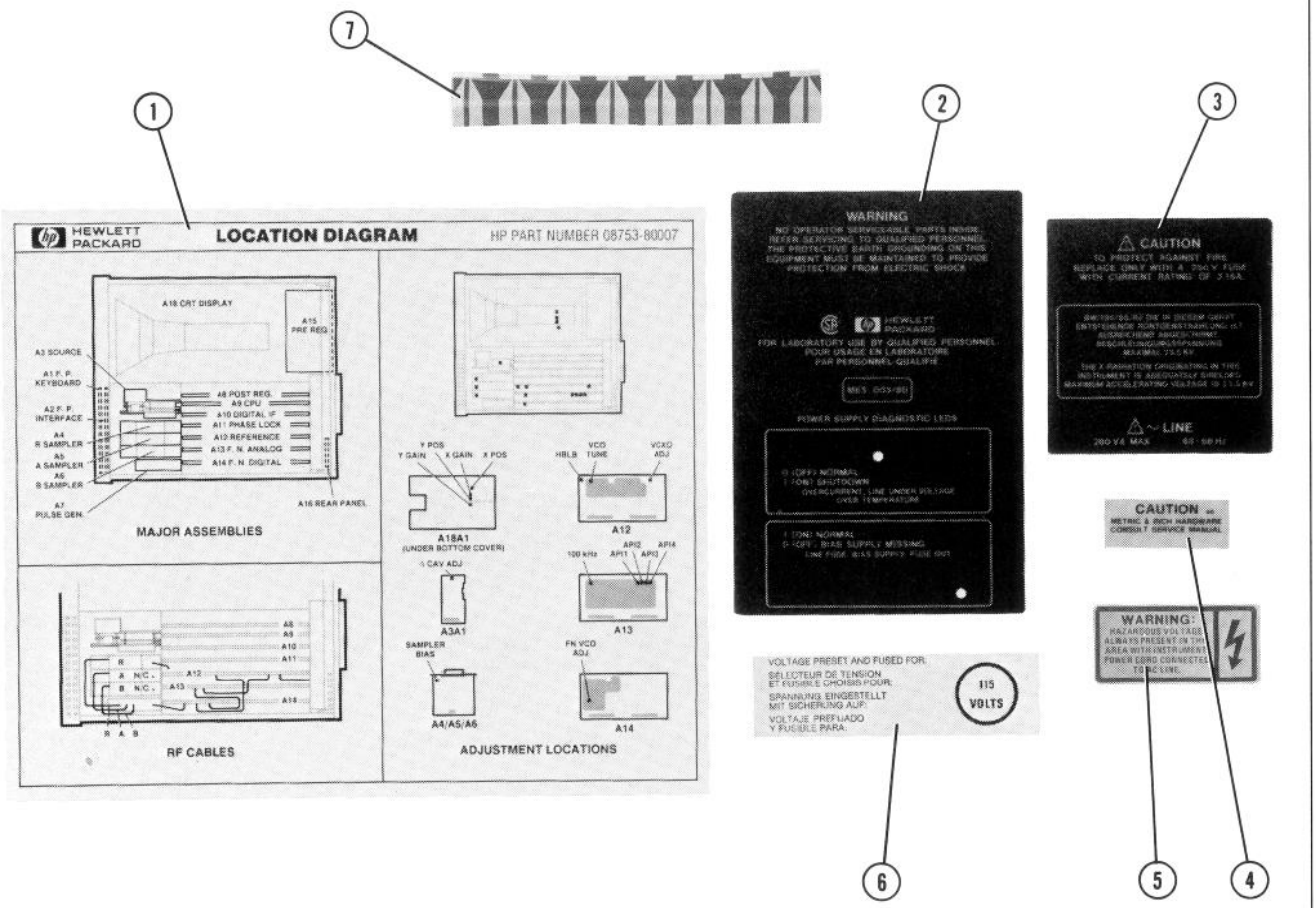
Figure 16. A3 Source Assembly



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1*	0515-0897	6	10	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD	28480	0515-0897
2	2360-0113	2	2	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	Order by Desc.
3*	0515-1323	5	6	SCREW-MACH M3 X 0.5 30MM-LG PAN-HD	28480	0515-1323
A3A1				SOURCE BIAS BOARD – PART OF A3 – SEE FIGURE 2		
A3A1W1				RIBBON CABLE ASSEMBLY – YIG OSC. TO A3A1 – SEE FIGURE 4		
A3A2				ALC BOARD – PART OF A3 – SEE FIGURE 2		
A3W3				CABLE ASSEMBLY – CAV. OSC. TO A3A1 – SEE FIGURE 4		

* **CAUTION**: This hardware is metric. Use of other thread types is likely to damage threaded holes.

Figure 17. A3 Source Assembly, Detail



Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
1	08753-80007	7	1	LABEL – LOCATION DIAGRAM	28480	08753-80007
2	08753-80002	2	1	LABEL – LED OPERATION WARNING	28480	08753-80002
3	08753-80001	1	1	LABEL – CAUTION FUSE RATING	28480	08753-80001
4	7121-2527	5	1	LABEL – METRIC HARDWARE CAUTION	28480	7121-2527
5	7120-4295	6	1	LABEL – HAZARDOUS VOLTAGE WARNING	28480	7120-4295
6	7120-6999	1	1	LABEL – LINE VOLTAGE SELECTOR SWITCH	28480	7120-6999
7	08753-80005	5	1	LABEL – PARALLAX SOFTKEY MENU	28480	08753-80005

Figure 18. Replaceable Labels

Table 2. Miscellaneous Replaceable Accessories

Ref. Desig.	HP Part Number	C.D.	Qty.	Description	Mfr. Code	Mfr. Part No.
				SERVICE TOOLS		
1	08753-60023	5	1	HP 8753A TOOL KIT	28480	08753-60023
2	08753-60050	8	1	HP 8753A BOARD KIT (REPAIRS INST. >95% OF THE TIME)	28480	08753-60050
3	08753-60051	9	1	HP 8753A BOARD KIT (REPAIRS INST. 70% OF THE TIME)	28480	08753-60051
				SOFTWARE		
4	08753-10010	5	1	PERFORMANCE TESTS AND ADJUSTMENTS SOFTWARE	28480	08753-10010
				DOCUMENTATION		
5	08753-90001	2	1	HP 8753A OPERATING AND PROGRAMMING MANUAL	28480	08753-90001
6	08753-90022	7	1	HP 8753A ON-SITE SYSTEM SERVICE MANUAL	28480	08753-90022
7	08753-90021	6	1	HP 8753A TEST SETS AND ACCESSORIES MANUAL	28480	08753-90021
8	85046-90001	8	1	HP 85046A/B S-PARAMETER TEST SETS MANUAL	28480	85046-90001
9	85044-90001	6	1	HP 85044A/B TRANSMISSION/REFLECTION TEST SETS MANUAL	28480	85044-90001
10	85031-90003	3	1	HP 85031B 7 MM CALIBRATION KIT MANUAL	28480	85031-90003
11	85032-90007	8	1	HP 85032B 50 OHM TYPE-N CALIBRATION KIT MANUAL	28480	85032-90007
12	85033-90007	9	1	HP 85033C 3.5 MM CALIBRATION KIT MANUAL	28480	85033-90007
13	85036-90003	8	1	HP 85036B 75 OHM TYPE-N CALIBRATION KIT MANUAL	28480	85036-90003
14	85029-90001	7	1	HP 85029A 7 MM VERIFICATION KIT MANUAL	28480	85029-90001
15	11851-90007	4	1	HP 11851B 50 OHM TYPE-N RF CABLE KIT MANUAL	28480	11851-90007
16	11857-90014	9	1	HP 11857D 7 MM TEST PORT EXTENSION CABLES MANUAL	28480	11857-90014
17	11857-90016	1	1	HP 11857B 75 OHM TYPE-N TEST PORT CABLES MANUAL	28480	11857-90016
18	11850-90019	7	1	HP 11850D 75 OHM 3-WAY POWER SPLITTER MANUAL	28480	11850-90019
19	11850-90021	9	1	HP 11850D 75 OHM 3-WAY POWER SPLITTER MANUAL	28480	11850-90021
20	11667-90003	6	1	HP 11667A POWER SPLITTER MANUAL	28480	11667-90003
21	11852-90009	7	1	HP 11852B 50 TO 75 OHM MINIMUM LOSS PAD MANUAL	28480	11852-90009
22	85033-90010	8	1	HP 85033A SMA CALIBRATION KIT MANUAL	28480	85033-90010
23	11600-90006	0	1	HP 11600B TRANSISTOR FIXTURE MANUAL	28480	11600-90006
24	11608-90029	5	1	HP 11608A TRANSISTOR FIXUTRE MANUAL	28480	11608-90029
25	11858-90001	5	1	HP 11858A TRANSISTOR FIXTURE ADAPTER MANUAL	28480	11858-90001
26	08510-90064	4	1	HP MICROWAVE CONNECTOR CARE MANUAL	28480	08510-90064
27	5958-7442	4	1	HP MICROWAVE CONNECTOR CARE APPLICATION NOTE	28480	5958-7442

Manual Backdating

INTRODUCTION

This manual section traditionally contains backdating, the information required to adapt the manual so that it applies to earlier versions or configurations of an instrument. Because there are no earlier versions of the HP 8753A (instruments having a serial prefix lower than those listed on the title page), there is no backdating information; the information in this manual applies directly to HP 8753A network analyzers that have a serial number prefix listed on the title page of this manual.

Instruments manufactured after the printing of this manual may be different than those documented in this manual. Later instrument versions will be documented in a manual changes supplement that will accompany the manual shipped with that instrument. For further information on manual changes supplements, refer to "Instruments Covered By Manual", in the General Information and Specifications section of the HP 8753A Operating and Programming Manual.

SERVICE

INTRODUCTION

The organization of this service section is based on the following troubleshooting method.

1. Overall instrument theory is discussed in Theory of Operation.

   Theory of operation is explained by discussing the operation of each "functional" group in the instrument. An overall block diagram (foldout) of the instrument is at the end of this section.

2. The instrument, itself is identified as having a fault in System Level Troubleshooting.

   The network analyzer is isolated and checked for proper operation by itself.

3. Use System Level Troubleshooting to isolate the faulty functional group.

   The HP 8753A network analyzer is divided into four "functional" groups (so-called because each performs a basic instrument function). They are: Power Supplies, Digital Control, Source, and Receiver.

   The overall block diagram in Theory of Operation and the information in Troubleshooting Reference should be used with the procedure in System Level Troubleshooting to identify the faulty functional group.

4. Use Functional Group Troubleshooting to probe deeper into the suspected functional group and to identify the faulty assembly.

   Each functional group consists of two or more assemblies and are detailed in Functional Group Troubleshooting. This section helps locate the faulty assembly within the functional group.

   A rebuilt-exchange program is offered on most assemblies. This program allows replacement of an assembly at a lower cost than a new assembly. Refer to the Replaceable Parts section for more details.

5. Verification, or any adjustments or performance tests required after replacing the defective assembly is performed.

   A table of what to adjust or verify after replacing any assembly is outlined in Related Service Procedures under Troubleshooting Reference in this section.

   The Troubleshooting Reference consists of information about internal diagnostics used to test, adjust, and troubleshoot the HP 8753A. The procedures in this subsectionb are referenced frequently throughout the rest of the service section.

THEORY OF OPERATION

INTRODUCTION

This section describes how the HP 8753A system works. Refer to Figure 1 and the HP 8753A Overall Block Diagram with Analog Bus Nodes in this section for the following text.

MAIN FEATURES

The HP 8753A system measures phase and magnitude transmission and reflection characteristics of RF and microwave components and sub-systems. The main component of the HP 8753A system is the HP 8753A network analyzer. The HP 8753A contains a built-in synthesized source, three identical receivers, and a display.

The HP 8753A system consists of the HP 8753A network analyzer and any of several available test sets. Refer to the latest Technical Data Sheet and Ordering Guide for information about compatible test sets and accessories.

FUNCTIONAL GROUPS

The HP 8753A system can be divided into four functional groups to help understand how the system works and facilitate troubleshooting. The four groups are power supply digital control, source, and receiver. Each group performs a specific function in the system. Some major assemblies belong to two groups, so some functional groups overlap.

Functional Group	Associated Assembly
Power Supply	A8 post-regulator A15 preregulator
Digital Control	A1/A2 front panel A9 CPU A10 digital IF A16 rear panel A18 display
Source	A3 source A4 sampler/mixer A7 pulse generator A11 phase lock A12 reference A13 fractional-N (analog) A14 fractional-N (digital)
Receiver	A4/A5/A6 sampler/mixer A10 digial IF A7 pulse generator A12 reference

HP 8753A SYSTEM BLOCK DIAGRAM

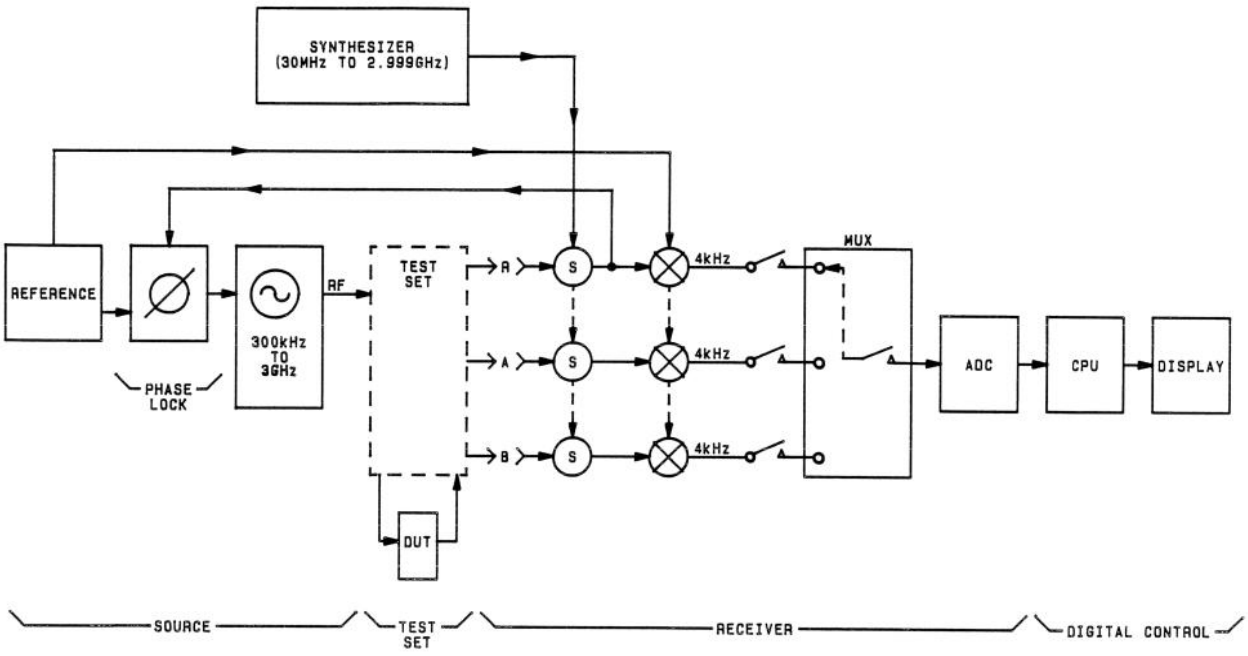


Figure 1. Simplified Block Diagram

POWER SUPPLIES FUNCTIONAL GROUP

Refer to Figures 2 and 3 for the following text. The power supplies functional group consists of the A15 preregulator assembly and the A8 post regulator board assembly.

The A15 preregulator assembly contains a power line switch, switching power supply, the over-voltage protection circuit for the +5 volt digital supply (+5VD), and some control circuitry. Refer to Figure 1, which shows the A15 Preregulator in block form as well as the following seven DC output voltages:

A15 Preregulator
Output Voltages

+25V
+18V
-18V
+8V
+5VD
+5VCPU
-8V

The power supply provides regulated DC voltages to power all assemblies in the instrument. The A15 preregulator assembly is an efficient switching power supply. It directly regulates the +5V instrument supply and indirectly regulates the remaining supply voltages. The +5V digital supply is routed through the A17 motherboard to the individual assemblies, and then fed back to the A15 preregulator for regulation.

The six other supplies from the A15 preregulator are routed to the A8 post-regulator for regulation and breakdown into various other supply voltages through individual regulators.

The A8 Post Regulator consists of the individual regulators for the instrument power supplies, over-temperature shutdown circuit, variable fan circuitry, and the air flow detector. Its inputs are the six different voltages from the A15 Preregulator. The outputs are routed to individual assemblies throughout the instrument.

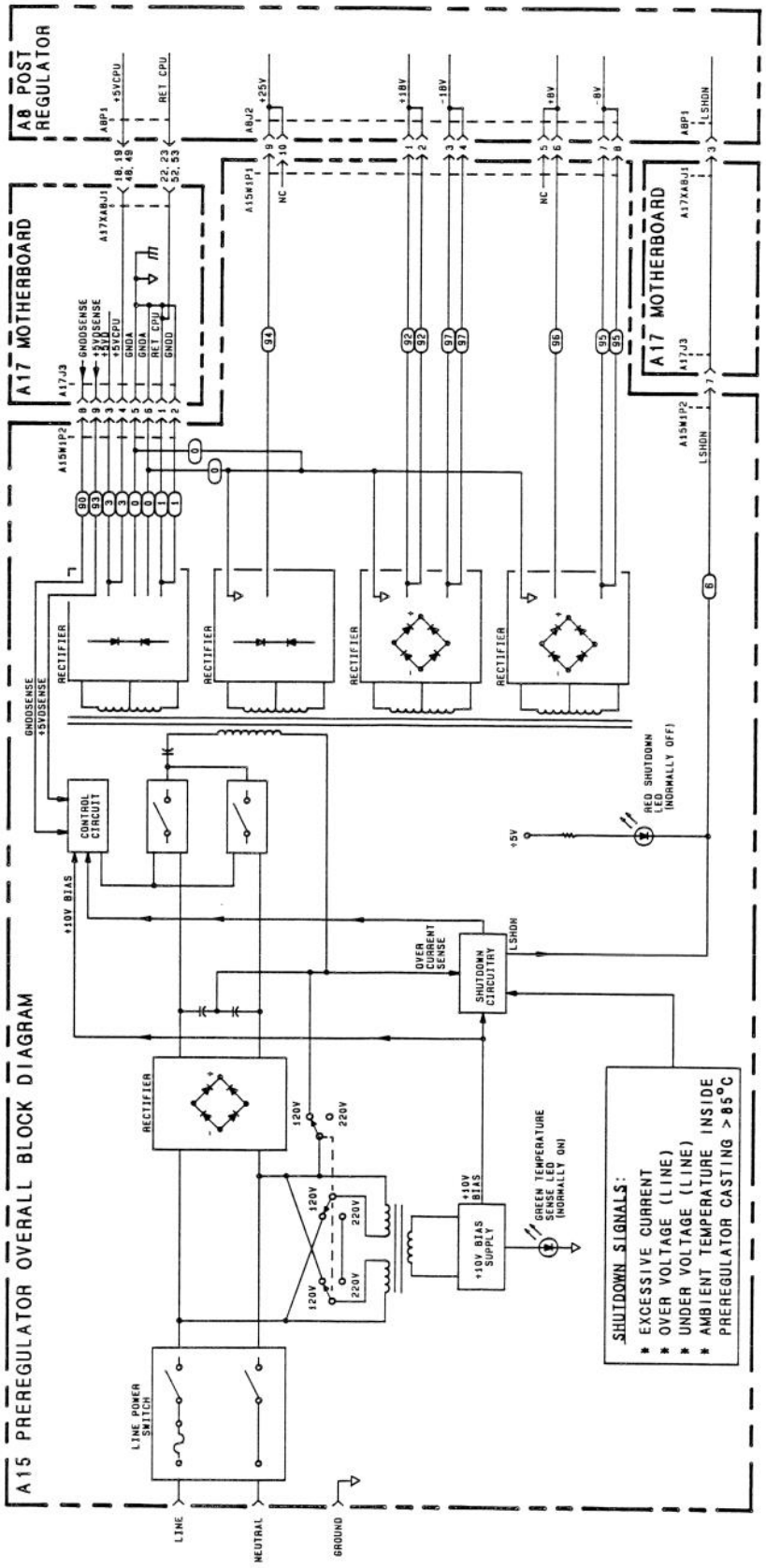


Figure 2. A15 Pre-regulator Block Diagram

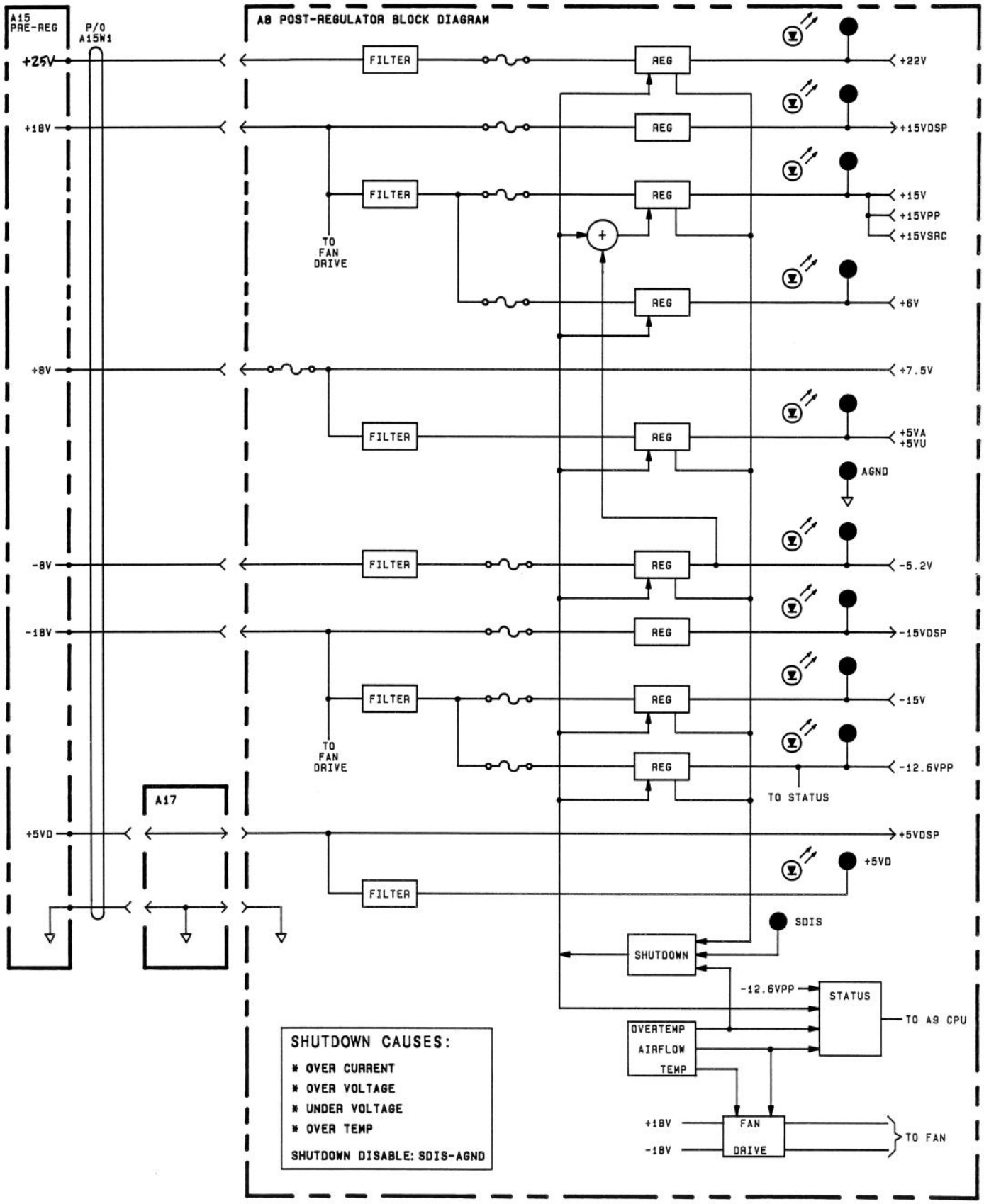


Figure 3. A8 Post-regulator Block Diagram

DIGITAL CONTROL FUNCTIONAL GROUP

Refer to Figure 4 for the following text. The master controller for the HP 8753A and the digital control functional group is the Motorola 68000 16-bit microprocessor. It controls the entire instrument via the instrument bus, including the A2 front panel assembly, the A16 rear panel assembly HP-IB interface, and the A18 display assembly.

The A2 front panel assembly contains a dedicated processor to detect and decode front panel key presses, rotary pulse generator (RPG) rotation, and communicates these user requests to the 68000. The front panel processor controls LEDs on the A1 front panel assembly to provide status information to the user.

The A16 rear panel assembly HP-IB interface contains a dedicated processor to monitor and control the handshake and data lines of the external bus, and communicate remote controller requests to the 68000.

The 68000 operates out of ROM on the A9 CPU board assembly and manages shared access to 128K bytes of dynamic RAM. Other processors which share this memory are the math processor and the A18 display processor. The math processor computes discrete fourier transforms which extract the complex data from the sampled 4 kHz IF. The math processor performs all the computation on the raw measuremnt data, and writes that data into dynamic RAM.

The 68000 then formats that data with respect to error correction, scaling, trace math, and time domain functions. Refer to Chapter 1 in the Operating and Programming Reference (OPR) for data flow and processing details. The A18 display then reads the formatted data from RAM and displays the data on the CRT.

The 68000 has access to two other types of memory: EEPROM and CMOS RAM. EEPROM contains the factory default correction constants for the specific instrument. These constants correct for several hardware imperfections such as sampler rolloff, source flatness, CRT intensity and focus, and so on. These correction constants can be updated by executing the routines found in the Adjustments and Correction Constants section of this manual.

CMOS RAM is backed up by a large "super" capacitor, providing at least 72 hours of data storage. This memory is used to store instrument states.

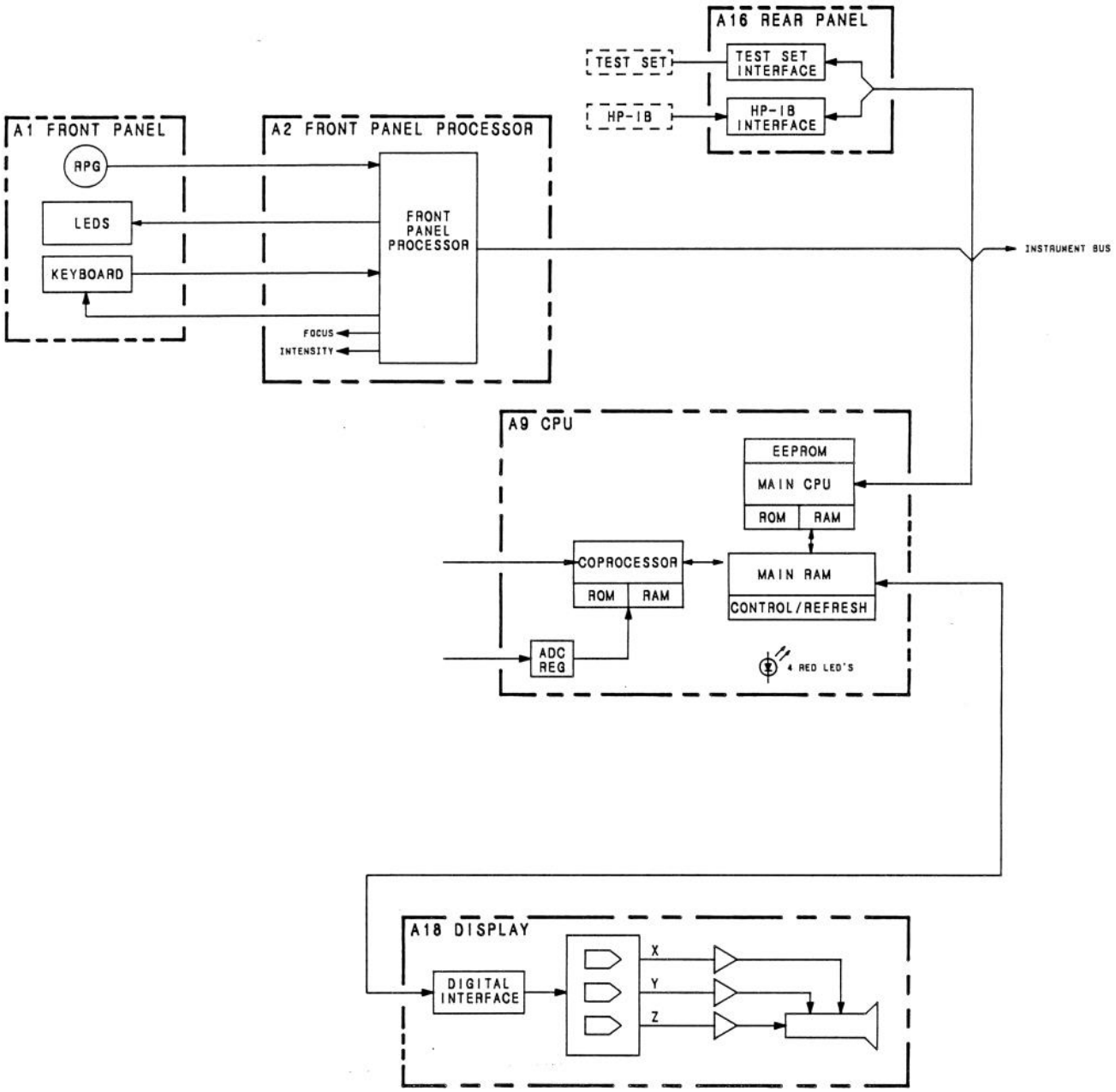


Figure 4. Digital Control Functional Group Block Diagram

SOURCE FUNCTIONAL GROUP

Refer to Figure 5 for the following text. The source functional group consists of the A12 reference, A11 phase lock, A3 source, A4 R input sampler/mixer, the A13/A14 fractional-N synthesizer, and the A7 pulse generator. The purpose of this group is to produce the RF output at the proper frequency and power level. Phase locking, leveling, and synthesizing are important functions accomplished by this group.

The phase locking scheme involves the A11 phase lock, A3 source, and the A4 R input sampler/mixer assemblies. Phase locking is achieved by comparing the difference frequency of the synthesizer to the A3 source. To be phase locked, the A3 source and the A13 and A14 fractional-N assemblies must maintain a frequency difference of 1 MHz. The synthesizer will be 1 MHz lower in frequency. The power leveling process is also done by the A3 source assembly. The A3 source contains the various microcircuits and automatic leveling control (ALC) circuitry.

The synthesizer includes a 30 MHz to 60 MHz oscillator whose signal is applied to a step recovery diode (SRD). The SRD generates the harmonics that are necessary to reach the upper frequency range of the A3 source. These harmonics are applied to the sampler as the first LO. The first IF signals are generated in the sampler and applied to the A11 phaselock board assembly. The A11 filters all undesired signals from the first IF.

The instrument is swept by sweeping the synthesizer (30 MHz to 60 MHz oscillator) and causing the A3 source to track the synthesizer. This is different from the method of sweeping the source (YIG oscillator) by a tune voltage.

Refer to Table 1 for the following text. The source covers its full range in two bands (lowband and highband). The operation of each of these bands will be covered in detail later in this Theory of Operation.

Within each band, the instrument is swept in subsweeps while the receiver processes the three inputs (R, A, and B). The band transitions require that the instrument break lock and then relock. This relock process is pretune, acquire, and to lock the instrument.

Table 1. HP 8753A Key Sweep Frequencies

RF Out (MHz)	Band	Frac-N (MHz)	Harmonic	1st IF (MHz)	2nd LO (MHz)	2nd IF (kHz)
.300-3.3	0,low	40.3-43.3	N/A	.300-3.3	.304-3.304	4
3.3-16	1,low	43.3-56	N/A	3.3-16	3.304-16.004	4
16-31	2,high	30-60	1/2	1	0.996	4
31-61	3,high	30-60	1	1	0.996	4
61-121	4,high	30-60	2	1	0.996	4
121-178	5,high	40-59	3	1	0.996	4
178-296	6,high	35.4-59.2	5	1	0.996	4
296-536	7,high	32.8-59.4	9	1	0.996	4
536-893	8,high	35.7-59.5	11	1	0.996	4
893-1607	9,high	33.0-59.5	27	1	0.996	4
1607-3000	10,high	31.5-58.8	51	1	0.996	4

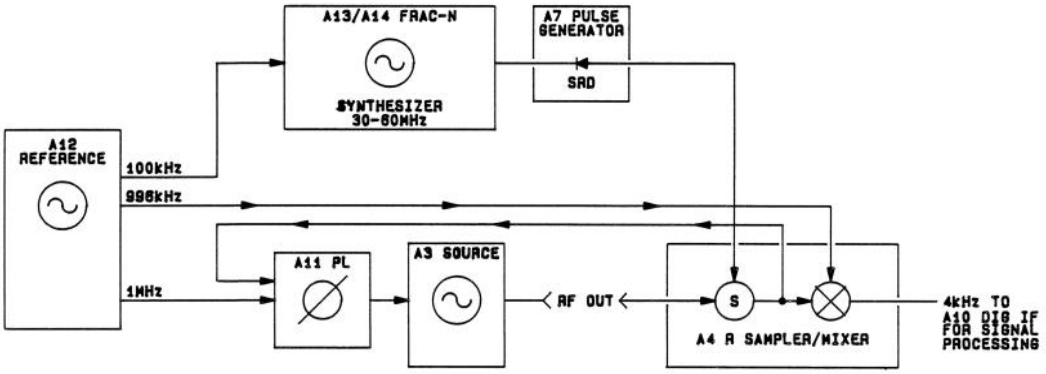


Figure 5. Source Functional Group Block Diagram

The source assemblies involved in the pretune sequence are the A11 phaselock (which generates the A3 source tuning voltage), and the A13 and A14 fractional-N assemblies (which generate a frequency 1 MHz below the desired RF frequency).

Tracking involves comparing the difference frequency between the synthesizer output and the R channel output to a 1 MHz reference. Until the difference is 1 MHz, the A11 phaselock board assembly will generate an error voltage to correct the A3 source assembly. The lock mode is when the synthesizer and the A3 source assembly frequencies are 1 MHz apart.

LOWBAND AND HIGHBAND THEORY

The HP 8753A is divided into two major sweep categories, highband and lowband. Within these bands, there are subsweeps that sweep portions of each band.

Refer to Figures 6 and 7 for the following text. The range for lowband is 300 kHz to 16 MHz while highband is 16 MHz to 3 GHz.

Lowband sweeps (300 kHz to 16 MHz) are significantly different from highband sweeps. The most significant difference is the reference frequency of the A11 phaselock board assembly. This reference frequency is derived from mixing a 40 MHz LO with the synthesizer RF input, so that the phaselock reference will vary as the synthesizer varies. The synthesizer frequency will be 40 MHz greater than the start frequency.

In lowband, the samplers are on continously (not sampled), so that R, A, and B input signals pass directly through them. The first IF is no longer fixed but is identical to the RF output frequency and sweeps with it.

The A11 phaselock board assembly will generate a pretune voltage to coarsely tune the A3 source. This coarse frequency is fed back to the A11 phaselock board assembly and compared to the reference frequency. An error voltage will be generated and applied to the A3 source until the reference frequency and the source frequency are the same.

When lock is achieved, the synthesizer starts sweeping. This changes the reference frequency and causes the A3 source to follow the sweep of the synthesizer. Because the second RF is sweeping, the second LO must also sweep to maintain the constant 4 kHz IF. This is required for signal processing. This sweeping LO is provided by the A12 reference board assembly.

The following steps indicate the sequence of events that take place when a lowband sweep is initiated.

Lowband Sweep Sequence

1. A power level and a frequency range (within lowband) is selected by the user.

2. The synthesizer is set to a frequency that is 40 MHz greater than the start frequency.

3. The A3 source is pretuned to a frequency that is close to the start frequency.

4. The A3 source RF output is fed back to the A11 phaselock through reference sampler/mixer (A4).

5. An error voltage is generated until the IF and source frequency are the same. When lock is achieved, data is processed and sweeping begins.

HP 8753A SYSTEM BLOCK DIAGRAM

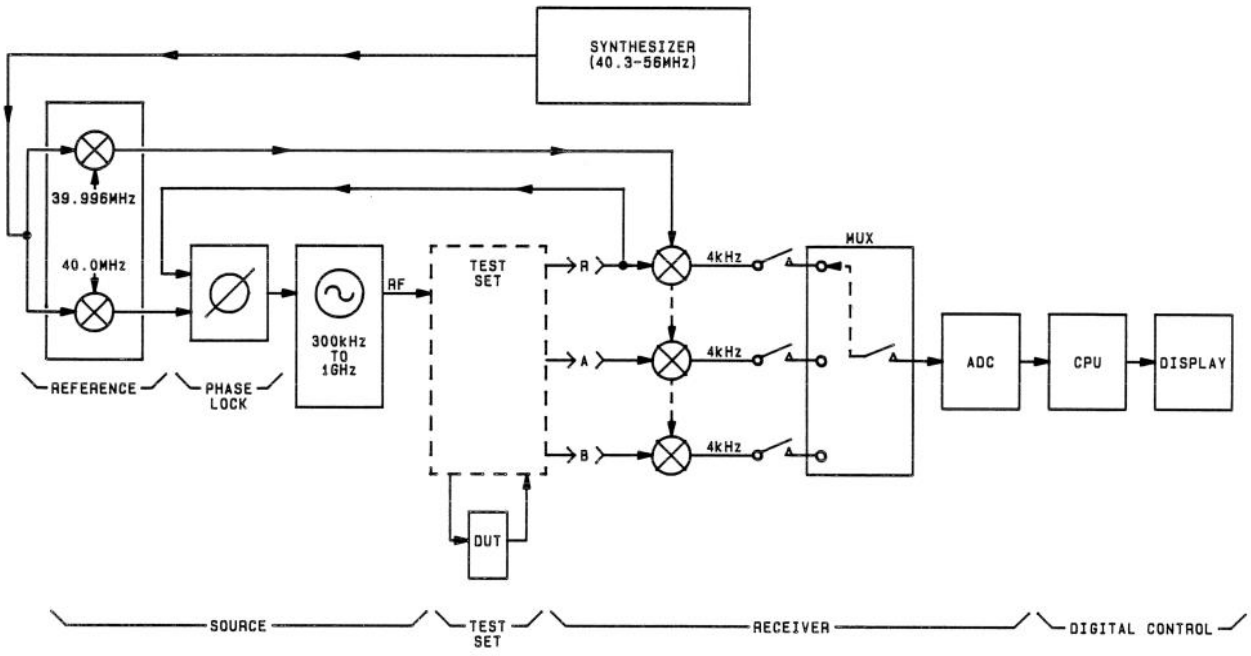


Figure 6. Lowband Operation

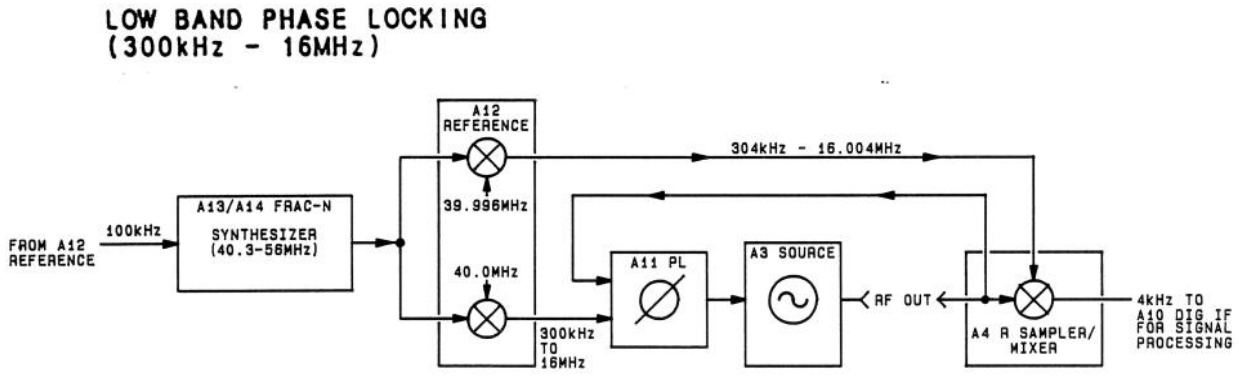


Figure 7. Lowband Phase Locking

Highband subsweeps are generated by phase-locking the A3 source to a harmonic multiple of the fractional-N VCO. A special case of highband is the 15 to 30 Mhz subsweep, when a divide-by-2 circuit (1/2 harmonic) is used. The following steps indicate the sequence of events that take place when a highband sweep is initiated.

Highband Sweep Sequence

Refer to Figures 8 and 9 for the following text.

1. A power level and a frequency range (within highband) is set by the user.

2. The synthesizer generates a frequency 1 MHz lower than the start frequency. This is accomplished by using the Fractional-N VCO and the harmonic generator to produce these upper frequencies.

3. The A3 source is pretuned 2 to 6 MHz higher than the start frequency.

4. The sampler IF output is fed back to the phaselock board and compared to a 1 MHz reference frequency.

5. An error voltage is produced which "fine tunes" the A3 source until the synthesizer and source are 1 MHz apart.

6. When lock is achieved, a sweep is taken.

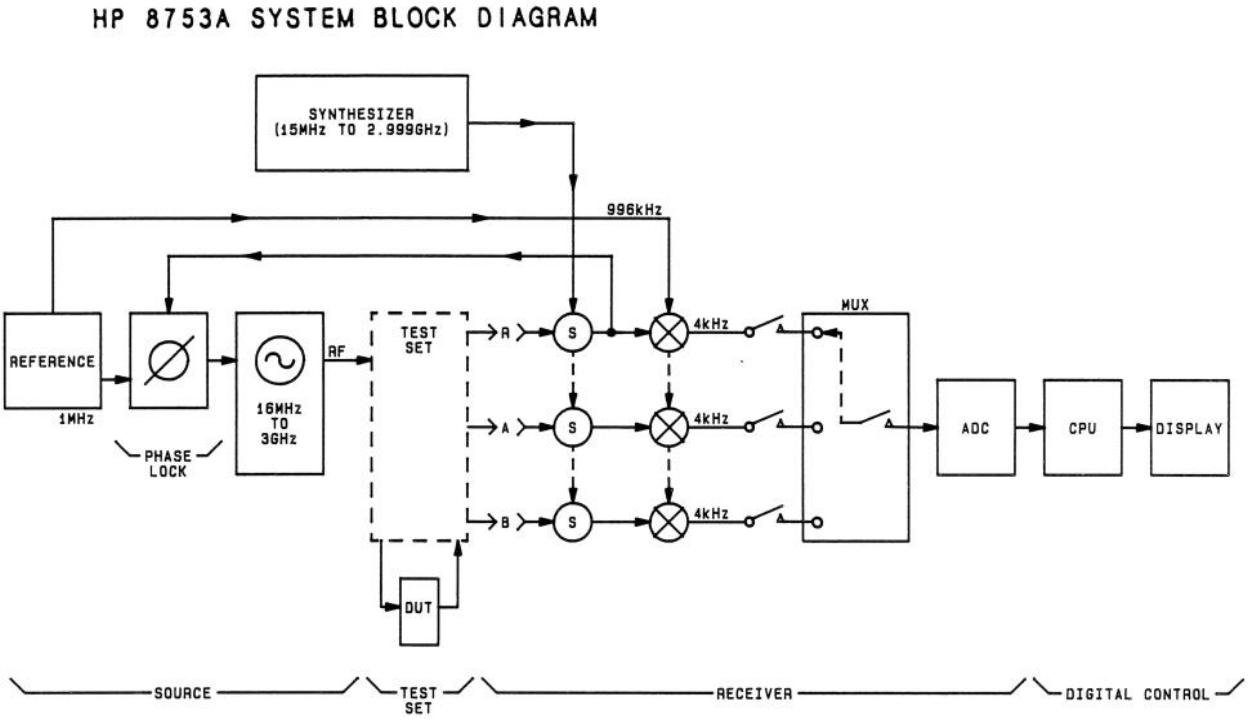


Figure 8. Highband Operation

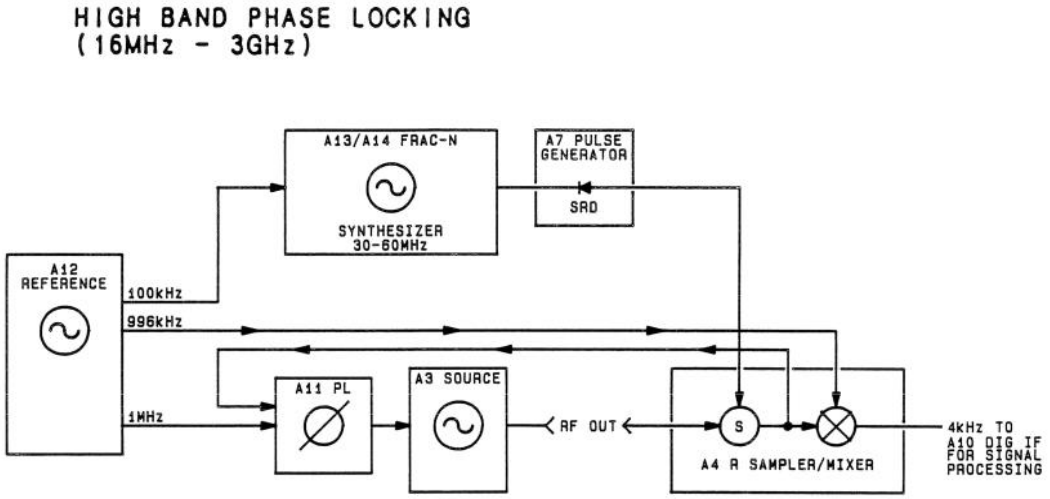


Figure 9. Highband Phase Locking

RECEIVER FUNCTIONAL GROUP

Refer to Figure 10 for the following text. The receiver functional group converts the RF signals at the R, A, and B inputs to a 4 kHz IF. This 4 kHz IF is then converted from an analog signal to a digital signal to be detected, processed, and displayed. Both amplitude and phase information are retained throughout the process.

The A4, A5, and A6 sampler/mixers are three **identical** assemblies that down-convert the RF input signals to a fixed 4 kHz second IF. Each assembly consists of a sampler and a mixer. Each sampler can be viewed as a harmonic mixer. The output frequency (IF) is the difference between the input frequency (RF) and the harmonic of the local oscillator (LO). The process can be expressed mathematically as:

First IF = RF ± n(LO)

where n is the harmonic value.

Filters remove all but the desired response.

The mixer stage then converts the first IF to a fixed second IF at 4 kHz. The second LO comes from the A12 reference board assembly. In highband, the second LO is fixed at 996 kHz, while in lowband it sweeps. This was discussed in Source Functional Group theory.

The A10 Digital IF board assembly converts the three 4kHz (second IF) signals to digital form for processing. Sample/hold circuits periodically sample these signals at a 16 kHz rate. A multiplexer sequentially directs each of the three sampled signals to the analog to digital converter (ADC), where the signals are digitized.

The A9 CPU board assembly includes a fast, dedicated microprocessor to transform the sampled phase and magnitude values from the ADC. The main 68000 processor handles the rest of formatting and controls the data to be displayed.

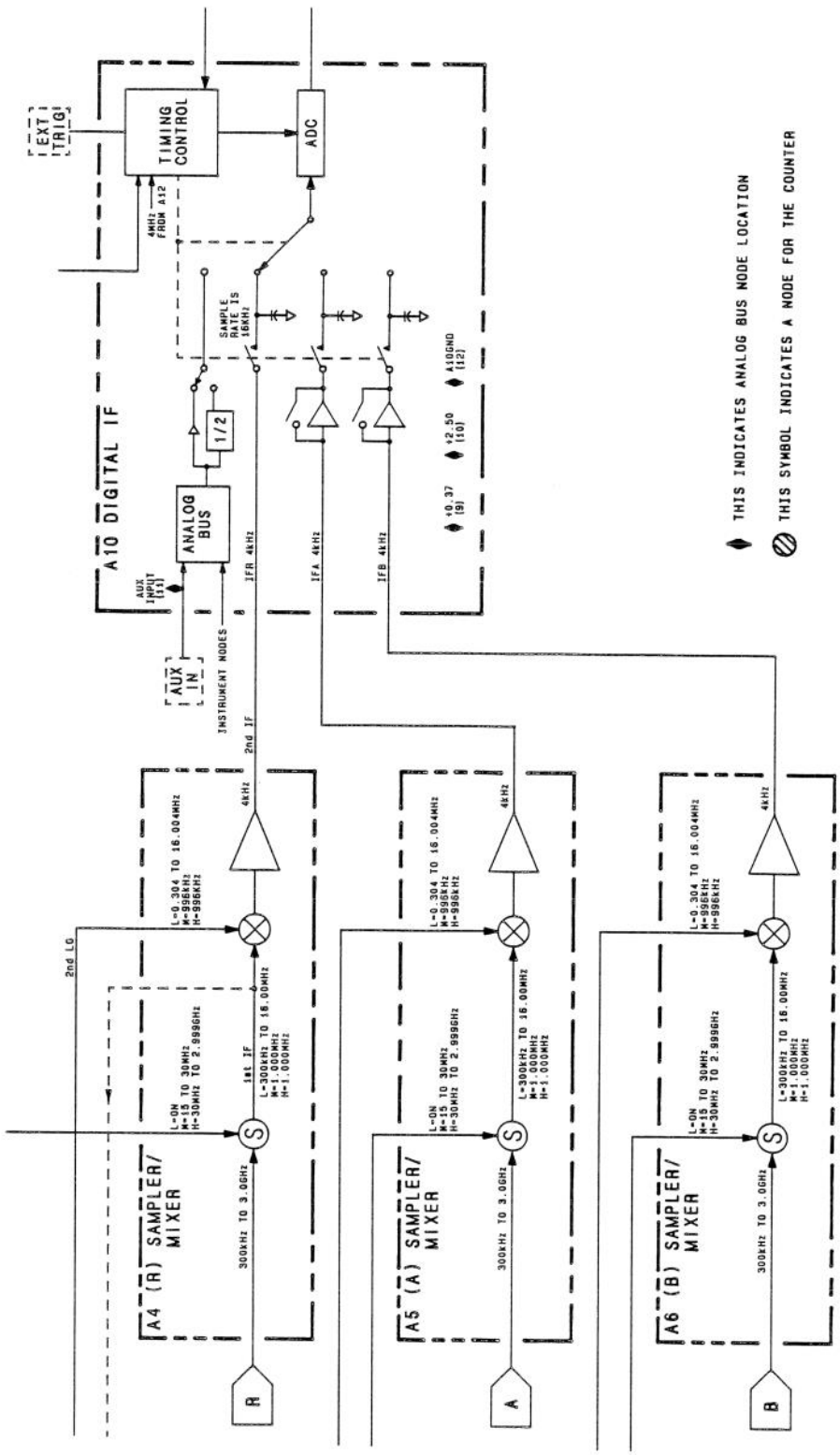
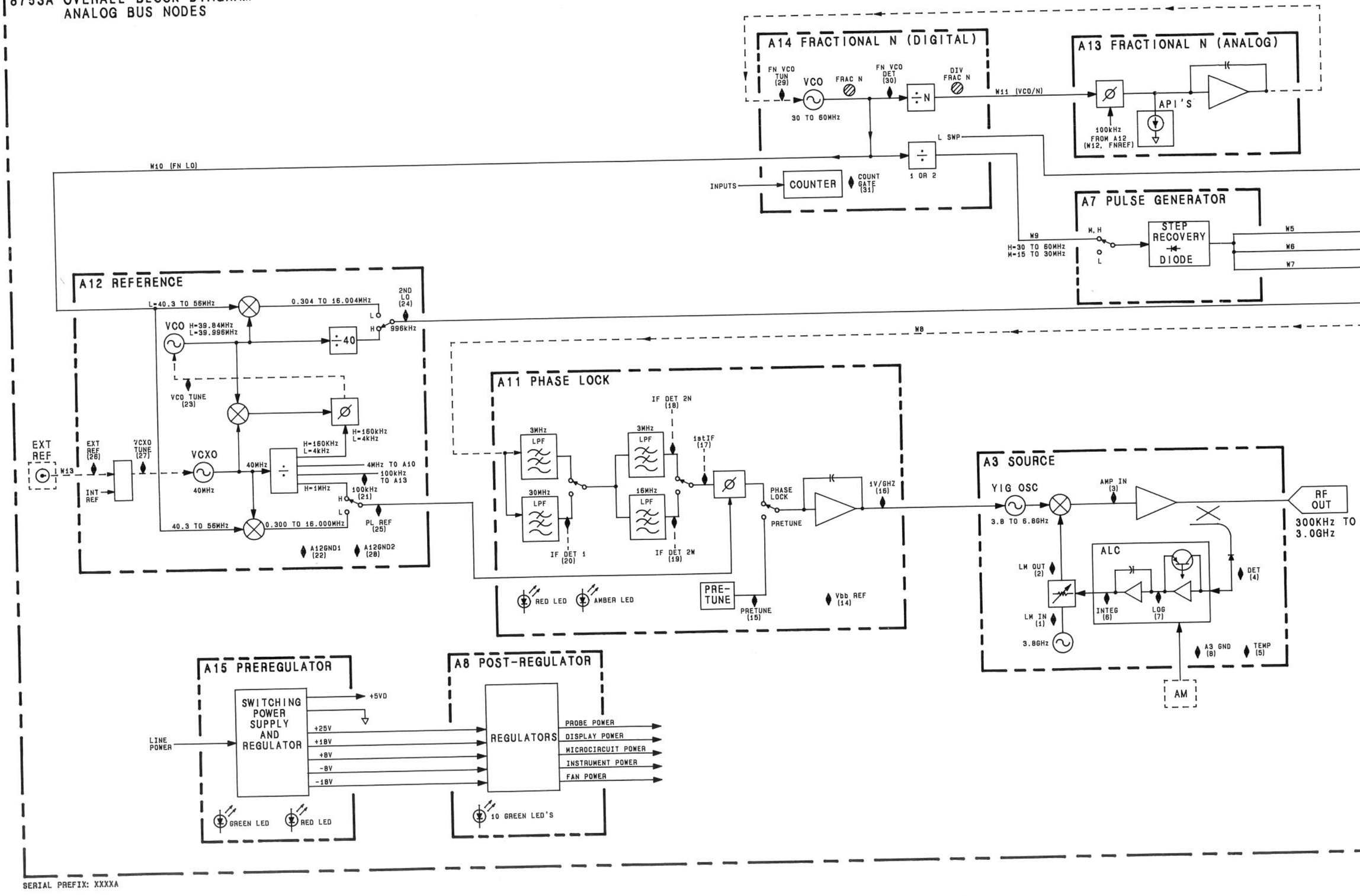


Figure 10. Receiver Function Group Block Diagram

8753A OVERALL BLOCK DIAGRAM
ANALOG BUS NODES



SERIAL PREFIX: XXXXA

A16 REAR PANEL

TEST SET

TEST SET INTERFACE

HP-IB

HP-IB INTERFACE

A1 FRONT PANEL

RPG

LEDS

KEYBOARD

A2 FRONT PANEL PROCESSOR

FRONT PANEL PROCESSOR

FOCUS

INTENSITY

INSTRUMENT BUS

EXT TRIG

A9 CPU

EEPROM

MAIN CPU

ROM RAM

COPROCESSOR

ROM RAM

MAIN RAM

CONTROL/REFRESH

4 RED LED'S

A10 DIGITAL IF

AUX INPUT (11)

AUX IN

ANALOG BUS

INSTRUMENT NODES

1/2

4MHz FROM A12

TIMING CONTROL

SAMPLE RATE IS 16KHz

IFA 4kHz

IFB 4kHz

ADC

ADC REG

+0.37 (9)

+2.50 (10)

A10GND (12)

1st LO

2nd LO

A4 (R) SAMPLER/ MIXER

L=ON
M=15 TO 30MHz
H=30MHz TO 2.999GHz

300kHz TO 3.0GHz

1st IF
L=300kHz TO 16.00MHz
M=1.000MHz
H=1.000MHz

L=0.304 TO 16.004MHz
M=996kHz
H=996kHz

4kHz

2nd IF

IFA 4kHz

A5 (A) SAMPLER/ MIXER

L=ON
M=15 TO 30MHz
H=30MHz TO 2.999GHz

300kHz TO 3.0GHz

L=300kHz TO 16.00MHz
M=1.000MHz
H=1.000MHz

L=0.304 TO 16.004MHz
M=996kHz
H=996kHz

4kHz

A6 (B) SAMPLER/ MIXER

L=ON
M=15 TO 30MHz
H=30MHz TO 2.999GHz

300kHz TO 3.0GHz

L=300kHz TO 16.00MHz
M=1.000MHz
H=1.000MHz

L=0.304 TO 16.004MHz
M=996kHz
H=996kHz

4kHz

A18 DISPLAY

DIGITAL INTERFACE

X

Y

Z

♦ THIS INDICATES ANALOG BUS NODE LOCATION

⊘ THIS SYMBOL INDICATES A NODE FOR THE COUNTER

SYSTEM LEVEL TROUBLESHOOTING

INTRODUCTION

The following system level procedure is designed to identify the functional group that contains the faulty assembly in an HP 8753A network analyzer that is not working. If any procedure fails, refer to the troubleshooting procedure for that group in Functional Group Troubleshooting. Follow that procedure to identify the bad assembly.

PROCEDURE

Power Supply Functional Group

Verify correct power to the instrument and that all DC supplies are operational:

1. Check the two power supply diagnostic LEDs on the rear panel of the HP 8753A by looking through the holes on the left of the line voltage selector switch. Normal operation is when the bottom (green) LED is on and the top (red) LED is off.

2. Check the 10 green power supply LEDs on the A8 post-regulator board assembly. Normal operation is when all LEDs are lit.

Digital Control Functional Group

Verify operation of all digital control functional group assemblies by using the following diagnostic tools:

Preset
Front panel LEDs
Internal tests
Self diagnose

3. Press **[PRESET]** to initiate a series of internal checks and to preset the instrument state. Normal operation is for all front panel amber LEDs to light, and then all but the CH 1 LED to go out soon afterwards.

4. Press **[CH 1]** and **[CH 2]** alternately and observe that only the active channel amber LED is lit. This test verifies that the A1/A2 front panel processor and the A9 CPU processor are communicating with each other correctly.

5. This step verifies A18 display operation and more of the A1/A2 front panel. Press **[MKR]**. Verify that the marker appears and can be controlled with the rotary pulse generator (RPG), step keys and entry keypad. Select random start and stop frequencies using the **[START]**, **[STOP]**, and entry keys and make sure the correct information is updated on the display.

   When the preceding steps have passed, confidence levels for the following assemblies may be assumed:

A1/A2 front panel	80%
A9 CPU	50%
A18 display	80%

6. This step causes internal diagnostic tests to be performed by the instrument. Press **[SYSTEM] [SERVICE MENU] [TESTS] [INTERNAL TESTS] [EXECUTE TEST]**.

   If any self-tests fail, press **[RETURN] [SELF DIAGNOSE]**. This feature displays all assemblies having a probability of failure based on the first internal test that failed. Use self diagnose as a guide. Verify any suspected assemblies. Further explanation of this feature may be found under the Troubleshooting Reference tab in this Service manual.

   When the preceding step has passed, confidence levels for the following assemblies may be assumed:

A1/A2 front panel	80%
A8 post-regulator	90%
A9 CPU	90%
A10 digital IF	50%
A15 preregulator	90%
A16 rear panel	20%

Source and Receiver Functional Groups

Perform the following procedure to determine if the faulty assembly is a part of the source or receiver functional group.

Useful analog bus nodes:

15
16
17

Refer to the Troubleshooting Reference tab in this Service manual for detailed information about use of the analog bus.

NOTE: Phaselock error messages are not particularly useful when troubleshooting at the system level. The problem may be in either the source functional group, or the receiver functional group. Error messages are discussed in more detail in the individual functional group troubleshooting sections.

8. To check source operation, connect a splitter to the RF OUT of the HP 8753A. Connect the splitter outputs to input R port and to the input of an oscilloscope.

First, determine if the problem is sweep time related: press **[MENU] [SWEEP TIME]**, then vary the sweep time (slower and faster) and check if the problem changes or goes away. If the problem goes away with a different sweep time, continue troubleshooting with the sweep time set to where the problem occurs.

Set the HP 8753A for 40 MHz CW (highband frequency). On the scope, verify that the frequency is correct. Vary the RF output power level and verify that a proportional change is indicated on the scope.

Repeat this at 10 MHz CW (lowband frequency).

9. Set the HP 8753A to sweep 300 kHz to 30 MHz. Verify a swept signal. Note the various power levels. This step verifies that the source can sweep through lowband and highband.

   Repeat this step sweeping from 2 to 15 MHz (lowband).

10. The A11 phase lock board assembly contains two diagnostic LEDs. A red LED is located at the top right-hand corner of the board assembly. An amber LED is located in the center of the board assembly and is more difficult to locate.

    The red LED should be off when the instrument is in CW, and should be flickering on and off rapidly at the sweep speed selected when the instrument is sweeping. A lit LED indicates phaselock condition, and off indicates not phaselocked (bandswitch relock).

    The amber LED is part of a pull-down circuit. When the LED is on, this indicates that the IF is not within the phaselock loop filter bandwidth. During normal operation this LED should light momentarily at retrace of each sweep. It may also light during the pretune mode of the phaselock sequence, but it should never light during the acquire and track modes. If the LED is on continuously, this indicates that the instrument is not able to phaselock.

    If either of these LEDs look abnormal, suspect that the source is not sweeping.

    If these checks pass, refer to receiver functional group troubleshooting. If there are problems with frequency or power, refer to source functional group troubleshooting.

FUNCTIONAL GROUP TROUBLESHOOTING

INTRODUCTION

There are four functional groups in the HP 8753A. Each of these functional groups contain various assemblies as shown in the following table. Some assemblies belong to more than one functional group.

Functional Group	Associated Assembly
Power Supply	A8 post-regulator A15 preregulator
Digital Control	A1/A2 front panel A9 CPU A10 digital IF A16 rear panel A18 display
Source	A3 source A4 sampler/mixer A7 pulse generator A11 phase lock A12 reference A13 fractional-N (analog) A14 fractional-N (digital)
Receiver	A4/A5/A6 sampler/mixer A10 digial IF A7 pulse generator

This section is to be used for troubleshooting a faulty functional group to the assembly level after the specific functional group has been identified through the procedure in System Level Troubleshooting. The theory of operation for each functional group and the Overall Block Diagram is located under the Theory of Operation tab.

Refer to Figure 11, which shows the location of all major assemblies in the HP 8753A network analyzer. For convenience when troubleshooting, a location diagram label is attached under the top cover of the instrument.

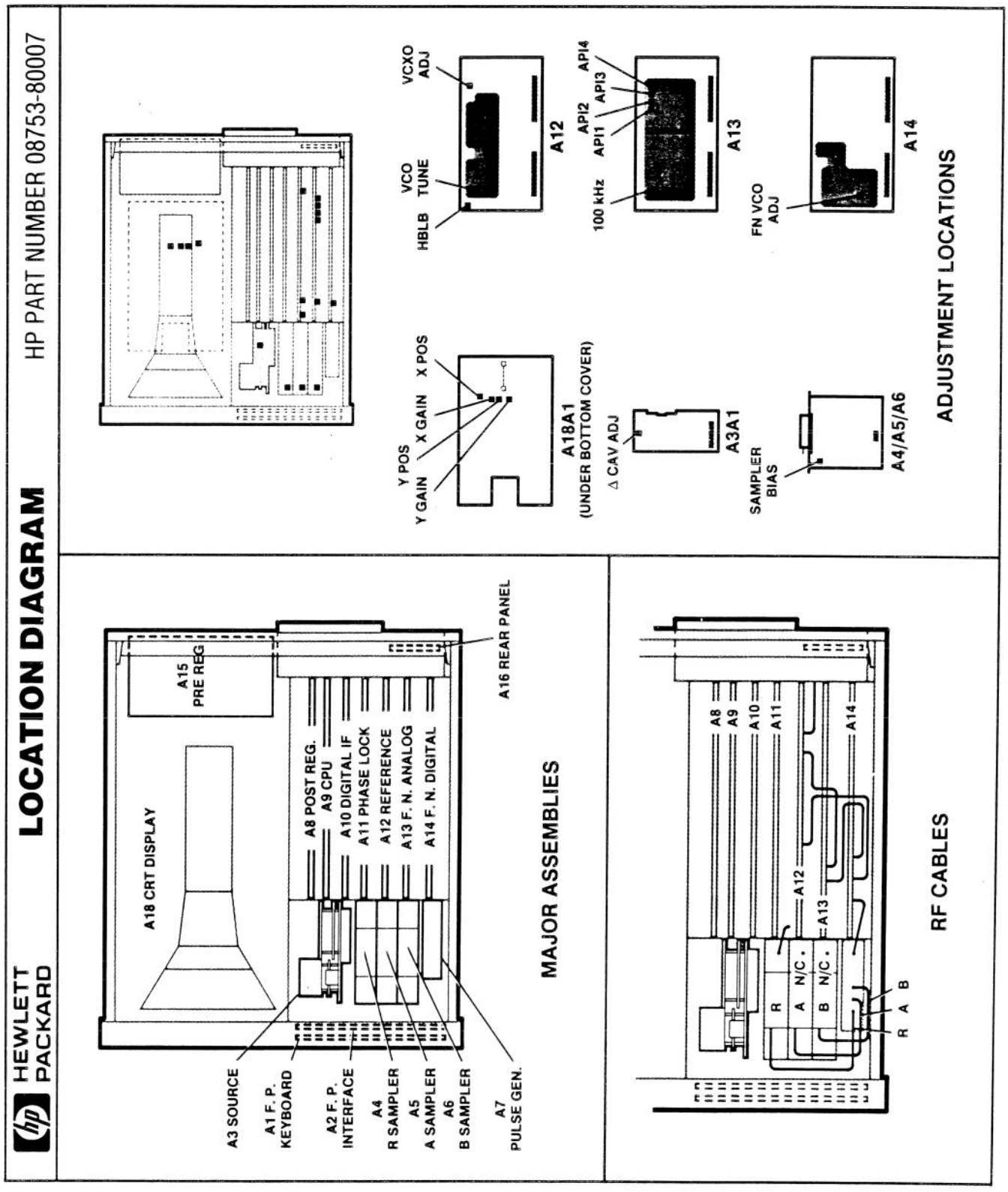


Figure 11. HP 8753A Assemblies Locations

POWER SUPPLIES FUNCTIONAL GROUP TROUBLESHOOTING

The A15 preregulator assembly switching power supply will operate when all external loads are disconnected from it. Figure 12 shows places to probe on the interconnecting cable between the A15 preregulator assembly and the A8 post regulator assembly to measure five of the seven voltages supplied from the A15 preregulator. Table 1 lists nominal voltages at the A8J2 connector, as well as voltages measured under varying operating conditions.

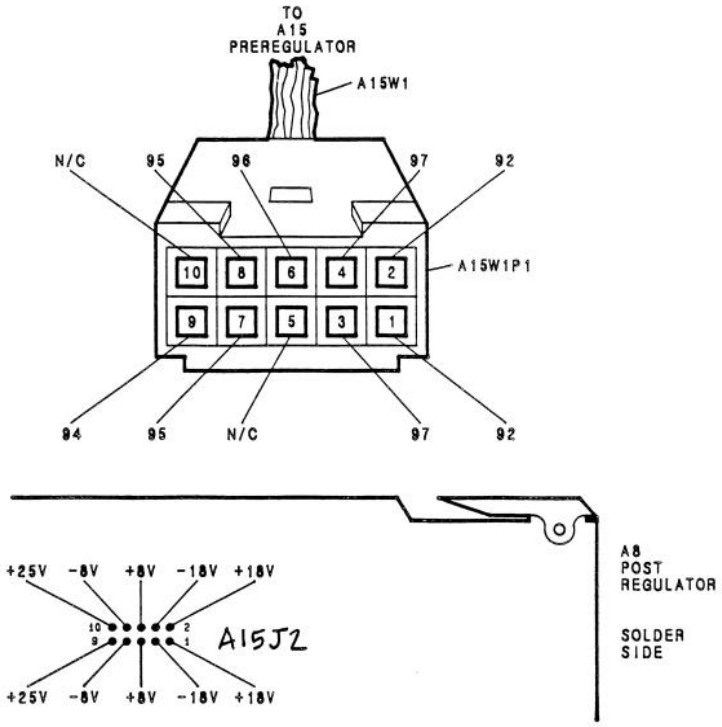


Figure 12. A15W1P1 Connector Detail

Table 2. Preregulator Output Voltages

	Voltages Measured at A15W1P1				
A15 Pre-Regulator Mnemonic	**No Load**	**A8 Connected**	**Fan on, and A8 Connected**	**Full Load**	**Nominal Current**
+25V	43V	35V	26.5V	26V	250ma
+18V	31V			25V	3A
+8V	13V	10.5V	8V	7.5V	350ma
+5VD				5V	4.5A
-8V				-8V	1.5A
-18V	-31V	-25V		-18V	1A

Faults caused by any assembly within the HP 8753A network analyzer can result in an error symptom in the power supply functional group.

Both the A15 Preregulator and the A8 Post Regulator assemblies contain their own sensing and shutdown circuitry for destructive protection from power supply problems. Each assembly has LEDs which indicate these shutdown conditions.

Two LEDs are located on the rear of the A15 Preregulator near the power line fuse. The green LED is a temperature indicator inside the A15 Preregulator casting and is normally on. The red LED is the shut down LED and is normally off. Shut down will be discussed later.

LEDs for the following signals are on the top edge of the A8 Post Regulator assembly (from left to right):

+15VDSP
-15VDSP
AGND
+5VD
SDIS
-15V
-12.6VPP
+15V
+5VU
-5.2V
+22V
+6V

The +5VD supply is routed to the A8 Post Regulator assembly to the LED near A8TP4, filtered, and then used for the alert and shutdown circuitry on the A8 Post Regulator assembly. The +5VD LED is on when this +5VD filtered signal is present. The +5VD supply is regulated by the A15 Preregulator assembly. The above A8 Post Regulator LEDs will be discussed later under "Symptoms and Solutions".

Table 3 shows the nominal voltages and currents found on the output of the A8 Post Regulator assembly, as well as the supply on the A15 Preregulator assembly that precedes it.

Table 3. A8 Post Regulator Output Voltages

Derived from A15 Prereg. Signal	Mnemonic on A8 Post Reg.	A8 Test Point	Nominal Voltage	Nominal Current
+25V	+22V	11	22.0	250ma
+18V	+15V	8	15.0	1.4A
+18V	+15VDSP	1	15.0	1.3A
+18V	+15VSRC	----	15.0	----
+18V	+15VPP	----	15.0	----
+18V	+ FAN V	----	+5.6 to +14.7	----
+18V	+6V	12	6.0	180ma
+8v	+5VU	9	5.1	250ma
+5VD	+5VD	4	5.16	4.5A
GNDA	AGND	3	0.00	----
-8V	-5.2V	10	-5.16	1.5A
-18V	-12.6VPP	7	-12.7	----
-18V	-15V	6	-15.0	650ma
-18V	-15VDSP	2	-15.0	360ma
----	SDIS	----	----	----

Shut down of supplies on the A15 Preregulator assembly can be caused by:

* The +10V bias supply is missing for the control circuitry.
* The incoming line voltage is less than 85 Vrms.
* Ambient temperature near the switching power transistors (inside the casting) > 85° C.
* If the +5VDSENSE line opens, the +5VD supply shuts down.

Shut down of supplies on the A8 Post Regulator assembly can be caused by:

* Incorrect voltages from the A15 Preregulator.
* Short circuits on assemblies
* Excessive heatsink temperature.

To disable the shutdown circuitry, ground TP 5 (SDIS) on the A8 Post regulator. The power supplies will attempt to function and allow further troubleshooting.

The +15VDSP and -15VDSP regulated voltages supply the A18 display assembly. The individual regulators for these supplies are not controlled by the A8 post regulator shutdown circuitry. This allows the A18 display assembly to operate for troubleshooting purposes when other supplies may be off.

SYMPTOMS AND SOLUTIONS

1) **Symptom:**

The green LED on the rear panel of the A15 preregulator assembly is off. This means that the bias supply is lacking the correct voltage for operation.

Probable Solutions:

A) The line voltage selector switch may be set incorrectly.

B) The main line fuse may be open.

C) There may be a problem on the A15 preregulator assembly. Check the output voltages from the A15 preregulator assembly to the A8 post-regulator assembly, using Figure 12 and Table 2.

2) **Symptom:**

The red LED on the rear panel of the A15 Preregulator is on.

Probable Solutions:

A) This LED indicates an A15 Preregulator shutdown, possibly due to a short circuit conditon. It could be a short circuit of the + 5VD (digital) which supplies the entire instrument. Also the secondaries of the transformer or the wires running to the A8 Post-regulator could be shorted. Check the +5VD (digital) located on the A17 Motherboard. (Refer to wiring list). If this is good, then check the ouput voltages from the A15 Preregulator to the A8 Post Regulator, using Figure 3 and Table 1.

B) There may be insufficient line voltage to the instrument. Supplied with 115 volts, the voltage selector switch may be set to 230 volts.

C) Defective part on the A15 Preregulator. Same procedure as A.

D) An overtemperature conditon may exist. The instrument is overheating and shutting itself down. The fan may have failed, power supply shorted, operating in an environment that is too hot, etc. Verify that the fan is working and smell for smoke.

3) **Symptom:**

The two A15 Preregulator rear panel LEDs are blinking, or both are on steady.

Probable Solutions:

A) If the LEDs are on steady then suspect a dead short by some component in the power supply loop (A15 preregulator assembly), or an overtemperature condition exists.

B) If the LEDs are blinking, suspect a low voltage problem or a low supply voltage.

4) **Symptom**:

Some or all of the green LEDs on the A8 post regulator are blinking, or are off.

Probable Solutions:

A) There could be a short circuit (overcurrent condition). The problem could be any of the assemblies supplied by the instrument. On the A8 post regulator, connect TP5 to TP3. This grounds the A8 post regulator SDIS (shutdown disable) line. Now look at individual supplies and compare to expected values in Table 2.

If any of these supplies look bad then refer to Table 3 to find out which output on the A15 preregulator assembly supplies this voltage. If the A15 preregulator assembly outputs are good, then refer to the motherboard wiring list in this binder to see which assemblies use these voltages. Remove one at a time to see if an assembly has a short.

B) An undervoltage condition may exist. The input voltage is low or one of the components on the A8 preregulator assembly is bad. Look at output voltages on the A15 preregulator assembly that supplies the voltage in question. Refer to Figure 12 and Table 2. If this voltage is good then suspect the A8 post regulator.

C) An overvoltage condition may exist, which probably means a regulator on the A8 post regulator assembly is bad. Verify the input to the A8 post regulated supply in question. If good, then the problem is with the A8 post regulator.

Fuse Locations

The main instrument fuse is located and accessed from the rear panel of the instrument. See Figure 15. Individual supply fuses are located at the top of the A8 post regulator assembly. The A15 preregulator assembly contains a fuse (inside the casing). If this fuse opens, suspect a problem with components in the A15 preregulator assembly.

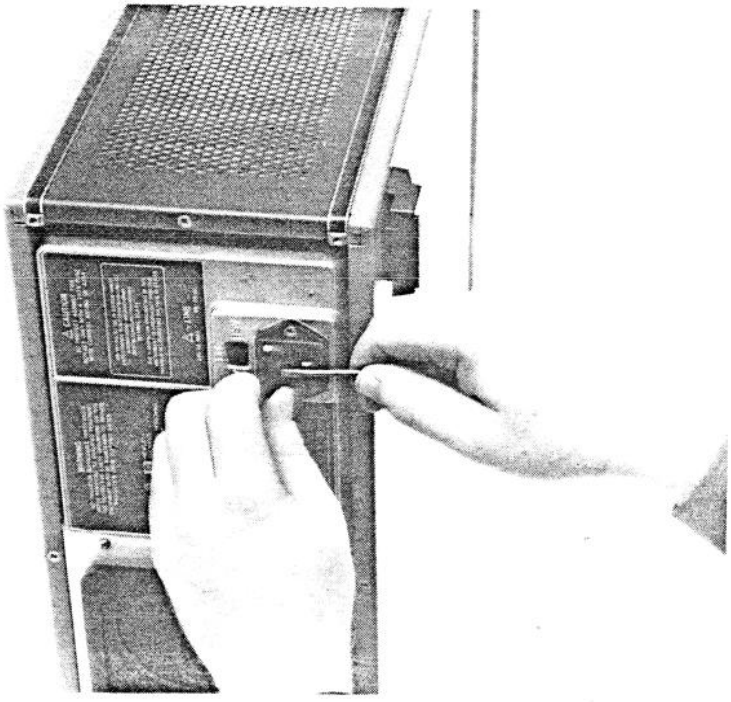


Figure 15. Removing Line Fuse

SOURCE FUNCTIONAL GROUP TROUBLESHOOTING

The source functional group includes the assemblies listed below. Refer to Figure 17, which illustrates the source functional group block diagram.

A3 source assembly
A4 sampler/mixer assembly
A7 pulse generator assembly
A11 phaselock assembly
A12 reference assembly
A13 fractional-N assembly (analog)
A14 fractional-N assembly (digital)

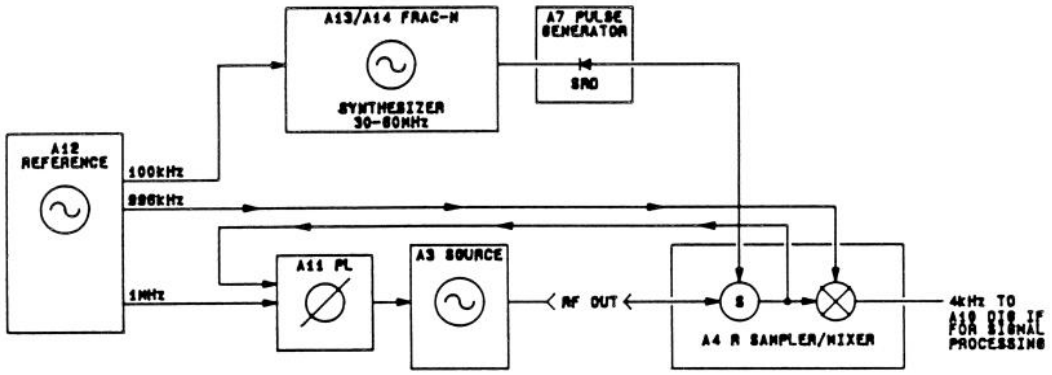


Figure 17. Source Functional Group Block Diagram

Follow this step-by-step procedure when you suspect a source problem.

R INPUT LEVEL CHECK

1. To eliminate the possibility of a failure being caused by the A4, A5 or A6 sampler/mixer assemblies, a few simple tests can be performed. First, check that the power level into the R input (A4 sampler assembly) is greater than -35 dBm. A minimum signal level is required to phase lock the source group.

INTERCHANGE SAMPLERS

2. Without physically removing the sampler/mixer assemblies, the A input sampler/mixer can be made to function electrically as the R input sampler/mixer. This is a very quick check to verify proper operation of the R input sampler/mixer.

   Remove the SMB connector of the flexible RF cable connecting the A4 sampler/mixer to the A11 phaselock board assembly (this is located on the top rear cover of the sampler). Attach this A11 cable to the similar SMB connector located on the A5 (A input) sampler/mixer. Make sure there is power into input A (front panel N connector), or there will be a loss of phaselock.

   Repeat this procedure for the A6 (B input) sampler/mixer. If the symptom remains the same, there is a high confidence that the problem is not sampler-related. If the error symptom goes away, suspect the sampler that was connected when the error message was displayed.

   When the preceding steps have passed, the confidence level for the A4/A5/A6 sampler/mixers is 40%.

SOURCE PRETUNE CHECK

Useful analog bus nodes:

15
16

3. The pretune portion of the source group phaselocking will now be exercised (see Figure 18). The following sequence of keys will allow the user to "break the loop" to test the A11 phaselock and A3 source assemblies. Connect the equipment as shown in Figure 19.

   Press **[MENU] [CW FREQ]** to select CW.
   Press **[SYSTEM] [SERVICE MENU] [SERVICE MODES] [SRC TUNE ON]** to activate the SRC tune function in service modes.

   Set the HP 8753A frequency to 10 MHz. Observe a 12 to 14 MHz signal on the oscilloscope. With the rotary pulse generator (RPG), step keys, or entry pad, vary the CW frequency. The frequency displayed on the scope should be 2 to 6 MHz higher than the display frequency.

   NOTE: The waveform changes frequency in discrete steps. This is due to the frequency resolution of the pretune DAC. These steps should be approximately 1 to 2 MHz.

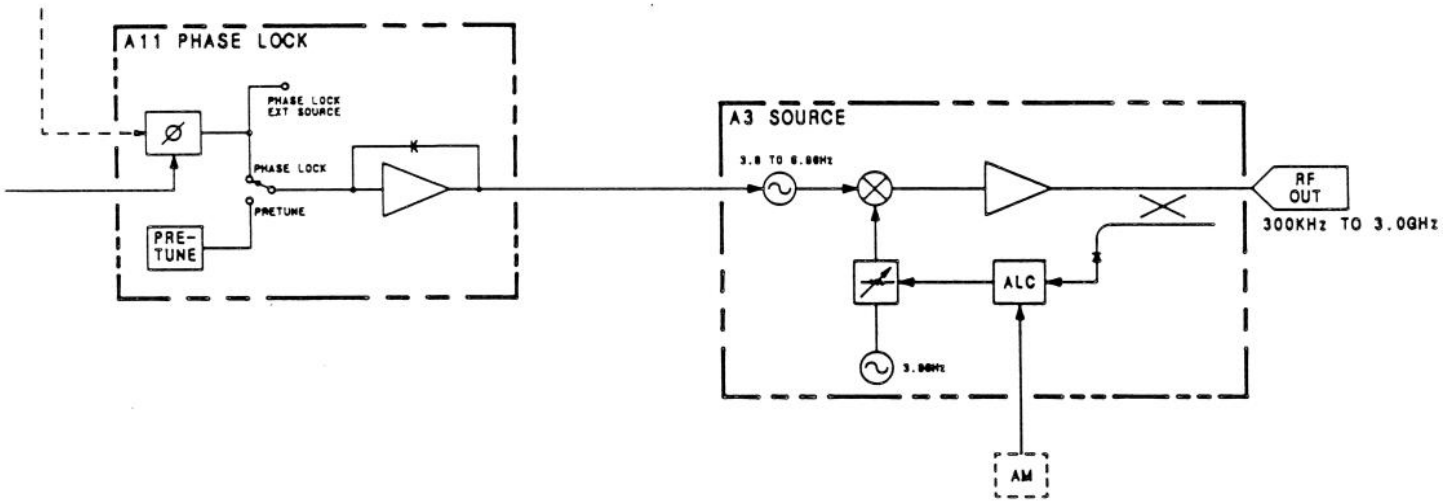


Figure 18. Source Pretune Block Diagram

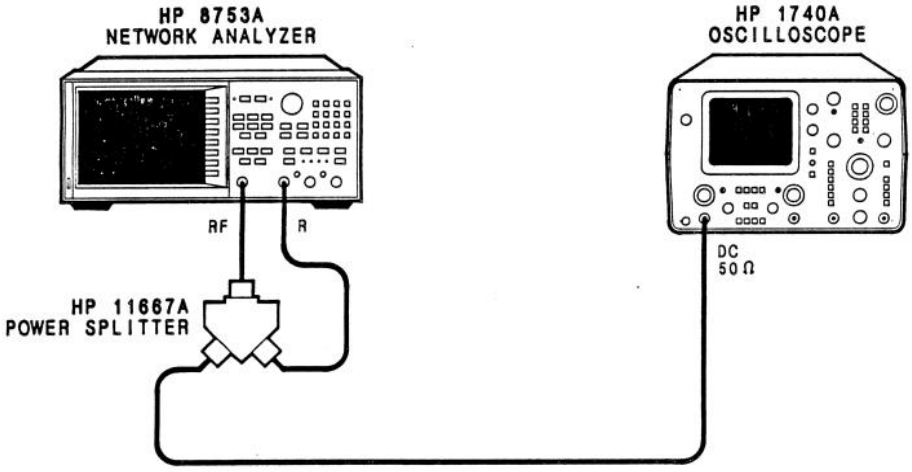


Figure 19. Pretune Test Equipment

4. Check that the signal amplitude displayed on the scope can be varied by changing the instrument power level. This verifies that the ALC circuitry of the source assembly is working.

   Press **[MENU] [POWER]**.

   Adjust the power level with the RPG, step keys or entry pad and verify an appropriate change on the oscilloscope.

   Useful analog bus nodes (to check ALC operation):

   1
   2
   3
   4
   6
   7

   When the preceding steps have passed, confidence levels for the following assmeblies may be assumed:

A3 source	80%
A11 phaselock	40%

A14 FRACTIONAL-N VCO CHECK

5. Verify that the A14 fractional-N synthesizer is producing its 30 to 60 MHz sine wave main output signal.

   Remove the A14 fractional-N assembly (digital) to A7 pulse generator assembly flexible RF cable at the A7 pulse generator assembly. Leave one end connected to the A14 fractional-N assembly and attach an SMB-to-BNC adapter to the other end (see Figure 20). Verify the fractional-N VCO output on the scope.

   Select CW mode (30 MHz) and see if a 30 MHz sine wave is displayed on the scope. Set the CW frequency to 50 MHz and check that 50 MHz is displayed on the scope. If so, the synthesizer (A13 & A14) is probably working. If not, continue this procedure. If there are problems, refer to A13 and A14 Fractional-N Troubleshooting in back of the Assemblies tab in this manual.

   Useful analog bus nodes:

   29

   Use the internal counter to check **FRACN** with the HP 8753A in CW, and **DIV FRACN** at 100 kHz.

   When the fpreceding steps have passed, confidence levels for the following assemblies may be assumed:

A13 fractional-N (analog)	90%
A14 fractional-N (digital)	90%

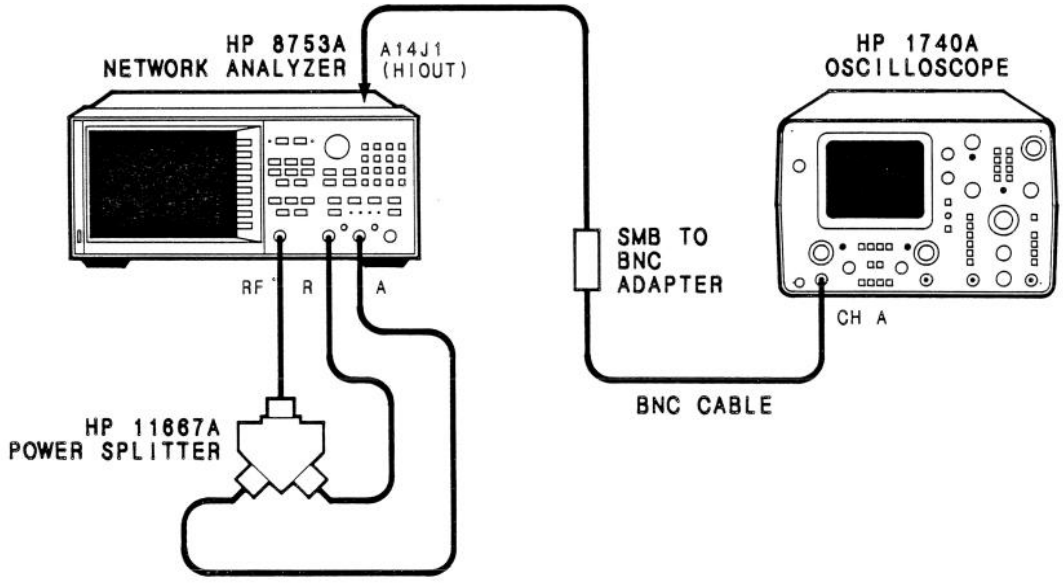


Figure 20. Synthesizer Test Equipment

A7 PULSE GENERATOR CHECK

6. Connect an SMB tee to the R sampler/mixer IF output, so that the IF can be simultaneously routed to the A11 phaselock assembly and to an oscilloscope.

   Press **[MENU] [CW FREQ]** to select CW.

   Press **[SYSTEM] [SERVICE MENU] [SERVICE MODES] [SRC TUNE ON]**.

   Select 50 MHz as a pretune value and press **[FRACN TUNE ON]**. Tune the fractional-N synthesizer output (LO) to 40 MHz. Check that the scope displays a 10 to 14 MHz sinusoidal signal. Vary the fractional-N synthesizer output and check that the IF signal on the oscilloscope also varies. Press **[MENU] [POWER]**. Vary the source RF power output and check that the IF signal level changes. Refer to Figures 21 and 22.

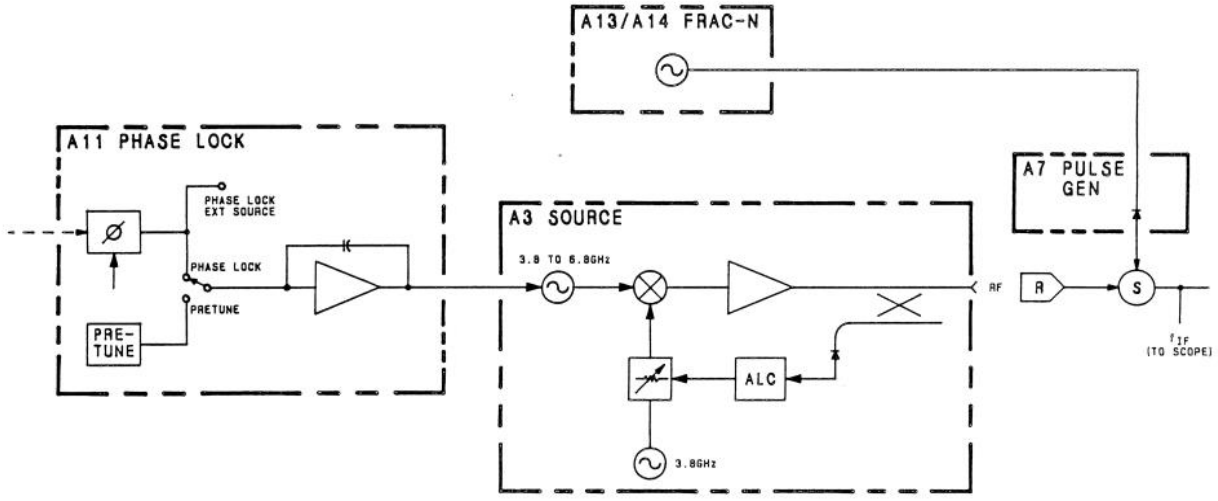
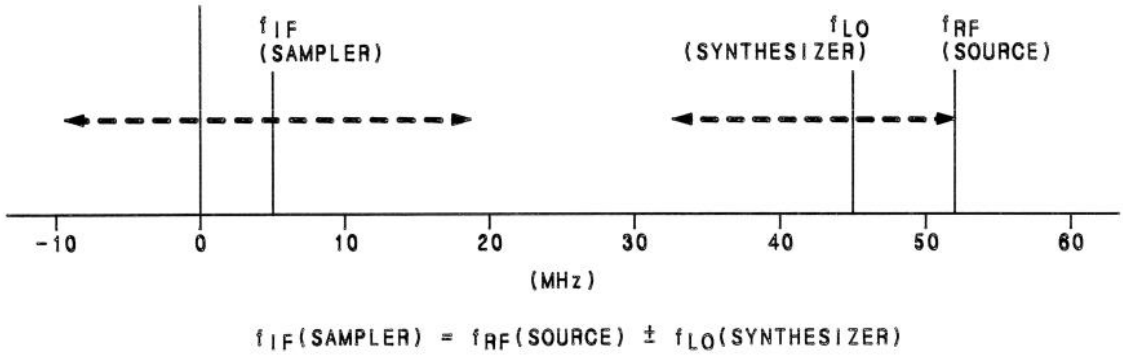


Figure 21. Pulse Generator Test Block Diagram



f(IF,scope)= f(RF,source) +/- f(LO, synthesizer)

Figure 22. Frequency Domain Diagram

Useful analog bus nodes:

17
18
19
20

When the preceding steps have passed, confidence levels for the following assemblies may be assumed:

A3 source	90%
A4 sampler/mixer (R input)	40%
A7 pulse generator	90%
A11 phaselock	40%
A12 reference	20%
A13 fractional-N (analog)	90%
A14 fractional-N (digital)	90%

A12 REFERENCE FREQUENCIES CHECK

7. Refer to Table 4 to verify a major portion of the A12 reference assembly frequencies used by the source functional group. Figures 23 and 24 illustrate some typical plots.

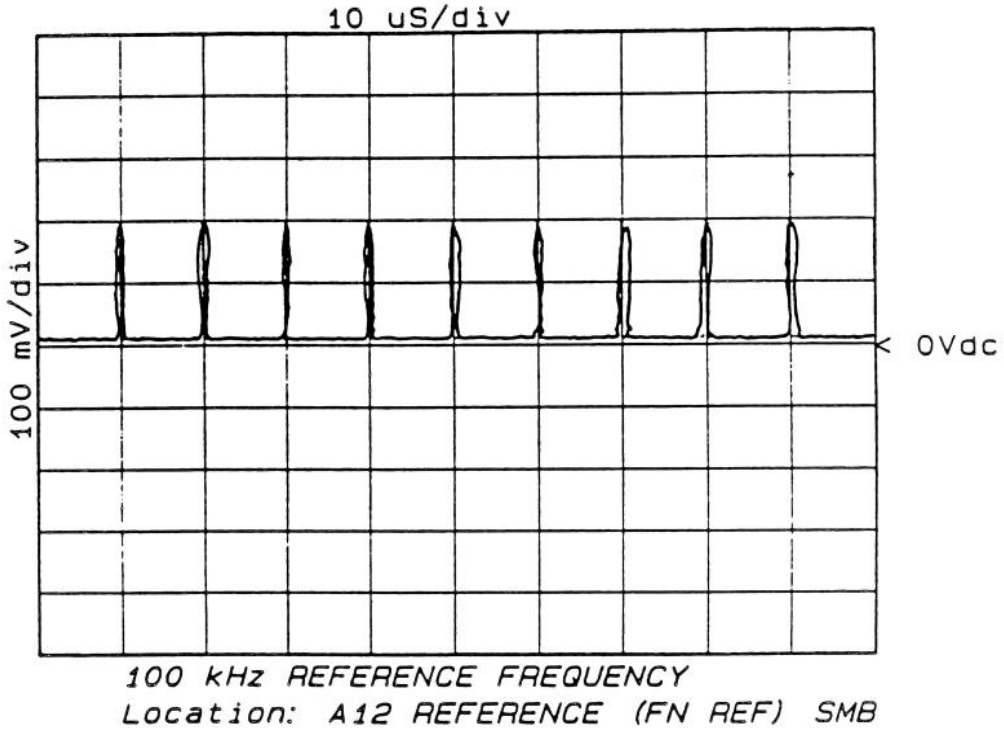


Figure 23. 100 kHz Reference

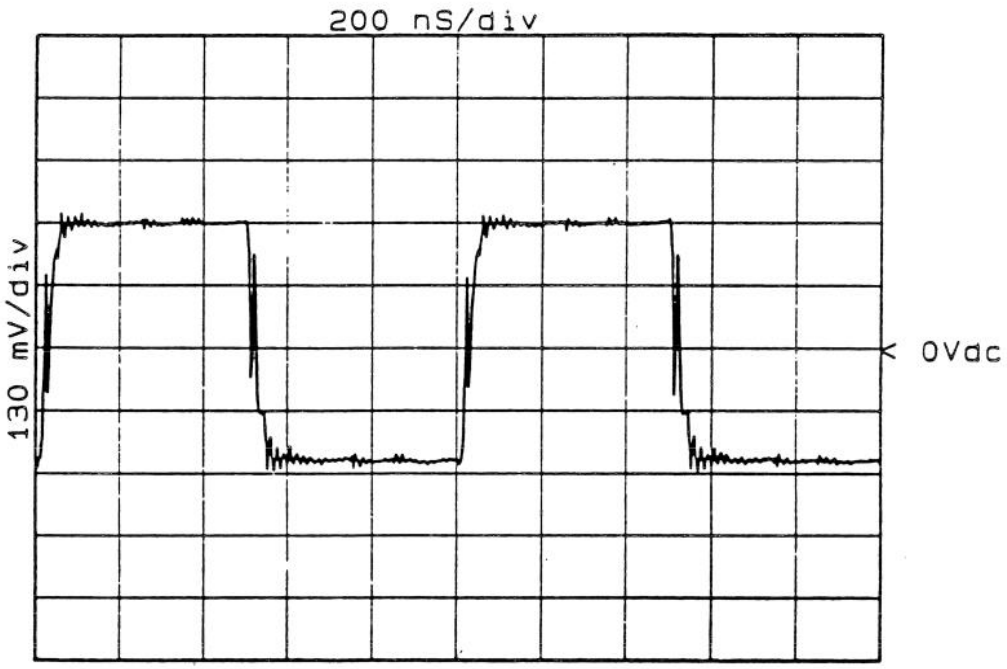


Figure 24. 1 MHz Reference

Table 4. Key Source Reference Frequencies

Signal Description	Wiring List Mnemonic	Location	Instrument Setup
100 kHz reference	FN100kHzREF	A13TP5	CW or sweep
1 MHz reference	PLREF+	A11J1P24,28	CW (16 MHz to 3 GHz)
*300 kHz to 16 MHz Reference	PLREF+	A11J1P24,28	CW (300 kHz to 16 MHz)
* The PLREF+ signal (lowband) is a square wave and should change frequency to follow the output frequency of the instrument.			

These waveforms verify only 30% of the A12 reference assembly, but 90% of the frequencies are used by the source functional group.

Useful analog bus nodes:

21
25

A11 PHASELOCK CHECK

8. Press **[PRESET] [SYSTEM] [SERVICE MENU] [SERVICE MODES]**.

Press **[PLL AUTO OFF]**.

This allows the phaselock to go through a normal phaselock sequence so the user can view the process. This key defeats the automatic pretune calibration routine.

Press **[MENU] [SWEEP TIME]**.

Enter a slow sweep time, such as 5 to 10 seconds. This will allow various intervals of the phaselock sequence to be seen (pretune, acquire, and track).

To start this sequence, press **[SYSTEM] [SERVICE MENU] [SERVICE MODES] [PLL DIAG ON]**. Each step in the phaselock sequence will be shown on the display.

Press **[PLL PAUSE [CONT]**. (This key should now read **[PLL PAUSE [PAUSE]]**.) The sequence will pause and the CRT will display what the phaselock loop is doing at that particular time.

An example is ACQUIRE (C2-B3), which indicates the HP 8753A is in the acquire mode of the phaselock sequence, monitoring channel 2 (C2), and is in band 3 (B3).

If there are problems in acquire or track mode, suspect the A11 phaselock assembly. For specific band related problems, refer to the key source reference frequencies in Table 5. If an error message appears, refer to Table 5A.

Table 5. HP 8753A Key Sweep Frequencies

RF Out (MHz)	Band	Frac-N (MHz)	Harmonic	1st IF (MHz)	2nd LO (MHz)	2nd IF (kHz)
.300-3.3	0,low	40.3-43.3	N/A	.300-3.3	.304-3.304	4
3.3-16	1,low	43.3-56	N/A	3.3-16	3.304-16.004	4
16-31	2,high	30-60	1/2	1	0.996	4
31-61	3,high	30-60	1	1	0.996	4
61-121	4,high	30-60	2	1	0.996	4
121-178	5,high	40-59	3	1	0.996	4
178-296	6,high	35.4-59.2	5	1	0.996	4
296-536	7,high	32.8-59.4	9	1	0.996	4
536-893	8,high	35.7-59.5	11	1	0.996	4
893-1607	9,high	33.0-59.5	27	1	0.996	4
1607-3000	10,high	31.5-58.8	51	1	0.996	4

Table 5A. Phase Lock Sequence and Associated Error Messages

Error Message	Phase Lock Mode Failure
No IF Found: Check R Input Level	Pretune not successful
No Phaselock	Detected IF, Pretune successful, but could not Acquire
Possible False Lock	Pretune, Acquire, and Track successful, but possibly locked to incorrect comb tooth
Phaselock Lost	Pretune and Acquire successful, but track mode not successful

If the message **NO PHASELOCK, POSSIBLE FALSE LOCK**, or **PHASELOCK LOST** is displayed, run Adjustement Tests, "ABUS Cor" and "Pretune Cor".

Press **[SYSTEM] [SERVICE MENU] [TESTS] [ADJUSTMENT TESTS] [4] [6] [X1] [EXECUTE TEST]** to run "ABUS Cor". Then press **[4] [8] [X1] [EXECUTE TEST]** to run "Pretune Cor". If "Pretune Cor" fails, the problem is most likely the A11 phase-lock assembly.

If the phase lock sequence appears to be working correctly and there are no error messages, confidence in the A11 phaselock assembly is 80%.

RECEIVER FUNCTIONAL GROUP TROUBLESHOOTING

The receiver functional group includes the following assemblies:

A4 R sampler/mixer
A5 A sampler/mixer
A6 B sampler/mixer
A10 digital IF

Refer to Figure 24A, which illustrates the receiver group block diagram and the relationship between the assemblies in that group.

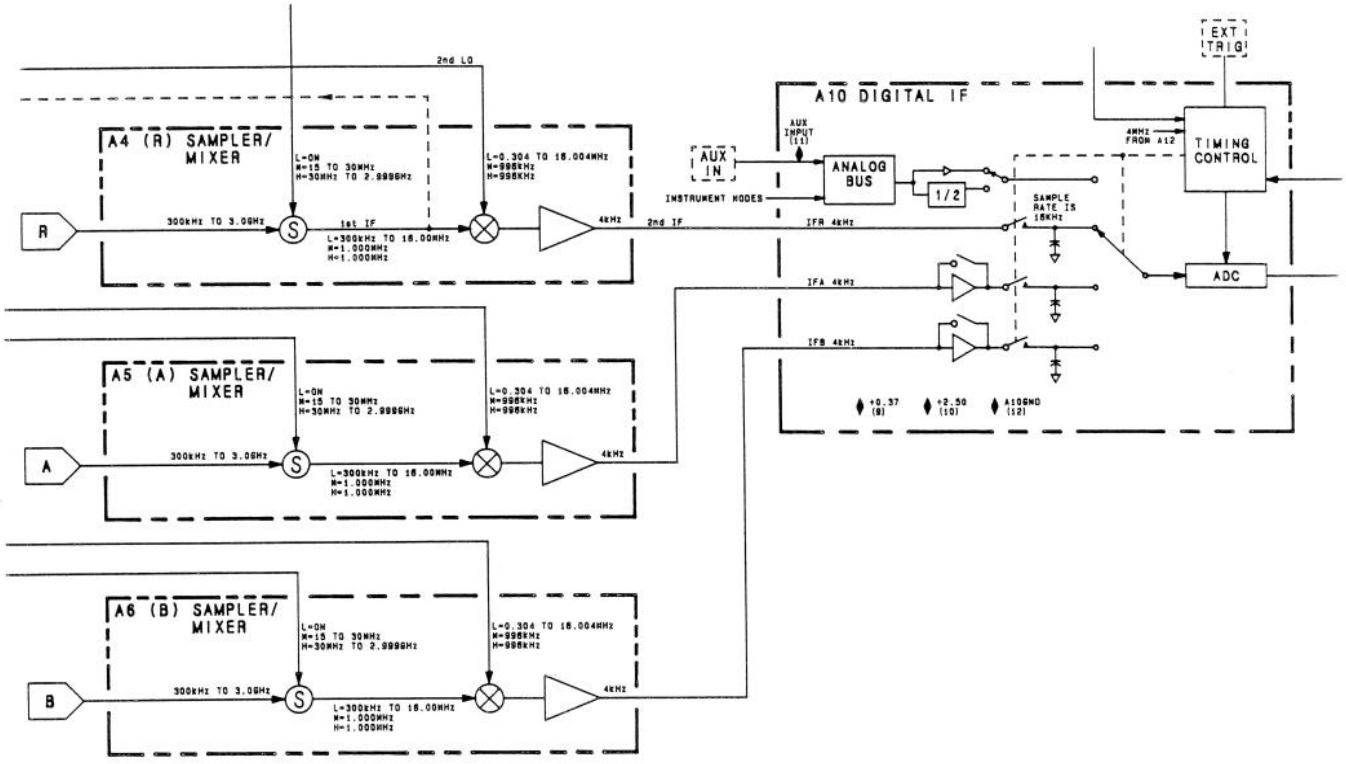


Figure 24A. Receiver Group Block Diagram

Follow this step-by-step procedure when a fault in the receiver functional group is suspected.

1. Verify that sampler/mixer assemblies A4, A5, and A6 are producing the second IF, which is a 4 kHz sine wave sent to the A10 digital IF assembly. Refer to Table 6 to locate this signal, and Figure 25 to identify its shape, frequency, and amplitude.

   Make sure there is power to the selected input (input A or B on the front panel).

Table 6. Location of 4 kHz Second IF Signals

Signal Description	Wiring List Mnemonic	*Location	Instrument Setup
R Input 2nd IF	IFR	A4P1-6	Any CW Freq.
A Input 2nd IF	IFA	A5P1-6	Any CW Freq.
B Input 2nd IF	IFB	A6P1-6	Any CW Freq.
* Remove the instrument bottom cover. These points are located on the bottom of the A17 motherboard.			

The waveforms should be approximately as shown in Figure 25. The IF should not vary and the signal amplitude displayed on the scope should vary with the source power. If there is a 4 kHz signal, then the sampler/mixers are working and the problem is with the A10 digital IF assemly. In this case, refer to A10 digital IF assembly troubleshooting in the assemblies section.

If the problem is frequency related, set the source to the CW frequency in question and check the second IF signals. As before, vary the sweep time and IF signals again.

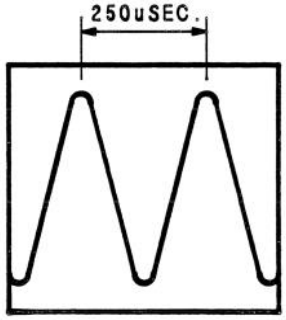


Figure 25. Typical IF Signal from A4/A5/A6 Sampler/Mixer

2. If there is no 4 kHz IF, make sure that the second LO frequencies from the A12 reference assembly are good. Refer to Table 25 and the waveform of Figure 26 to verify these frequencies.

Table 7. Location of the Highband Second LO Signals

Signal Description	Wiring List Mnemonic	Location	Instrument Setup
2nd LO to A4 Sampler	LO or YLO	A4P4,11	CW(16 MHz to 3 GHz)
2nd LO to A5 Sampler	LO or YLO	A5P4,11	CW (16 MHz to 3 GHz)
2nd LO to A6 Sampler	LO or YLO	A6P4,11	CW (16 MHz to 3 GHz)

Compare these signals to the waveform shown in Figure 26.

While in lowband (300 kHz to 16 MHz), the signal should still be a square wave, but will be 4 kHz offset from the frequency diplayed on the front panel. Compare the measured waveform to the one shown in Figure 26 for similarities. The frequency should be 996 kHz in highband.

INTERCHANGE SAMPLERS

3. Verify that the A5 and A6 sampler/mixers are good. Refer to the Figure 24A, Receiver Functional Group Block Diagram.

Without physically removing the sampler/mixer assemblies, the A input sampler/mixer can be made to function electrically as the R input sampler/mixer. This is a very quick check to verify proper operation of the R input sampler/mixer.

Remove the SMB connector of the flexible RF cable connecting the A4 sampler/mixer to the A11 phaselock board assembly (this is located on the top rear cover of the sampler). Attach this A11 cable to the similar SMB connector located on the A5 (A input) sampler/mixer. Make sure there is power into input A (front panel N connector), or there will be a loss of phaselock.

Repeat this procedure for the A6 (B input) sampler/mixer. If the symptom remains the same, there is a high confidence that the problem is not sampler-related. If the error symptom goes away, suspect the sampler that was connected when the error message was displayed.

When the preceding steps have passed, the confidence level for the A4/A5/A6 sampler/mixers is 40%.

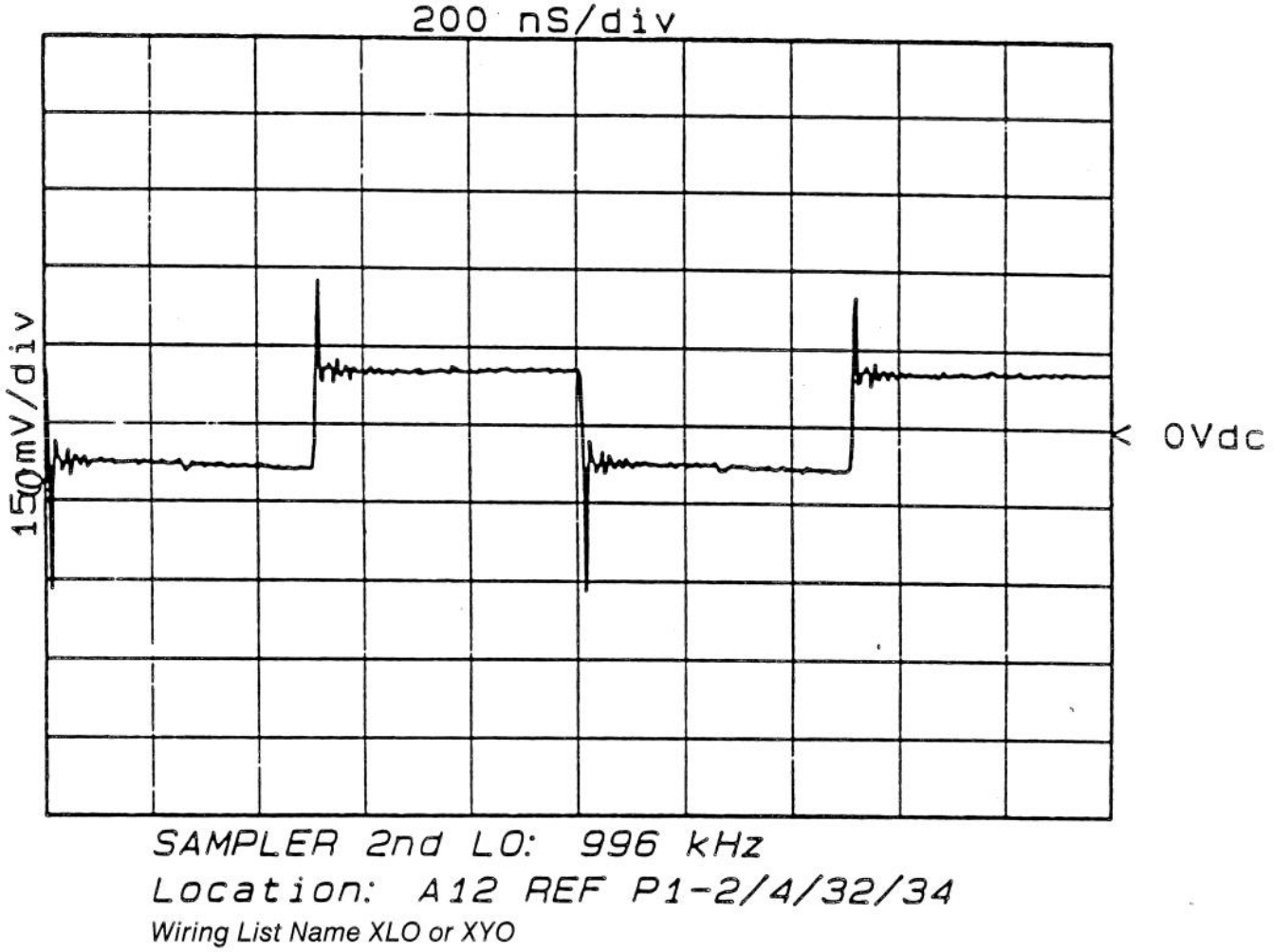


Figure 26. 2nd LO to A4/A5/A6 Sampler/Mixer in Highband (16 MHz to 36 GHz)

A1/A2 FRONT PANEL TROUBLESHOOTING

Refer to Figure 26A, which illustrates all assemblies that are included in the digital control functional group.

Verify that the front panel processor and keys are working by performing the following tests. If any of these tests fail, replace the A1 front panel keyboard assembly and the A2 front panel interface board assembly.

1. The front panel processor is exercised by an internal service test named **FR PAN WR/Rd**.

   Press **[SYSTEM] [SERVICE MENU] [TESTS] [INTERNAL TESTS]**. Press the ↑ and ↓ step keys to scroll through the internal tests to find **FR PAN WR/Rd**. Press **[EXECUTE TEST]** to run the test.

2. The front panel keys are exercised by two similar external service tests named **FR PAN SEQ** and **FR PAN DIAG**.

   FR PAN SEQ requires that the troubleshooter press respective front panel keys in a particular sequence. All front panel keys are tested.

   FR PAN DIAG allows the troubleshooter to press any key and have the display respond by printing the name of the key pressed. This test is very useful if a certain key is believed to be defective.

   Press **[SYSTEM] [SERVICE MENU] [TESTS] [EXTERNAL TESTS]**. Press the ↑ and ↓ step keys to scroll through the internal tests to find **FR PAN SEQ** or **FR PAN DIAG**. Press **[EXECUTE TEST]** to run the test.

3. Perform the Front Panel Error Codes check in the Troubleshooting Reference tab in this service manual. This check allows the user to exercise the front panel microprocessor by isolating the front panel from the main microprocessor on the A9 CPU board assembly, and the instrument bus.

A18 DISPLAY TROUBLESHOOTING

1. Verify that the power supply voltages to the A18 display assembly are correct by measuring them on the PC board assembly on the top of the display. If these are not within tolerance, verify the output voltages of the A15 preregulator, using Table 2 in Power Supply Group Troubleshooting.

2. If any type of trace is on the display, turn off the HP 8753A. Remove the A9 CPU board assembly, and turn the instrument on. The A18 display should show a test pattern.

   If the test pattern is visible, but the display is out of adjustment, refer to display adjustments in the Adjustments and Correction Constants section of this Service Manual. If the test pattern is not visible, suspect a problem with the A18 display assembly.

   If the display shows the correct test pattern but does not work with the instrument, suspect the input/output connector. If this looks good, the A9 CPU board assembly may be bad.

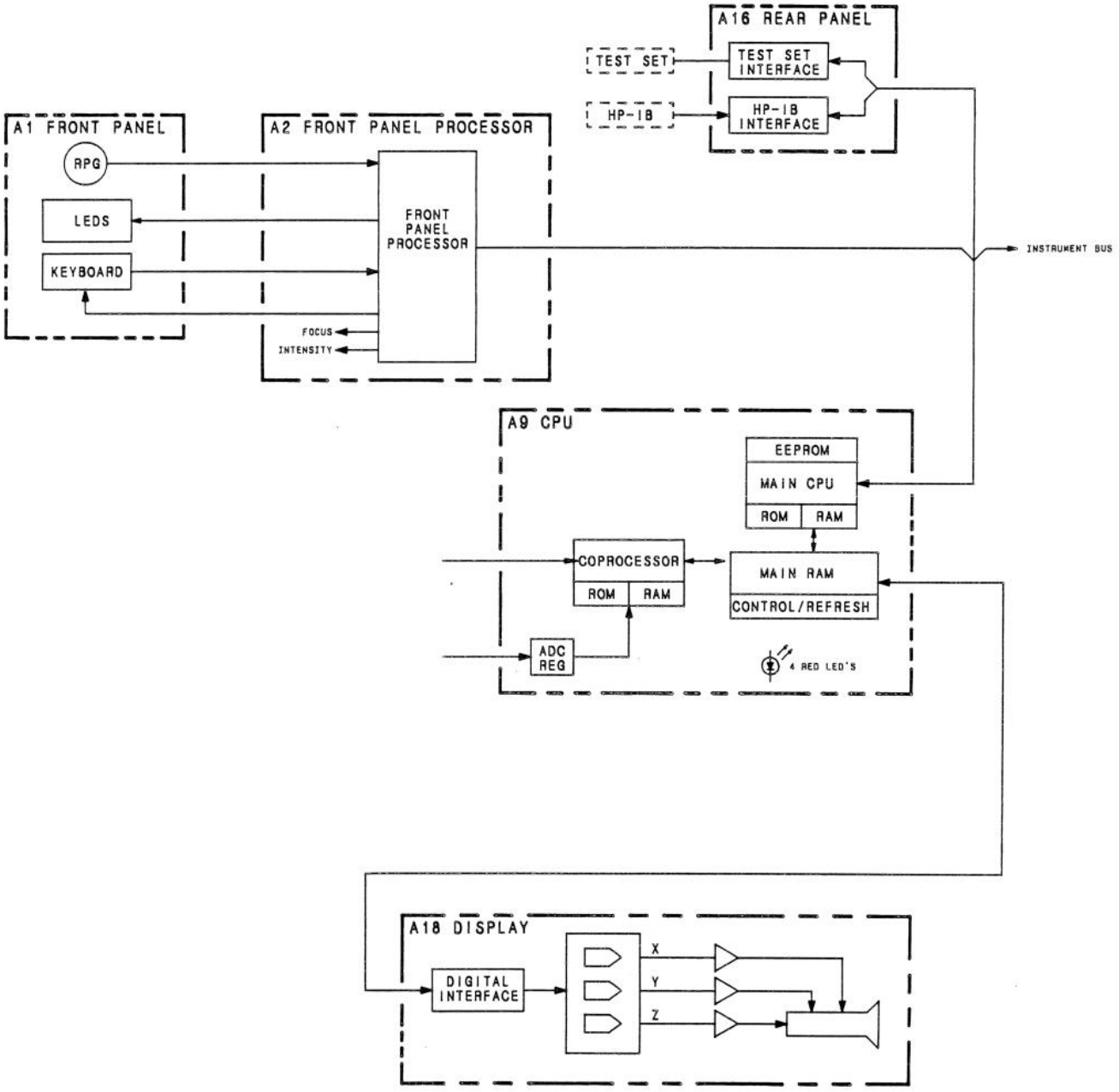


Figure 26A. Digital Control Block Diagram

A13 AND A14 FRACTIONAL-N (SYNTHESIZER) TROUBLESHOOTING

If the instrument has passed all internal tests but isn't sweeping, verify operation of the A13 and A14 fractional-N assemblies. These two assemblies provide the synthesizer and the sweeping function for the instrument.

The A13 and A14 assemblies combine to form a phaselocked 30-60 MHz VCO. This fractional-N combination is digitally swept by a counter circuit. The A3 source assembly is phase locked to this sweeping "synthesizer", and hence follows the fractional-N.

The key inputs to the A13 and A14 fractional-N assemblies include the 100 kHz reference and CPU control lines. The A14 fractional-N assembly (digital) contains the synthesizer controller, fractional-N controller, digital counter, timing, and VCO circuitry.

The A13 fractional-N assembly (analog) contains the analog portion of the synthesizer. This includes the phase detector, integrator, sample and hold, and analog phase interpolators (API's).

SYNTHESIZER CHECK

1. Make sure that the synthesizer is producing a 30 to 60 MHz sine wave by attaching a scope to the A14J1 SMB connector. Remove the flexible RF cable at the rear cover of the A7 pulse generator. Attach an SMB-to-BNC adapter, and connect a BNC cable to the scope. Observe the output from the fractional-N VCO.

   Select 30 MHz CW; a sine wave should be displayed on the scope. Change the CW frequency to 50 MHz and see if there is a change on the scope. If there is a change, there is high confidence that the synthesizer (A13 and A14) is working properly. If not, continue with this procedure.

2. Verify the 100 kHz (main reference) frequency from the A12 reference assembly. Probe A13TP5 and compare the result with the waveform of Figure 27. The waveform should be sharp 100 kHz pulses. If it is not, refer to the A12 reference assembly troubleshooting procedure to verify that the board is producing the correct signal. If the signal is good, continue with this procedure.

   Useful analog bus nodes:

   21
   29

   The **FRACN TUNE** service mode is also useful. Check the output at A14J2 (lowband), and A14J1 (highband) using the oscilloscope, frequency counter, or spectrum analyzer. Enter various frequencies between 10 and 60 MHz and check the scope. Select CW, and then turn **FRACN TUNE** on.

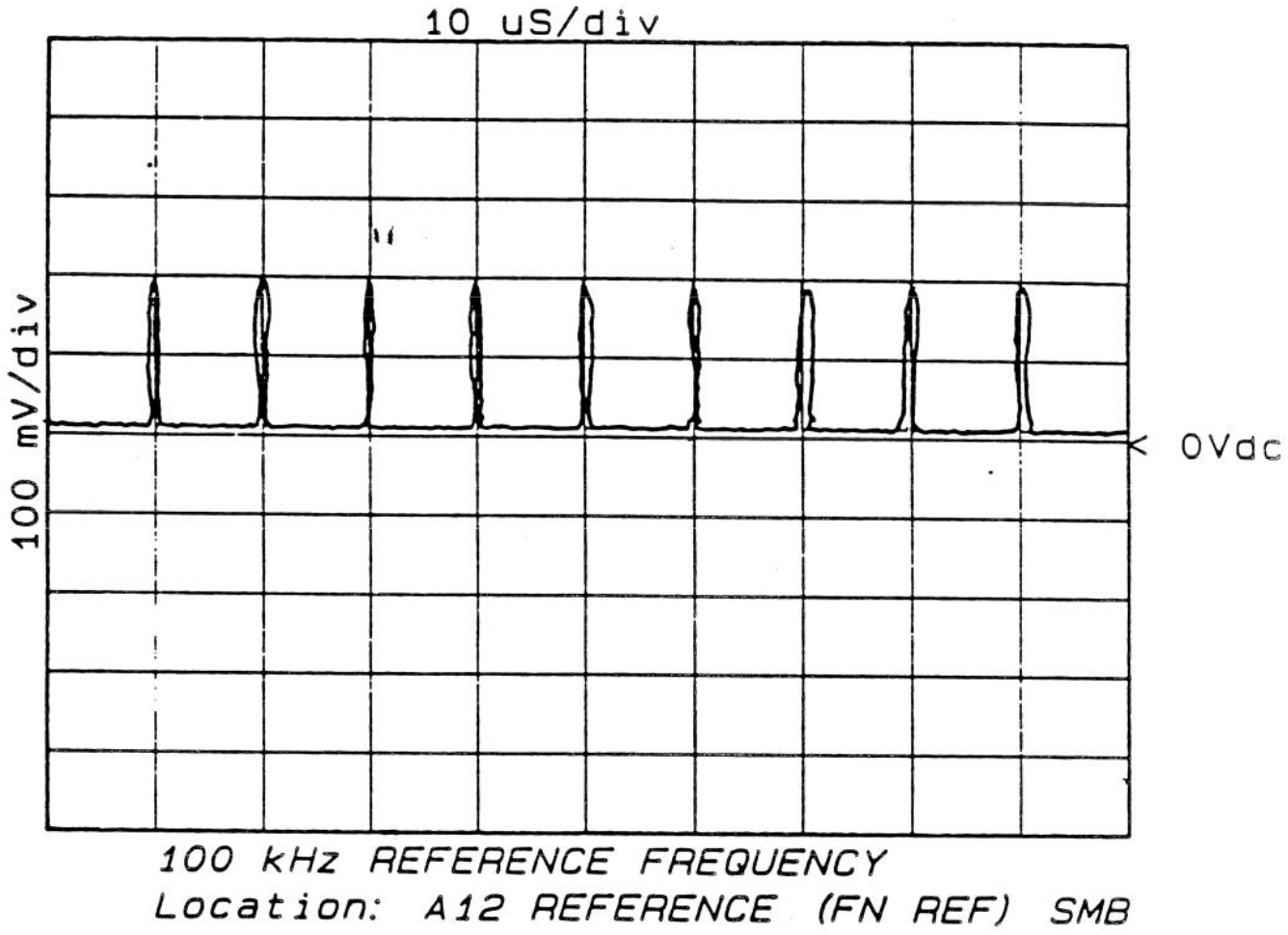


Figure 27. 100 kHz Reference

Figure 27. 100 kHz Reference.

3. The A14 Fractional-N assembly (digital), which controls most of the timing signals, will now be verified.

   Place the A14 fractional-N (digital) on an extender board.
   Remove A13 fractional-N (analog) board assembly.
   Ground A14 TP14 (**TUNE**).

   Press **[MENU] [CW FREQ] [50.010101] [MHz]**.

   Connect the scope to A14TP3 (CST, cycle start) and compare the measured result with the waveform of Figure 28. This verifies proper operation of the control lines from the A9 CPU assembly and the main control chip.

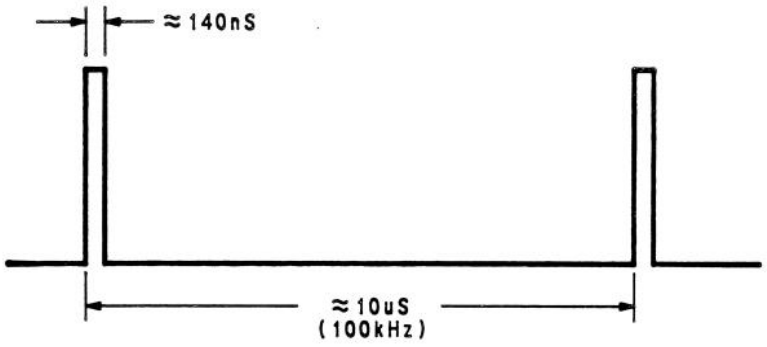


Figure 28. A14TP3 "CST" Waveform

Trigger the scope on A14TP3 (CST) and check the signals of Figure 29, using the test point and pin locations shown on the figure. If any of these have major deviations, the problem is with the A14 fractional-N assembly (digital).

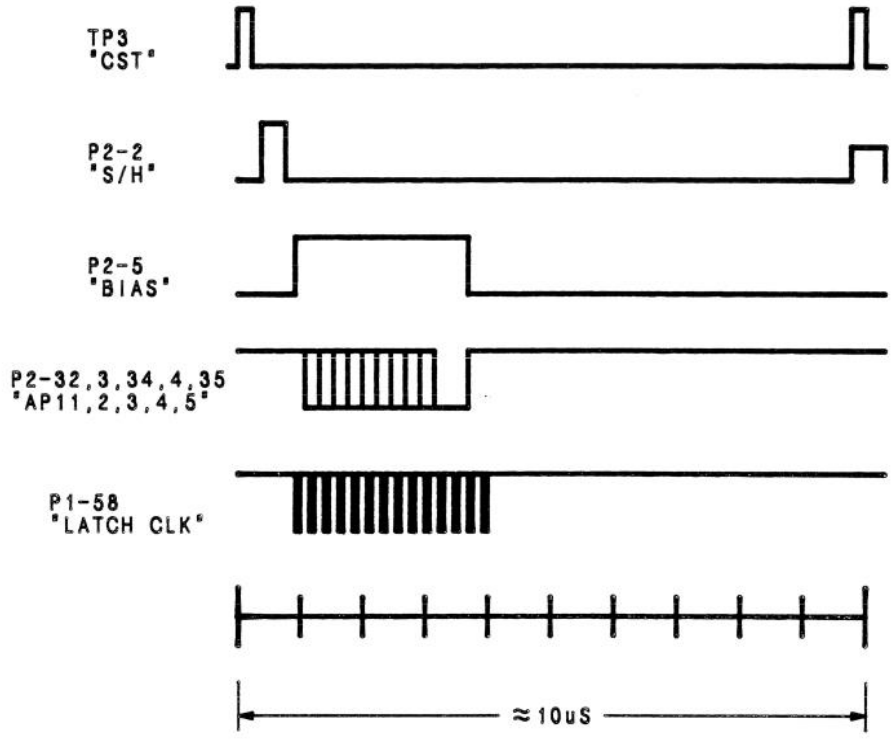


Figure 29. A14 Fractional-N Assembly Digital Waveforms

If the waveforms of Figure 29 are ok, connect the oscilloscope probe to A14J3 (VCO/N). Select 50 ohm input and DC trigger on the oscilloscope. You should see the waveform shown in Figure 30. The pulse width should be between 6 ns and 14 ns, and the amplitude should be approximately 1.8 V.

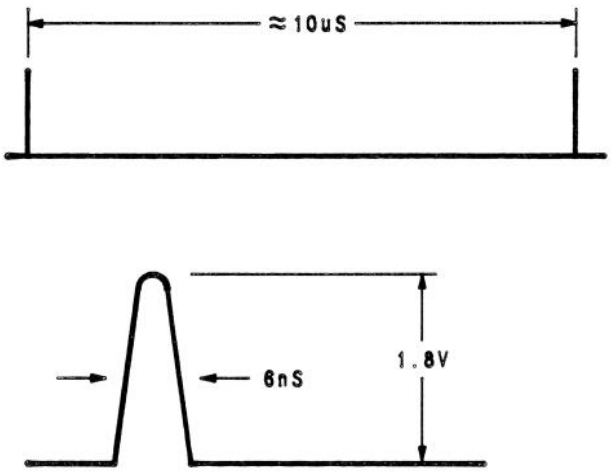


Figure 30. A14J3 VCO/N Waveforms

Press **[PRESET] [START] [3] [1] [MHz], [STOP] [6] [1] [MHz]** to set the start and stop frequencies.

Press **[MENU] [SWEEP TIME] [1] [0] [x1]** to change the sweep speed to 10 seconds.

Connect a scope to A14TP3 (CST). As the instrument sweeps, the period of the pulses should smoothly increase from 6 to 12 microseconds. If the pulses jerk forward or move backwards, this indicates a stuck bit on the A14 fractional-N assembly divider.

When the preceding steps have passed, the confidence level for the A14 fractional-N (digital) board assembly is 95%.

4. Remove the flexible RF cable from A13J1 (VCO/N) and connect the scope probe to A13TP1 (TUNE). The voltage should be -15 volts.

   Remove the RF cable from A13J2 (FN REF IN) and connect the scope probe to A13TP1. The voltage should be +15 volts. If this fails, the A13 fractional-N (analog) assembly is defective.

5. If the instrument is not sweeping, check the L SWP (L=sweep) signal on A14P2 pin 31. This signal is generated on the A14 fractional-N assembly (digital) and should toggle between 0V and 5V at the start of each sweep. It controls the A10 digital IF assembly data-taking process.

Troubleshooting Reference

INTRODUCTION

This Troubleshooting Reference section is made up of several small sections that describe the internal tools used to test, adjust, and troubleshoot the HP 8753A system. Details on how to access them are described in each section. Procedures that use these tools are provided in other sections of this manual; this section only describes what they are and what they do. Also provided in this section is a table that lists the related service procedures, a listing of the error messages that could be displayed on the CRT, and a description of the front-panel error codes.

The information is this section is organized as follows:

- Table of Related Service Procedures
- Analog Bus
- Service Modes
- Tests, Test Options, Self Diagnose
- Peek/Poke
- Firmware Revision
- Error Term (Calibration Coefficient) Troubleshooting
- ROM/RAM Tests
- Front Panel Error Codes
- Error Messages

URCE	MNEMONIC DESCRIPTION	A1/A2 FRONT PANEL	A3 SOURCE	A4 R SAMPLER/ MIXER	A5 A SAMPLER/ MIXER	A6 B SAMPLER/ MIXER	A7 PULSE GEN	A8 POST- REGULATOR		A9 CPU	
		J1	XA3J1	XA4J1	XA5J1	XA6J1	XA7J1	XA8J1	XA8J2	XA9J1	XA9J2
	L=ENABLE DIGITAL IF										17
	L=ENABLE FRAC N										45
	L=ENABLE FRONT PANEL	12								1	
	L=ENABLE PHASE LOCK										15
	L=ENABLE POST REG							45			46
	L=ENABLE REFERENCE										16
	L=ENABLE REAR PANEL										47
	L=ENABLE SOURCE		2							31	
0	EXTERNAL LEVELING (REAR PANEL)		40								
9	EXTERNAL LEVELING COMMON		39								
	L=EXTERNAL TRIGGER (REAR PANEL)										
	FAN VOLTAGE +							31			
	FAN VOLTAGE -							32			
. 34	FM COIL + (P/O YIG OSC)		37								
. 33	FM COIL - (P/O YIG OSC)		36								
2	FRAC N AP11										
	FRAC N AP12										
4	FRAC N AP13										
	FRAC N AP14										
5	FRAC N AP15										
	FRAC N BIAS										
	L=FRAC N HOLD										
9	FRAC N LATCH CLOCK										
4	FRAC N PHASE										
7	L=FRAC N PRETUNE										
		26									
	FRAC N VCO TUNE (FROM FRAC N ANALOG)										
	FRAC N TUNE 2 (FROM PHASE LOCK)						5				
		25									
, A9P2-49	INSTRUMENT ADDRESS 0 (LSB)	10	5							34	49
A9P2-20	INSTRUMENT ADDRESS 1		24							4	20
, A9P2-50	INSTRUMENT ADDRESS 2		4							33	50
A9P2-21	INSTRUMENT ADDRESS 3		23							3	21
, A9P2-51	INSTRUMENT ADDRESS 4 (MSB)		3							32	51
	INTERMEDIATE FREQ (4KHz) A				6						
	INTERMEDIATE FREQ (4KHz) B					6					
	INTERMEDIATE FREQ (4KHz) R			6							

8753A MOTHERBOARD WIRING LIST (2 OF 4)

A11 PHASE LOCK		A12 REFERENCE		A13 FRAC N (ANLG)		A14 FRAC N (DIG)		A15 PRE-REGULATOR	A16 REAR PANEL	A18 DISPLAY	FOCUS/ INT	FAN SUPPLY	CHASSIS MISCELLANEOUS NOTES
J1	XA11J2	XA12J1	XA12J2	XA13J1	XA13J2	XA14J1	XA14J2	J3	J6	J4	J2	J5	
	45* 15		45*		45*		45						
	16*		16						16				
									34 33 1				EXT LEVELING EXT TRIGGER
4 3												1 3	
					32 3 34 4 35		32 3 34 4 35						
					5 2 28 24	34	5 2 58 54						
											2		
				2		32 35							
											1		
	49 20 50 21 51		49 20 50 21 51		49 20 50 21 51		49 20 50 21 51		10 11 12 14 15				

SOURCE	MNEMONIC DESCRIPTION	A1/A2 FRONT PANEL	A3 SOURCE	A4 R SAMPLER/ MIXER	A5 A SAMPLER/ MIXER	A6 B SAMPLER/ MIXER	A7 PULSE GEN	A8 POST- REGULATOR		C
		J1	XA3J1	XA4J1	XA5J1	XA6J1	XA7J1	XA8J1	XA8J2	XA9J1
A2PX-19	L=INTERRUPT, FRONT PANEL	11								9
A8P1-60	L=INTERRUPT, POWER FAIL							60		
A10P2-2	L=INTERRUPT, CO-PROCESSOR									
A10P2-32	L=INTERRUPT, EXTERNAL									
A9J2-14	L=INTERRUPT, PHASE LOCK									
A16P1-6	L=INTERRUPT, RS232									
A16P1-27	L=INTERRUPT, HP-IB									
A9P1-2, A9P2-19	L=INSTRUMENT WRITE (H=READ)	9	22							2
A9P1-8 , A9P2-23	INSTRUMENT DATA 0 (LSB)	1	28					7		8
A9P1-38, A9P2-53	INSTRUMENT DATA 1	2	9					37		38
A9P1-7, A9P2-24	INSTRUMENT DATA 2	3	27					6		7
A9P1-37, A9P2-54	INSTRUMENT DATA 3	4	8					36		37
A9P1-6, A9P2-25	INSTRUMENT DATA 4	5	26					5		6
A9P1-36, A9P2-55	INSTRUMENT DATA 5	6	7					35		36
A9P1-5, A9P2-26	INSTRUMENT DATA 6	7	25							5
A9P1-35, A9P2-56	INSTRUMENT DATA 7 (MSB)	8	6							35
A14J1-5	MIDBAND (TO SAMPLER/MIXER)			9	9	9				
A10P1-28	L=HIGH BAND (TO REFERENCE)									
A10P1-23	L=LOW BAND (TO MIXER/SAMPLER)			8	8	8	12			
A12P1-54	PHASE LOCK REFERENCE +									
A12P1-58	PHASE LOCK REFERENCE -									
A8P1-30	L=POWER-ON/PRESET	14						30		
A8P1-3	L=SHUTDOWN							3		
A3P1-3	L=SOURCE HOT (OVERTEMP)							8		
A14P2-31	L=SWEEP									
A11P1-2, 32	YIG OSC COIL +		35							
A11P1-1, 31	YIG OSC COIL -		34							
A3P1-33	L=YO HOT							9		
A11P1-6, A11P1-36	1V/GHz		38							
A12P1-2, 32	2nd LO (TO MIXERS, 0 DEG)			11	11	11				
A12P1-1, 34	2nd LO (TO MIXERS, -90 DEG)			4	4	4				
A9P2-48	4MHz CLOCK FOR HP-IB									
A12P2-36	4MHz REF FOR DIGITAL IF									

8753A MOTHERBOARD WIRING LIST (3 OF 4)

A11 PHASE LOCK		A12 REFERENCE		A13 FRAC N (ANLG)		A14 FRAC N (DIG)		A15 PRE-REGULATOR	A16 REAR PANEL	A18 DISPLAY	FOCUS/ INT	FAN SUPPLY	CHASSIS MISCELLANEOUS NOTES
J1	XA11J2	XA12J1	XA12J2	XA13J1	XA13J2	XA14J1	XA14J2	J3	J6	J4	J2	J5	
	43												
	19		19		19		19		2 13 9				
	23 53 24 54		23 53 24 54		23 53 24 54		23 53 24 54		17 18 19 20				
	25 55 26 56		25 55 26 56		25 55 26 56		25 55 26 56		21 22 23 24				
		23	32			5							
		54 58											
							31	7	30				NOT USED
2 1													NOT USED
6		2, 32 4, 34											
			36						39				

)URCE	MNEMONIC DESCRIPTION	A1/A2 FRONT PANEL	A3 SOURCE	A4 R SAMPLER/ MIXER	A5 A SAMPLER/ MIXER	A6 B SAMPLER/ MIXER	A7 PULSE GEN	A8 POST- REGULATOR		A9 CPU	
		J1	XA3J1	XA4J1	XA5J1	XA6J1	XA7J1	XA8J1	XA8J2	XA9J1	XA9J2
, 51	+22Vdc		14						21, 51	10, 40	
, 16, 45, 46	+15Vdc		19	7	7	7	7		15, 16 45, 46	15, 16 45, 46	
 34 , 56	+15Vdc DISPLAY (ALSO FRONT PANEL) +15Vdc PROBE POWER +15Vdc SOURCE	13 17, 18	 15, 16					29	 4, 34 8*, 26, 56		
, 40	UNREG +5VA								10, 40	21*, 51*	
, 54	+6Vdc PULSE GEN						3		24, 54		
, 50	+5Vdc MICROCIRCUIT		17	2	2	2			20, 50	11*, 41*	
	+5Vdc DIGITAL (CPU DISPLAY & FRONT PANEL)	23, 24						18, 19 48, 49			12, 13 42, 43
	+5Vdc DIGITAL (INSTRUMENT)		1					20, 21 50, 51			10, 11 40, 41
	+5Vdc SENSE (TO PRE-REGULATOR)										11
	GROUND ANALOG	19, 20	12, 13 32, 33	3, 5 10, 12	3, 5 10, 12	3, 5 10, 12	2, 4, 5, 6 8, 9, 11		MULTI- PINS	MULTI- PINS	
	GROUND DIGITAL		21					22, 23 52, 53			8, 9 38, 39
	+5Vdc DIGITAL GROUND SENSE										
		21, 22						24, 25 54, 55			6, 7 36, 37
), 48	-5.2Vdc		18				1		18, 48	13, 43	
36	-12.6Vdc PROBE POWER	15, 16							6, 36		
), 12, 41, 42	-15Vdc		20	1	1	1			11, 12 41, 42	19*, 20* 49*, 50*	

WER SUPPLIES CONNECTED DIRECTLY BETWEEN A8 TO A18.

+5VD CONNECTED TO A15.

CONNECTED TO +5VD ON A17.

, GNDDSENSE CONNECTED TOGETHER WITH SHIELD AND OUND ON A17.

D GNDD CONNECTED AT A15.

8753A MOTHERBOARD WIRING LIST (4 OF 4)

A11 PHASE LOCK		A12 REFERENCE		A13 FRAC N (ANLG)		A14 FRAC N (DIG)		A15 PRE-REGULATOR	A16 REAR PANEL	A18 DISPLAY	FOCUS/ INT	FAN SUPPLY	CHASSIS MISCELLANEOUS NOTES
J1	XA11J2	XA12J1	XA12J2	XA13J1	XA13J2	XA14J1	XA14J2	J3	J6	J4	J2	J5	
		9, 39		9, 39		9, 39			33				
6 6		15, 16 45, 46		15, 16 45, 46		15, 16 45, 46							
													NOTE 1 PROBE POWER
		30, 60		30, 60		30, 60							
1		11, 41											
								6					NOTE 1, 2
	10, 11 40, 41		10, 11 40, 41		10, 11 40, 41		10, 11 40, 41	4	3, 4				NOTE 2
								5					NOTE 3
- -		MULTI- PINS	MULTI- PINS	MULTI- PINS	MULTI- PINS	MULTI- PINS	MULTI- PINS	9, 10	17, 18 19, 20	3, 5	3, 5		NOTE 4 AUX IN COMMON
	7, 8, 9 37, 38 39		7, 8, 9 37, 38 39		7, 8, 9 37, 38 39		7, 8, 9 37, 38 39	2	5, 6 7, 8 28, 30	25, 26			NOTE 4
								3					NOTE 4
								1					NOTE 4 NOTE 5
3		13, 43		13, 43		13, 43							
													PROBE POWER
0 0		19, 20 49, 50		19, 20 49, 50		19, 20 49, 50							NOTE 1

URCE	MNEMONIC DESCRIPTION	A1/A2 FRONT PANEL	A3 SOURCE	A4 R SAMPLER/ MIXER	A5 A SAMPLER/ MIXER	A6 B SAMPLER/ MIXER	A7 PULSE GEN	A8 POST- REGULATOR		A9 CPU	
		J1	XA3J1	XA4J1	XA5J1	XA6J1	XA7J1	XA8J1	XA8J2	XA9J1	XA9J2
	ANALOG BUS (ABUS)		31								
1	ABUS ADDRESS 0 (LSB)		11								
1	ABUS ADDRESS 1		30								
2	ABUS ADDRESS 2 (MSB)		10								
2	ABUS ENABLE REFERENCE										
3	ABUS ENABLE SOURCE		29								
8	L=ABUS COUNTER GATE										
	AUXILIARY INPUT (FROM REAR PANEL)										
, 47	CMOS MEMORY CONTROL (SUPERCAP)							17, 47		44	
3	DIGITAL IF CONVERSION COMPLETE										33
	DIGITAL IF (SERIAL) CLOCK										4
	DIGITAL IF (SERIAL) DATA (OUT)										3
	DIGITAL IF DATA 0 (LSB)										27
	DIGITAL IF DATA 1										57
	DIGITAL IF DATA 2										28
	DIGITAL IF DATA 3										58
	DIGITAL IF DATA 4										29
	DIGITAL IF DATA 5										59
	DIGITAL IF DATA 6										30
	DIGITAL IF DATA 7 (MSB)										60
	DIGITAL IF ENABLE 0										34
	DIGITAL IF ENABLE 1										5
	DIGITAL IF ENABLE 2										35
	SOURCE SPUR CONTROL		22								
	DISPLAY DATA 0 (LSB)									30	
	DISPLAY DATA 1									60	
	DISPLAY DATA 2									29	
	DISPLAY DATA 3									59	
	DISPLAY DATA 4									28	
	DISPLAY DATA 5									58	
	DISPLAY DATA 6									27	
	DISPLAY DATA 7									57	
	DISPLAY DATA 8									26	
	DISPLAY DATA 9									56	
	DISPLAY DATA 10									25	
	DISPLAY DATA 11									55	
	DISPLAY DATA 12									24	
	DISPLAY DATA 13									54	
	DISPLAY DATA 14 (MSB)									23	
	DISPLAY DATA VALID									53	
	DISPLAY DISCONNECT SENSE									22	
	DISPLAY READY FOR DATA									52	

LAB PILOT?

8753A MOTHERBOARD WIRING LIST (1 OF 4)

A11 PHASE LOCK		A12 REFERENCE		A13 FRAC N (ANLG)		A14 FRAC N (DIG)		A15 PRE-REGULATOR	A16 REAR PANEL	A18 DISPLAY	FOCUS/ INT	FAN SUPPLY	CHASSIS MISCELLANEOUS NOTES
J1	XA11J2	XA12J1	XA12J2	XA13J1	XA13J2	XA14J1	XA14J2	J3	J6	J4	J2	J5	
0		10, 40 21 51 22		10, 40* 21* 51*		10, 40 21 51							
		52					48		32				AUX INPUT
	44									23 24 21 22 19			
										20 17 18 15 16			
										13 14 11 12 9			
										10 7 8			

Troubleshooting Reference

INTRODUCTION

This Troubleshooting Reference section is made up of several small sections that describe the internal tools used to test, adjust, and troubleshoot the HP 8753A system. Details on how to access them are described in each section. Procedures that use these tools are provided in other sections of this manual; this section only describes what they are and what they do. Also provided in this section is a table that lists the related service procedures, a listing of the error messages that could be displayed on the CRT, and a description of the front-panel error codes.

The information is this section is organized as follows:

- Table of Related Service Procedures
- Analog Bus
- Service Modes
- Tests, Test Options, Self Diagnose
- Peek/Poke
- Firmware Revision
- Error Term (Calibration Coefficient) Troubleshooting
- ROM/RAM Tests
- Front Panel Error Codes
- Error Messages

RELATED SERVICE PROCEDURES

INTRODUCTION

When a module is replaced in the HP 8753A, it may be necessary to perform additional service procedures to ensure that the new module is working properly and the instrument as a whole has maintained its current level of calibrated performance.

Depending on the module replaced, you may need to adjust variable hardware components and/or generate correction constants (data) to be stored in non-volatile memory. In all cases, you will need to perform some level of verification. The necessary procedures are listed in Table 1, Related Service Procedures, for each replacement module.

VERIFICATION PROCEDURES

Two distinct methods of testing are available to the user to verify performance following a repair:

- PERFORMANCE TESTS — The individual instrument specifications, listed in the General Information and Specifications section of the System Operating and Programming Manual, can be verified by performing the procedures found in the Performance Tests section of this manual. These procedures provide a rigorous exercise of the HP 8753A instrument level capabilities and, in some cases, are the only procedures which can verify that an out-of-tolerance type of failure has been fully remedied.
- SYSTEM VERIFICATION — System measurement uncertainty can be verified for an HP 8753A and a test set by performing the procedure found in the System Verification section of this manual. System verification does not measure the individual instrument performance specifications, but does determine whether or not an error-corrected system is providing accurate and traceable measurements. In general, this procedure requires less external equipment than performance tests.

For most repairs, Table 1 prescribes the relevant performance test procedures that verify the instrument level specifications affected by the replaced module. The system verification procedure is prescribed as an alternate procedure (where applicable) for any HP 8753A that is part of a system. Refer to the System Verification section for system definition.

If the replaced module does not affect a specified performance parameter of the instrument, nor affect the measurement capability of the system, execution of the self-test routine (preset self-test) is deemed sufficient to verify the repair.

ADJUSTMENTS AND CORRECTION CONSTANTS

Adjustment and correction constant routines must be performed in the order listed in Table 1. These procedures are found in the Adjustments and Correction Constants section of this manual.

Most HP 8753A replaceable modules rely on some digital correction stored in non-volatile memory on the A9 CPU board. If a new module utilizes or affects the value of correction data, that data will have to be regenerated.

Table 1. Related Service Procedures

Replaced Module	Verification, Adjustments, Correction Constants
A1 Front Panel	Verify: Self-Test
A2 Front Panel Interface	Adjust: Display Intensity and Focus CC Verify: Self-Test
A3 Source	Adjust: Analog Bus CC Source Pretune CC Source Spur Avoidance Tracking RF Output Power CC Cavity Oscillator Frequency CC Verify: Output Power Spectral Purity (harmonics and mixer spurs) or System Verification
A4/A5/A6 Samplers	Adjust: Sampler Diode Bias (replaced module only) Sampler Magnitude and Phase CC Verify: Minimum R Level (if R sampler replaced) Input Crosstalk Absolute Amplitude Accuracy Frequency Response Input Impedance (replaced module only) or System Verification
A7 Pulse Generator	Adjust: Sampler Magnitude and Phase CC Verify: Frequency Response Frequency Range and Accuracy Spectral Purity (phase noise) or System Verification
A8 Post-Regulator	Adjust: Source Spur Avoidance Tracking Cavity Oscillator Frequency CC Verify: Self-Test Check A8 test point voltages

Table 1. Related Service Procedures

Replaced Module	Verification, Adjustments, Correction Constants
A9 CPU	Adjust: Display Intensity and Focus CC Serial Number CC Option Number CC Analog Bus CC ADC Linearity CC Source Pretune CC Sampler Magnitude and Phase CC RF Output Power CC IF Amplifier CC Cavity Oscillator Frequency CC Verify: Output Power Absolute Amplitude Accuracy Frequency Response Dynamic Accuracy or System Verification
A10 Digital IF	Adjust: Analog Bus CC ADC Linearity CC Sampler Magnitude and Phase CC IF Amplifier CC Verify: Receiver Noise Level Trace Noise Input Crosstalk Absolute Amplitude Accuracy Dynamic Accuracy or System Verification
A11 Phase Lock	Adjust: Analog Bus CC Source Pretune CC Verify: Minimum R Level Frequency Accuracy or System Verification
A12 Reference	Adjust: High/Low Band Transition Frequency Accuracy Verify: Frequency Range and Accuracy

Table 1. Related Service Procedures

Replaced Module	Verification, Adjustments, Correction Constants
A13 Fractional-N (Analog)	Adjust: Fractional-N Spur and FM Sideband Verify: Spectral Purity (other spurious signals) Frequency Range and Accuracy
A14 Fractional-N (Digital)	Adjust: Fractional-N Frequency Range Verify: Frequency Range and Accuracy or System Verification
A15 Preregulator	Verify: Self-Test
A16 Rear Panel	Verify: Execute internal test #13, Rear Panel
A17 Motherboard	Verify: Self-Test
A18 Display	Adjust: Display Intensity and Focus CC Display Image Size, Position and Trace Alignment Verify: Observation

ANALOG BUS

INTRODUCTION

The HP 8753A has an analog bus built in that is useful for testing about 80% of the instrument's analog circuits. This bus is a single multiplexed line that networks a variety of nodes or "test points" throughout the instrument. It can be controlled from the front panel to examine up to 31 possible nodes, one at a time. With this analog bus, the instrument can make voltage and frequency measurements just like a voltmeter, oscilloscope, and frequency counter.

This section describes how to use the analog bus, as well as each node (how to set-up, what to look for, and any special conditions). Refer to the Overall Block Diagram, it shows where all the nodes are located in the instrument.

GENERAL INFORMATION

The following paragraphs provide general information about the structure and operation of the analog bus. Figure 1 illustrates the relationship between the analog bus, the assemblies, and the frequency counter.

The analog bus consists of a source section and a receiver section. The source could be any one of the 31 nodes from any of the assemblies shown in Figure 1, the A14 Fractional N VCO, or the A14 Fractional N VCO after its been divided down to 100 kHz.

The receiver portion is either the main ADC or the frequency counter. These are described below.

The ADC: The main ADC, located on the A10 assembly, makes the voltage measurements. It is useful for all but four of the 31 nodes.

Voltage measurements can be made in either low resolution mode (for measuring large signals) or high resolution mode (for measuring small signals). Different circuits are used for the two modes. This is discussed in more detail later in the Analog Bus Menu Descriptions.

NOTE: Waveforms to approximately 200 Hz can be reproduced.

The Frequency Counter: The frequency counter is located on the A14 assembly and can be used to count one of three sources: the selected analog bus node, the A14 Fractional N VCO (FRAC N), or the A14 Fractional N VCO after its been divided down to 100 kHz (DIV FRAC N). Its frequency range is 100 kHz to 16 MHz. The counts are triggered by the phase lock cycle; one each at pretune, acquire, track, and sweep for each bandswitch. (The service mode, SOURCE PLL, must be ON for the counter to be updated at each bandswitch).

The counter works in swept modes or in CW mode. However, in CW mode the **[MEAS RESTART]** softkey must be pressed to update the counter. The counter can be used in conjunction with SERVICE MODES for troubleshooting phase lock and source problems.

To read the counter over HP-IB, use the command OUTPCNTR.

NOTE: If the counter is turned on to analog bus nodes with no distinct AC signal to count, it will typically read about 0.750 MHz.

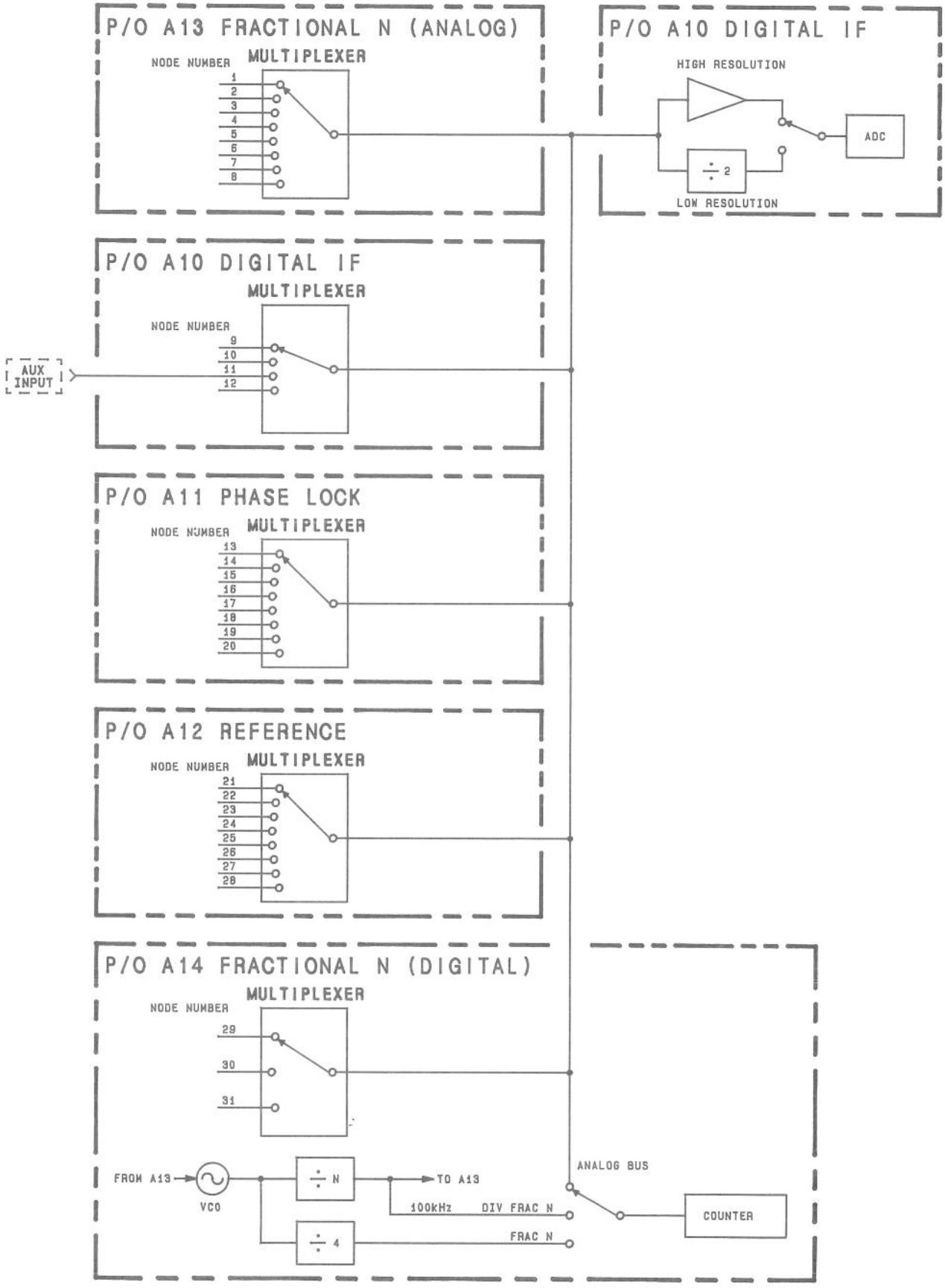


Figure 1. Simplified Diagram of the Analog Bus

HOW TO USE THE ANALOG BUS

To look at the bus nodes, the system must be phased locked. If a test set is not connected to the system, connect RF OUT to input R on the front panel. To prevent R channel power overload, make sure there is 26 dB of loss between the RF OUT and input R. NOTE: Test Sets have 19 dB of loss.

The ANALOG BUS menu can be accessed as follows:

1. Press **[PRESET]**.
2. Press **[SYSTEM] [SERVICE MENU] [ANALOG BUS ON].**
3. Press **[MEAS].**
4. If an s-parameter test set is connected, press **[ANALOG IN]**. If there is not an s-parameter test set, press **[S PARAMETERS]**, then **[ANALOG IN]**.
5. When the analog bus menu appears, the bus will be enabled, and the default node number will be displayed in the active entry area of the CRT.
6. Analog bus nodes must be viewed in the "real" format: Press **[FORMAT] [REAL]**.
7. Repeat steps 3 through 4. Any of the 31 nodes can then be accessed using the entry keys, the STEP keys, or the RPG.

The display and marker units (U) correspond to volts. Note that when displaying analog bus traces, the frequency is the x-axis. For a linear x-axis in time, switch to CW TIME mode (or sweep a single band), or for power, switch to POWER SWEEP.

NOTES:

- Do not use the analog bus with uncoupled source.
- Fast-moving waveforms may be sensitive to sweep time.
- Anything occurring during bandswitches is not visible.
- The analog bus input impedance is about 50K Ohms.

Analog Bus Menu Descriptions

[ANALOG BUS on off] (ANAB) enables the analog bus. This must be ON to access the analog bus menu under the **[MEAS]** key.

[RESOLUTION] allows you to measure both large and small signal levels. The circuits are different for measuring small and large voltage signal levels. For small signals (high res.) an amplifier is used; large signals (low res.) are attenuated. High resolution resolves very small voltage levels; in the order of microvolts. The range is ± 0.5 volts. Low resolution resolves voltage levels to the order of millivolts. The range is ± 10 volts.

[AUX OUT] allows you to look at the analog bus nodes on external equipment (oscilloscope, voltmeter, etc.). To do this, connect the equipment to the AUX INPUT BNC connector on the HP 8753A rear panel, and turn AUX OUT to ON. AUX OUT ON enables all nodes, except nodes 9 through 12, to be output on the AUX INPUT line. **NEVER input any signal on to the AUX INPUT rear panel connector with this function turned ON. Doing so can cause damage to the instrument.**

[COUNTER OFF] switches the counter off and removes the counter display from the CRT.

[ANALOG BUS] switches the counter to count the analog bus. Refer to Figure 1.

[FRAC N] switches the counter to count the A14 Fractional N VCO frequency. Note that this is not part of the analog bus.

[DIV FRAC N] switches the counter to count the A14 Fractional N VCO frequency after it has been divided down to 100 kHz for phase locking the VCO. Note that this is not part of the analog bus.

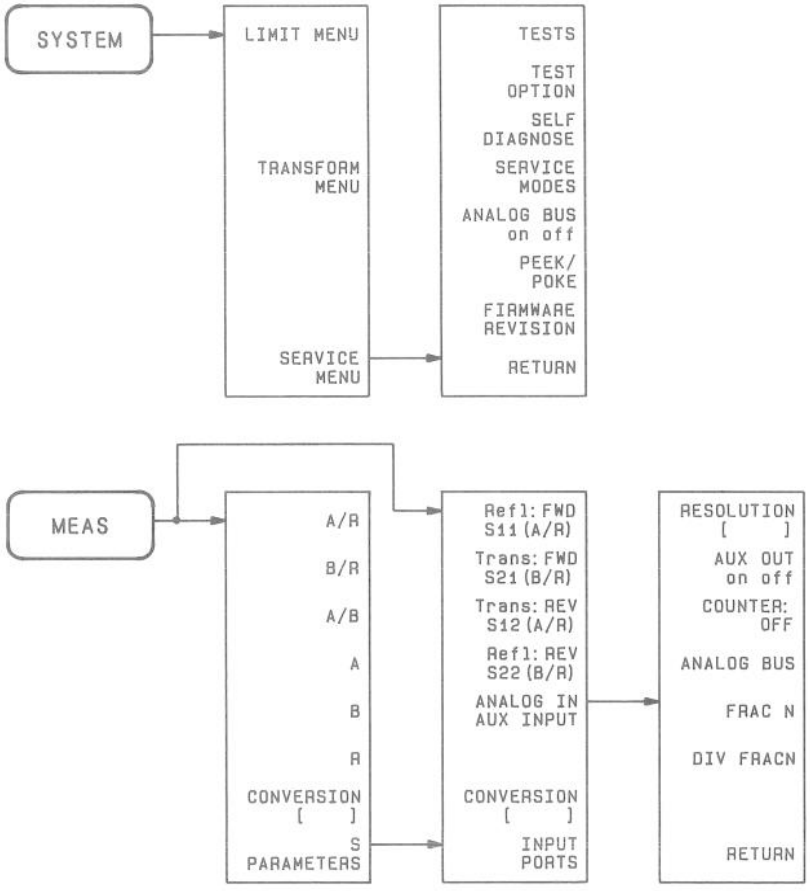


Figure 2. Analog Bus Menu

DESCRIPTION OF ANALOG BUS NODES

The following paragraphs describe the 31 analog bus nodes. They are listed in numerical order and are grouped by assembly. Refer to the Overall Block diagram for node locations.

To look at the bus nodes, the system must be phased locked. If a test set is not connected to the system, connect RF OUT to input R on the front panel. To prevent R channel power overload, make sure there is 26 dB of loss between the RF OUT and input R. NOTE: Test Sets have 19 dB of loss.

A3 Source

1 **LM In** (Level modulator input detector)

Resolution: Low
Scale: 500 mV/div
Reference value: −5 V
Set to Power Sweep (under STIMULUS **[MENU], [SWEEP TYPE MENU]**
Start: −10 dBm
Stop: +25 dBm
CW Freq: 3 GHz

This node detects the RF power from the cavity oscillator going into the Level Modulator. Setting the x-axis to the power sweep allows you to see the voltage proportional to the power out of the cavity oscillator on the y-axis. You should see a trace similar to the trace shown in Figure 3. The absolute voltage levels will vary slightly from instrument to instrument. Any flat lines that occur at the start or stop of the sweep indicate ALC saturation. Saturation points will also vary from instrument to instrument, however, saturation should never occur between −5 dBm and +20 dBm. If the cavity oscillator is not putting out any power, you will see a flat line across the sweep at about 0V.

Figure 3. Node 1 LM In, Level Modulator Input.

2 LM Out (Level modulator output detector)

Set to Power Sweep (under STIMULUS **[MENU]**, **[SWEEP TYPE MENU]**
Start: −10 dBm
Stop: +25 dBm
Scale: 500 mV/div
Reference Value: 0 V
CW Freq: 3 GHz

The node detects the RF power coming out of the Level Modulator. Setting the x-axis to power sweep allows you to see the voltage proportional to the power out of the level modulator on the y-axis. You should see a trace similar to the trace shown in Figure 4. Absolute voltage levels will vary from instrument to instrument. Any flat areas that occur at the start or stop of the sweep indicate ALC saturation. Saturation points will also vary from instrument to instrument, however, saturation should never occur between −5 dBm and +20 dBm. If the cavity oscillator is not putting out any power, you will see a flat line across the sweep at about 0V.

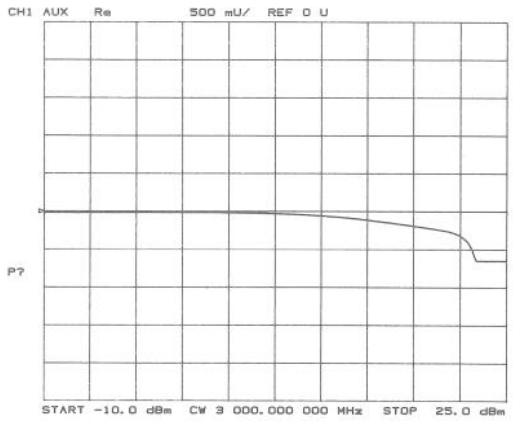


Figure 4. Node 2 LM Out, Level Modulator Output.

3 Amp In (Amplifier input detector)

Set to Power Sweep (under STIMULUS **[MENU]**, **[SWEEP TYPE MENU]**
Start: −10 dBm
Stop: +25 dBm
Scale: 500 mV/div
Reference Value: 0 V
CW Freq: 3 GHz

This node detects the power coming out of the mixer and going into the amplifier. Setting the x-axis to power sweep allows you to see the voltage proportional to the power out of the mixer on the y-axis. You should see a trace similar to the trace shown in Figure 5. Notice the trace is flat and is at 0V up to approximately 20 dBm (this varies with different instruments). This is because the power is so low up to that point that the analog bus detector does not respond.

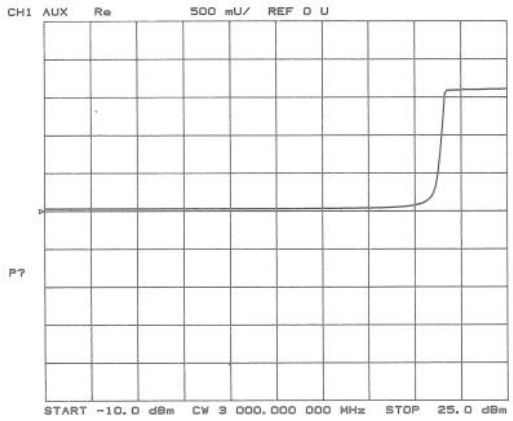


Figure 5. Node 3 Amp In, Amplifier Input.

4 Det (Detects RF OUT power level)

Set to Power Sweep (under STIMULUS **[MENU]**, **[SWEEP TYPE MENU]**
Start: −10 dBm
Stop: +25 dBm
Scale: 100 mV/div
Reference Value: 0 V
CW Freq: 3 GHz

This node detects the power that is coupled and detected from the RF OUT arm to the ALC loop. Setting the x-axis to power sweep allows you to see the voltage that is proportional to the coupled power on the y-axis. You should see a trace similar to the trace shown in Figure 6. Notice the voltage exponentially follows power level. This signal goes into a "logging" circuit that will produce a linear voltage ramp with respect to power.

Absolute voltage levels may vary from instrument to instrument. Any flat areas that occur at the start or stop of the sweep indicate ALC saturation. Saturation points will also vary from instrument to instrument, however, saturation should never occur between −5 dBm and +20 dBm.

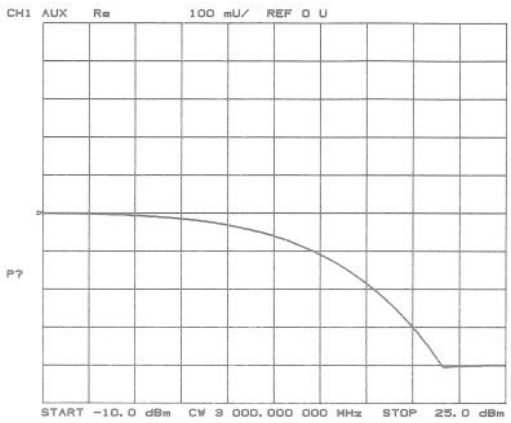


Figure 6. Node 4 Det, RF OUT Power Level Detector.

5 Temp (Temperature sensor)

Resolution: Low
Scale: 1 V/div

This node indicates the internal temperature of the HP 8753A, near the cavity oscillator. The sensitivity is 10 mV per degree Kelvin. The oscillator changes frequency slightly as it's temperature changes. This sensor indicates the temperature so that the frequency can be predicted, which is critical for the spur avoidance feature.

6 Integ (ALC leveling integrator output that drives the ALC leveling modulator)

Resolution: Low
Set to Power Sweep (under STIMULUS **[MENU]**, **[SWEEP TYPE MENU]**
Start: −10 dBm
Stop: +25 dBm
Scale: 1 V/div
Reference Value: 0 V
CW Freq: 3 GHz

This node displays the output of the summing circuit in the ALC loop. The summing circuit sums a reference linear voltage ramp with the coupled signal from the RF OUT path. In power sweep, you should see a voltage ramp as shown in Figure 7. Absolute voltage levels vary slightly from instrument to instrument. Any flat areas that occur at the start or stop of the sweep indicate ALC saturation. Saturation points will also vary from instrument to instrument, however, saturation should never occur between −5 dBm and +20 dBm.

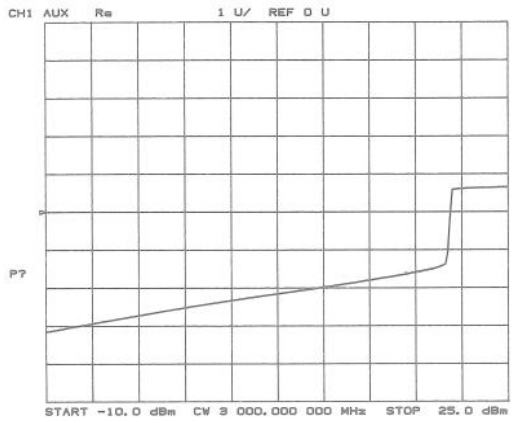


Figure 7. Node 6 Integ, ALC Leveling Integrator Output.

7 Log (Log amp output detector)

Resolution: Low
Set to Power Sweep (under STIMULUS **[MENU]**, **[SWEEP TYPE MENU]**
Start: −10 dBm
Stop: +25 dBm
Scale: 500 mV/div
Reference Value: 0 V
CW Freq: 3 GHz

This node displays the output of "logging" circuit in the ALC loop. Before this circuit, the coupled voltage signal from the RF OUT path has an exponential relationship to power (seen at node 4). After the logger circuit you should see a linear voltage ramp (if power is leveled across the sweep), as shown in Figure 8. This ramp is then compared with a reference linear voltage ramp (the output of the circuit can be seen at node 6). The correct waveform at this node shows that the circuits in the A3 Source ALC loop are functioning properly and the source is leveled (i.e. the level modulator is controlling the power level correctly).

Absolute voltage levels vary slightly from instrument to instrument. Any flat areas that occur at the start or stop of the sweep indicate ALC saturation. Saturation points will also vary from instrument to instrument, however, saturation should never occur between −5 dBm and +20 dBm.

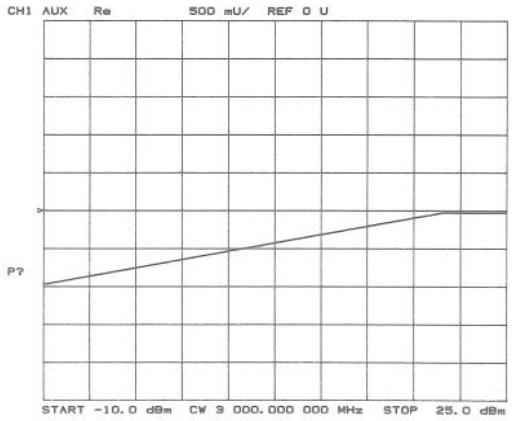


Figure 8. Node 7 Log, Log Amp Output.

8 **A3 Gnd** (Ground)

A10 Digital IF

9 **+0.37V** (+0.37V reference)

Resolution: High
Scale: 200mV/div
Reference Value: 0 V

Check for a flat line at approximately + 0.37V. This is used as the voltage reference in the "Analog Bus Resolution" adjustment procedure for calibrating out the analog bus high/low resolution gain and offset errors. The absolute voltage level is not critical, but it should be the same in high and low resolution.

10 **+2.50V** (+2.50V reference)

Resolution: Low
Scale: 10 mV/div

Check for a flat line at approximately +2.5V. This voltage is used in the "Analog Bus Resolution" adjustment procedure as a reference for calibrating the analog bus low resolution circuitry.

11 **Aux Input** (Rear panel input)

This selects the rear panel AUX INPUT to drive the analog bus for making voltage and frequency measurements. This can be used to look at test points within the instrument on the HP 8753A CRT (using the HP 8753A as an oscilloscope). Connecting the test point of interest to the AUX INPUT BNC connector on the HP 8753A rear panel. This feature can be useful if an oscilloscope is not available. Also, it can be used for testing voltage controlled devices by connecting the driving voltage of the DUT to the AUX IN connector. You can look at the driving voltage on one display channel, while displaying the DUT s-parameter response on the other display channel.

Also, with AUX OUT turned ON, you can look at analog bus nodes on external equipment (oscilloscope, voltmeter, etc.). See the Analog Bus Menu Descriptions for more information about this.

12 A10 Gnd (Ground reference)

Resolution: High
Counter: Off
Scale: 10mV/div

This is used in the "Analog Bus Resolution" adjustment procedure as a reference for calibrating the analog bus low and high resolution circuitry.

A11 Phase Lock

13 VCO Tune 2

Not used.

14 Vbb Ref (ECL reference voltage level)

Resolution: Low
Scale: 1 V/div
Reference Value: 0 V

The voltage level should be −1.29 V + 0.3V across the sweep. This voltage defines the midpoint of the ECL voltage swing. The instrument uses this as a reference to compensate for ECL voltage drift by comparing Vbb to the ECL voltages within the limiter/filter stages (nodes 18, 19, and 20).

15 Pretune (Open-loop pretune voltage for A3 source)

Resolution: Low
Scale: 500mV/div
Reference Value: 4.5 V
Start Freq: 300 kHz
Stop Freq: 3 GHz

This node displays the signal used to pretune the A3 source oscillator. The trace should be a stair-step ramp as shown in Figure 9. Each step corresponds to the beginning of each band, which is approximately equal to 1V/GHz. NOTE: The message, "CAUTION: POSSIBLE FALSE LOCK" will appear on the CRT; this is normal and can be ignored.

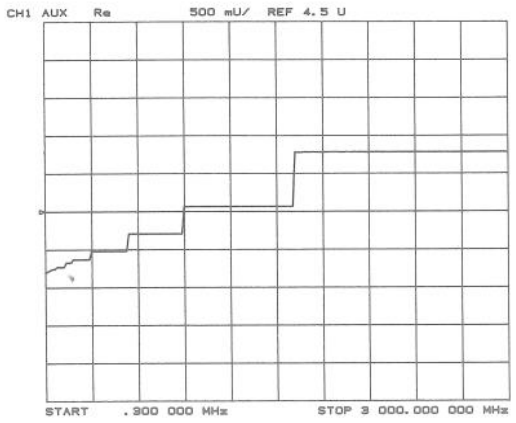


Figure 9. Node 15 Pretune, A3 source oscillator pretune voltage.

16 1V/GHz (A3 source oscillator tuning voltage)

Resolution: Low
Scale: 500mV/div
Reference Value: 5 V
Start Freq: 300 kHz
Stop Freq: 3 GHz

This node displays the tuning voltage ramp used to tune the A3 source oscillator. You should see a smooth linear voltage ramp, as shown in Figure 10. The beginning of the sweep should be at about +3.8V, and the end of sweep should be at about +6.8V. If this waveform is correct, you can be confident that the A11 Phase lock assembly, the A3 Source assembly, and the A13/A14 Fractional N assemblies are working properly and the instrument is phase locked. If you see anything other than a smooth linear ramp, any one of the assemblies in the source functional group could be the problem.

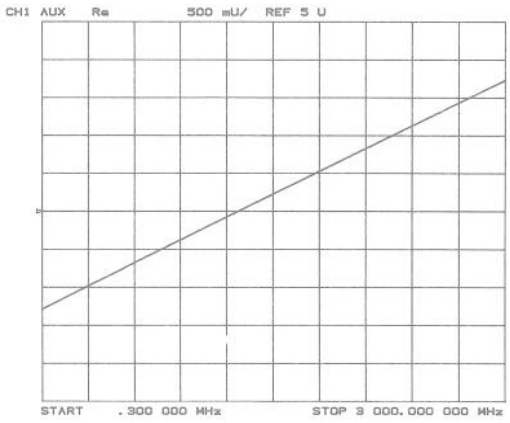


Figure 10. Node 16 1V/GHz, A3 Source Tuning Voltage.

17 1st IF (1st IF after limiting and filtering)

Counter: ON
Freq Type: CW Freq

This node counts the 1st IF frequency as it enters the A11 phase detector, after limiting and filtering. This signal comes from the R sampler output and is used to phase lock the system.

As CW frequencies from 300 kHz to 15.999 MHz are entered, you should see the counter track the entered frequency. As frequencies from 16 MHz to 3 GHz are entered, the counter should always read 1 MHz.

Because the counter is triggered by phase lock cycle, this node allows you to see what is happening between bands (phase locking occurs between bands). This node can be used with PLL DIAG service mode to count the IF at several steps during phase lock cycle.

18 IF Det 2N (IF on A11 Phase Lock after 3 MHz filter)

Resolution: Low
Scale: 200mV/div
Reference Value: −1.2 V
Stop Freq: 20 MHz

This node detects the presence of the IF within the 3 MHz low pass filter/limiter. This filter is used only during the track and sweep portion of the phase lock sequence. You should see a display like that shown in Figure 11. The low levels of the trace indicate the IF signal is in the passband of the filter; the high levels indicate the IF is out of the passband of the filter. The low levels should be at about −1.7V. This node can be used with the FRAC N TUNE and SRC TUNE service modes. These modes allows you to tune to a specific IF and check the for presence of the IF within the filter bandwidth. Using these modes also checks the A3 Source and A13/A14 Fractional N circuits.

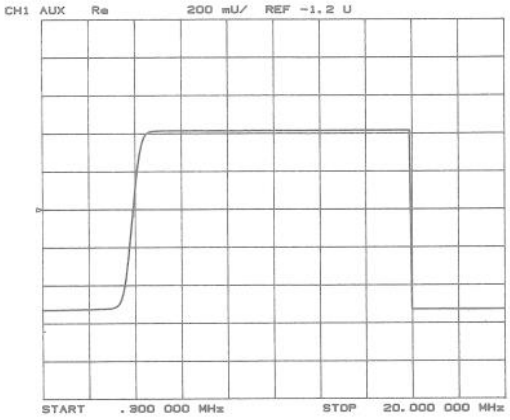


Figure 11. Node 18 IF Det 2N, IF Detector After 3 MHz Filter.

19 IF Det 2W (IF on A11 Phase Lock after 16 MHz filter)

Resolution: Low
Scale: 200 mV/div
Reference Value: −1.6 V
Stop Freq: 20 MHz

This node detects the presence of the IF after 16 MHz low pass filter/limiter. This filter is used during the pretune and acquire portion of the phase lock sequence. You should see a flat line at approximately −1.7V (ECL logic low), which indicates that the IF frequencies are in the passband of the filter. Higher voltage levels indicate that the IF is not within the passband of the filter, which is not normal. This node can be used with the FRAC N TUNE and SRC TUNE service modes. These modes allows you to tune to a specific IF and check the for presence of the IF within the filter bandwidth. Using these modes also checks the A3 Source and A13/A14 Fractional N circuits.

20 IF Det 1 (IF on A11 Phase Lock after 30 MHz filter)

Resolution: Low
Scale: 1 V/div
Reference Value: 0 V

This node detects the presence of IF power after the first 30 MHz filter/limiter. The filter should pass IF for all frequencies across the 300 kHz to 3 GHz sweep. The trace should be a flat line and at least 0.5V greater than Vbb (voltage at node 14). Any voltage levels less than this indicate that IF is not being detected at those frequencies.

A12 Reference

21 100 kHz (100 kHz reference frequency)

Counter: ON

This node counts the 100kHz reference signal from the A12 Reference assembly. The 100kHz is used on A13 Fractional N (Analog) assembly as a reference frequency for phase detector.

22 A12 Gnd 1 (Ground)

23 VCO Tune (A12 VCO tuning voltage)

Resolution: High
Scale: 50 mV/div
Reference Value: −50mV
Stop Freq: 20 MHz

This node displays the tuning voltage for the A12 VCO. The trace should show a step in voltage as shown in Figure 12. The step occurs at the frequency where lowband switches to high-band. The "VCO Adjustment Procedure" in the Adjustment section adjusts high-band/low-band voltages and the transition time. The lowband voltage level should be 0V + 1V. The high-band level should be 0.3V + 0.1V higher than lowband.

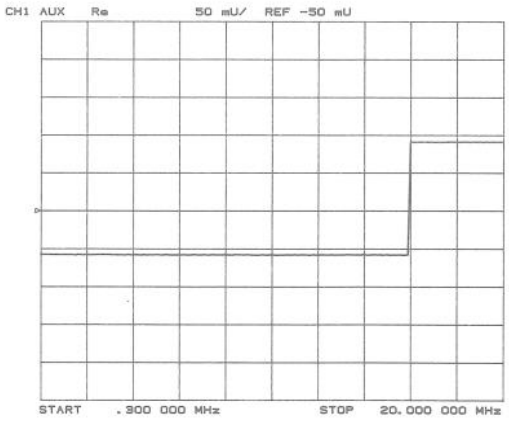


Figure 12. Node 23 VCO Tune, A12 VCO Tuning Voltage.

24 2nd LO

Counter: ON
Resolution: N/A
Scale: N/A
Sweep Type: CW Freq

This node counts 2nd LO used by the sampler/mixer assemblies to produce the 2nd IF of 4 kHz. In low band, the counter should indicate a frequency that is 4 kHz higher than the entered CW frequency. In high band, the counter should always read 996 kHz. NOTE: Check low band below 1 MHz only. Between 1 MHz and 16 MHz the counter is not accurate for this node.

25 PL Ref (Phase lock reference (300 kHz to 16.000 MHz))

Counter: ON
Resolution: N/A
Scale: N/A
Sweep Type: CW Freq

This node counts the reference signal used by the A11 Phase Lock phase detector. In low band, the counter frequency should be the same as the entered CW frequency. In high band, the counter should always read 1 MHz. NOTE: Check low band below 1 MHz only. Between 1 MHz and 16 MHz the counter is not accurate for this node.

26 Ext Ref (Rear panel external reference input)

Resolution: Low
Scale: 1 V/div
Reference Value: 0 V

This node is used to detect an external reference voltage. If an external reference voltage is used, the voltage level should be about −0.6V. If an external reference is not used, the voltage level should be about −0.87V.

27 VCXO Tune (40 MHz VCXO tuning voltage)

Resolution: Low
Scale: 1 V/div
Reference Value: 0 V

This node displays the voltage used to fine tune the A12 Reference VCXO to 40 MHz. You should see a flat line at some voltage level (the actual voltage level varies from instrument to instrument). Anything other than a flat line indicates that the VCXO is tuning to different frequencies. The VCXO can be adjusted to 40 MHz using the "Frequency Accuracy" adjustment procedure in the Adjustment section of this manual.

28 A12 Gnd 2 (Ground)

A14 Fractional N (Digital)

29 FN VCO Tun (A14 FN VCO tuning voltage)

Resolution: Low
Scale: 2 V/div
Reference Value: 2 V

This node displays the A14 FN VCO tuning voltage. This voltage comes from the A13 Fractional N (analog) assembly and is the return path for the Fractional N phase lock loop. If A13 and A14 assemblies are functioning properly and the VCO is phase locked, the trace should look like the trace shown in Figure 13. Any other waveform indicates that the FN VCO is not phase locked. The vertical lines in the trace indicate the band crossings.

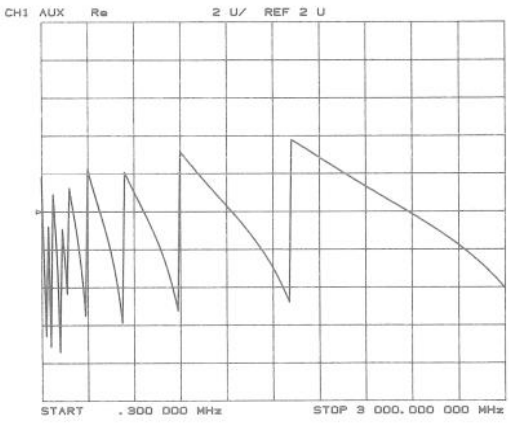


Figure 13. Node 29 FN VCO Tun, FN VCO Tuning Voltage.

30 FN VCO Det (A14 Fractional N VCO detector)

Resolution: High
Scale: 50mV/div
Reference Value: 0 V

This node is used to check that the A14 Fractional N VCO is oscillating. You should see a waveform like that shown in Figure 14. The trace is normally between 0 and −100mV.

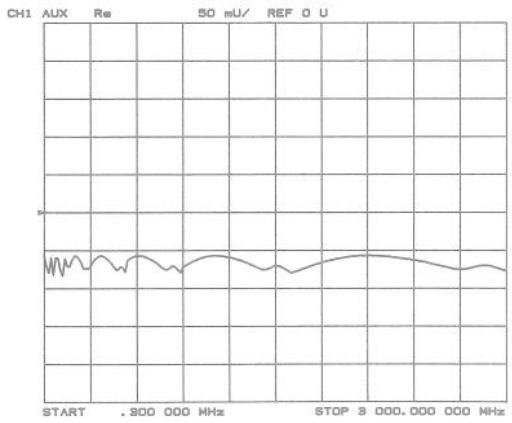


Figure 14. Node 30 FN VCO Det, A14 FN VCO Detector.

31 Count Gate (Analog bus counter gate)

Resolution: Low
Counter: Off
Scale: 1 V/div
Reference Value: 5 V

This node checks the analog bus counter gate signal. You should see a flat line at +5V. The counter gate activity occurs during bandswitches, and therefore is not visible on the analog bus. To view the bandswitch activity, look at this node on an oscilloscope, using AUX OUT ON (refer to Analog Bus Menu Descriptions).

SERVICE MODES

The **[SERVICE MODES]** softkey accesses a menu of softkeys that allow you to control and monitor various circuits in the HP 8753A for troubleshooting. These softkeys are described below.

To access the SERVICE MODES menu, press **[SYSTEM]**, **[SERVICE MENU]**, **[SERVICE MODES]** (see Figure 15).

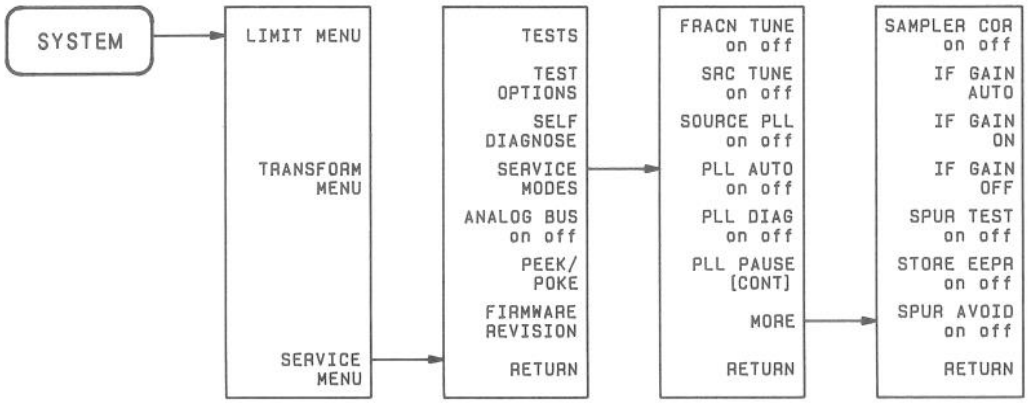


Figure 15. Service Modes Menu.

SERVICE MODE DESCRIPTIONS

[FRACN TUNE]. (SM1) This mode is useful for testing the A13 and A14 Fractional-N circuits. It allows you to directly control and monitor the output frequency of the fractional-N synthesizer (10 MHz to 60 MHz). Set the instrument to CW sweep mode, then turn FRACN TUNE ON.

The front-panel entry keys or the RPG can be used to enter the frequencies of interest. The output of the A14 assembly can be checked at A14J1 HI OUT (for high band) or A14J2 LO OUT (for lowband) with an oscilloscope, a frequency counter, or a spectrum analyzer. If using an oscilloscope or spectrum analyzer you will notice that the signal jumps and changes shape slightly at certain frequencies. This is due to the switching of the digital divider on the A14 board. The divider divides the frequency of the fundemental oscillator (which sweeps from 29.2 MHz to 60.8 MHz) by a factor of 2 or 3. When tuning down in frequency, a change will occur at 29.2 MHz and 15 MHz. When tuning up in frequency, a change will occur at 20 MHz and 30 MHz. The A13/A14 Fractional N circuits are phase-locked (synthesized) in this mode.

This mode can also be used in conjunction with SRC TUNE mode to test the A4, A5, and A6 samplers. The procedure to do this is described in the Source Functional Group Troubleshooting section.

[SRC TUNE]. (SM2) This mode is useful for testing the pretune functions of A11 Phase Lock board and the A3 Source board. It allows you to directly control the pretune frequency of the A3 source from 300 kHz to 3 GHz. The front-panel entry keys or the RPG can be used to enter the frequencies of interest. Set the instrument to CW sweep mode, then turn SRC TUNE ON. The frequency can be monitored at the front-panel RF OUT with an oscilloscope, a frequency counter, or a spectrum analyzer. Note that the source is typically pretuned 2 MHz to 4 MHz above the indicated (entered) frequency.

In this mode, the phase lock circuit is set to the pretune mode only, and does not attempt to phase lock. Since source is not phase locked, the residual FM increases significantly.

This mode can also be used in conjunction with FRACN TUNE mode to test the A4, A5, A6 samplers. The procedure to do this is described in the Source Functional Group Troubleshooting section.

[SOURCE PLL]. (SM3) This mode is useful for isolating a problem to either the receiver portion of the HP 8753A or the source. It allows you to disable the phase lock between the source and receiver. With this mode turned OFF, the source stays in the pretune mode and does not attempt to complete the phase lock sequence. Also, all phase lock error messages are disabled. The Fractional N circuits and the receiver operate normally.

With this mode OFF, you can check the receiver operation independent of the source. This can done by using an external synthesized source in place of the HP 8753A source. With the synthesizer external reference output connected to the HP 8753A EXT REF INPUT, and the RF output connected to HP 8753A R input, the receiver should operate and take data normally.

[PLL AUTO]. (SM4) During normal operation (PLL AUTO ON) when the instrument encounters phase lock problems (e.g. "harmonic skip"), it will automatically attempt to determine new pretune values. It will continue to do this until phase lock is achieved. This mode allows you to disable that function so that phase lock loop is not continuously trying to recalibrate itself. With PLL AUTO OFF the frequencies and voltages are not changing as they are when they are attempting to phase lock, so troubleshooting the phase lock loop circuits is more convenient.

[PLL DIAG]. (SM5) The instrument starts a new phase lock sequence at the beginning of each band (there are 11 bands). This normally occurs very rapidly, making it difficult to troubleshoot phase lock problems. Turning this mode ON slows the process down, allowing you to inspect the "steps" of the phase lock sequence (pretune, acquire, and track/sweep) by pausing at each step. The steps are indicated on the CRT, along with the channel (C1 or C2) and band number (B0 through B10).

This mode can be used with SWP PAUSE to halt the process at any step. It can also be used with the analog bus counter.

[PLL PAUSE]. This mode is used only with PLL DIAG mode. **[CONT]** indicates that it will continuously cycle through all steps of the phase lock sequence. **[PAUSE]** holds it at any step of interest. This mode is useful for troubleshooting phase lock loop problems.

[MORE]. This accesses the following modes.

[SAMPLR COR]. (SM6) This mode turns the sampler correction ON or OFF. Correction constants are used to improve the absolute power accuracy and phase tracking of the A4, A5, and A6 samplers. This mode can disable this feature so you can examine the uncorrected sampler responses. The sampler correction is ON during normal operation.

[IF GAIN AUTO]. The A10 assembly includes a switchable gain section that amplifies low-level 4 kHz IF signals (for A and B inputs only). This mode allows the A10 IF section to automatically determine if the IF gain amplifiers should be switched in or out. The switch occurs when the A or B input signal is at approximately −30 dBm. IF GAIN AUTO is the normal operating condition.

[IF GAIN ON]. This mode forces the A10 IF gain amplifiers to be switched in, regardless of the amplitude of the A or B IF signal. Be aware that input signal levels above −30 dBm will saturate the ADC and cause measurement errors. Turning this ON switches in both the A and B gain amplifier circuits; they cannot be switched independently. This mode is useful for checking the A10 IF gain amplifiers circuits.

[IF GAIN OFF]. This mode forces the A10 IF gain amplifiers to be switched out, regardless of the amplitude of the A or B IF signal. It is important to note that small input signals will appear noisy, and raise the apparent noise floor of the instrument. Turning this OFF switches both the A and B gain amplifier circuits; they cannot be switched independently. This mode is useful for checking the A10 IF gain amplifiers circuits.

[SPUR TEST]. (SM7) This mode requires the use of special equipment and software that is available only at the HP factory.

[STORE EEPR]. This mode allows you to store the correction constants that reside in non-volatile memory (EEPROM) onto a disc. Correction constants improve instrument performance by compensating for specific operating imperfections due to hardware limitations (refer to the "Adjustments and Correction Constants" section). Having this information on disc is useful as a back-up, in case the constants are lost (perhaps due to a CPU board failure). Without a disc back-up the correction constants can be reloaded manually, however the procedure is more time consuming.

[SPUR AVOID]. (SM8) During normal operation the HP 8753A can avoid the affects of unwanted mixing products (spurs) produced by the A3 Source. Although spurs are usually filtered out, at certain frequencies some spurs coincide with the desired frequency and are passed through the filter to the receiver. These spur frequencies are predictable and are avoided by offsetting (moving) the frequency of both the A3 source oscillator and the A3 cavity oscillator by the same amount. Doing this moves the desired frequency away from the spur, so that only the desired frequency passes through the filter.

Selecting SPUR AVOID OFF disables this feature, allowing all spurs to pass through. This can be useful for troubleshooting the A3 source assembly, since the oscillators are not being shifted around in frequency to avoid the spurs. This mode also allows you to examine the spurs.

TESTS, TEST OPTIONS, SELF DIAGNOSE

This following paragraphs describe the **[TEST]**, **[TEST OPTIONS]**, and **[SELF DIAGNOSE]** softkeys. These softkeys are accessed from the **[SYSTEM]** key as shown in figure 16.

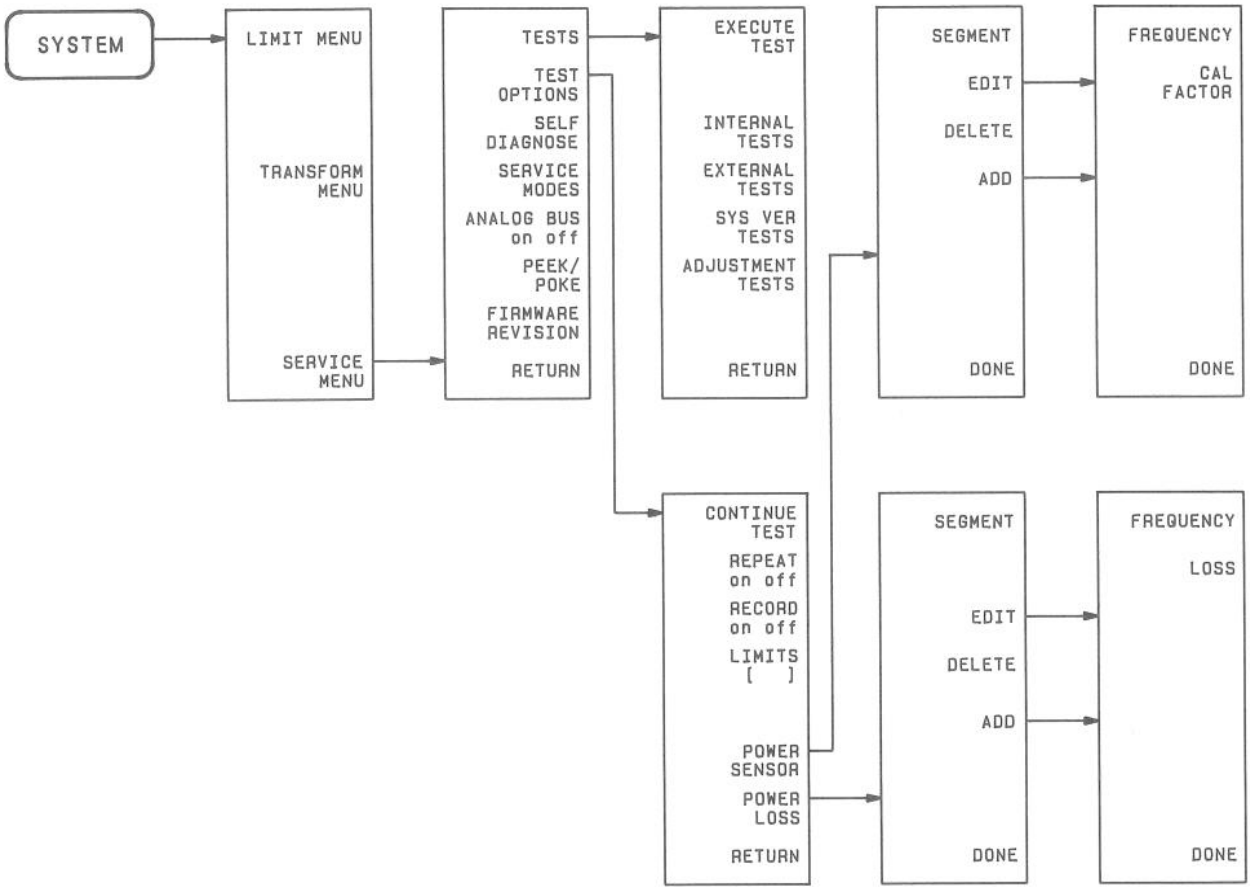


Figure 16. Tests, Test Options, Self Diagnose Menus.

TESTS

[TESTS] (TEST) softkey makes TEST the active function and accesses a menu that can be used to select or execute a test.

The tests that are divided into four categories (described below), depending on their function. Descriptions of each test in the category are under the heading "Test Descriptions" on the following pages. To access the first test in each category, press the category softkey. Use the step keys, the RPG, or the entry keys to access the other tests in that category. The test name, number and status of the last test executed is displayed in the active entry area of the CRT. The test status is coded as follows:

PASS (0) – PASS
FAIL (1) – FAIL
(NA) (3) – NOT AVAILABLE
-ND- (4) – NOT DONE
-IP- (2) – IN PROGRESS
DONE (5) – DONE

NOTE: The HP-IB command for each code is in parenthesis. The HP-IB command to output of any of these is OUTPTESS.

[EXECUTE TEST] (EXET) runs the selected test.

[INTERNAL TESTS] includes all self-tests that are completely internal and self-evaluating. These do not require external connections or user interaction.

[EXTERNAL TESTS] are additional self-tests that are also self-evaluating. However, these require some external connections (e.g. connect source to receiver) or user interaction (e.g. press keys).

[SYSTEM VER TESTS] includes tests for system verification procedure, as well as tests to examine the contests of measurement calibration arrays. The procedure is in the System Verification section. Information about the calibration arrays is under Calibration Coefficients (Error Term) Troubleshooting.

[ADJUSTMENT TESTS] are tests for generating and storing all correction constants. Refer to the Adjustments and Correction Constants section of this manual.

TEST OPTIONS

The **[TEST OPTIONS]** softkey accesses a menu of softkeys that can be uses to select options that affect the way tests (routines) run, or supply additional data tests may need. The softkeys are described below.

[CONTINUE TEST] (TESR1) continues the selected test from where it was stopped.

[REPEAT] (TO2) turns on or off the repeat function. If turned ON, the selected test will be run repeatedly, up to 10000 times. The total number of passes or fails are displayed in the active entry area. Press any key to stop repeating.

[RECORD] (TO1) turns on or off the record function. If on, the results of some tests are sent to a printer via HP-IB. This is especially useful for correction constants. Instrument must be in SYSTEM CONTROLLER mode or PASS CONTROL mode to print (under **[LOCAL]** key). Be sure to enter the new HP-IB address of printer if its not default address 1.

[LIMITS] selects either NORMal or SPECiaL limits for those tests that have "analog" pass or fail limit testing. With SPEC selected, tighter (special) limits can be chosen that are more difficult to pass; useful for a guard band.

[POWER SENSOR] is used to enter power sensor cal data for the adjustment tests requiring a power meter. Refer to the Adjustments and Correction Constants section.

This softkey accesses more menus (see Figure 16) for entering and editing the cal factor number for any frequency. For each frequency and corresponding cal factor that is added, a "segment" number is automatically assigned. The **[SEGMENT]** softkey allows you to view and edit any frequency and cal factor that has been entered, using the entry keys to enter the segment number desired. If the table is empty, it assumes 100% cal factor.

[POWER LOSS] is used in the Adjustments and Correction Constants section to enter external power losses due to external equipment connections. The intention varies from test to test.

This softkey accesses more menus (see Figure 16) for entering and editing the loss at any frequency. For each frequency and corresponding loss that is added, a "segment" number is automatically assigned. The **[SEGMENT]** softkey allows you to view and edit any frequency and loss that has been entered, using the entry keys to enter the segment number desired. If the table is empty, a default value is used. This value varies from test to test.

SELF DIAGNOSE

This routine examines the pass/fail status of all internal tests that have been run, and determines the assembly (assemblies) most probably causing the failure, with a confidence factor (0% to 100%). The routine uses the first failure, and assumes all previous tests (lower test number) have passed.

If no test have failed, "NO FAILURE FOUND" is displayed.

TESTS DESCRIPTIONS

The HP 8753A has many built-in test routines that test, verify, or adjust the instrument. This section describes each test available. Note: In several cases, additional details are found elsewhere in this manual.

Internal Tests

This group of tests run without external connections or operator interaction. All are "self-evaluating" – they return a PASS or FAIL condition.

0 ALL INT. Runs the following subset of internal tests: First, the RAM/ROM tests 2, 3, and 4. Then tests 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, and 20. If any of these tests fail, this test displays a FAIL status, and indicates the *first* test that failed. If *all* pass, the test displays a PASS status. Each test in the subset retains its own test status.

1 PRESET. Runs the following subset of internal tests: First, the RAM/ROM tests 2, 3, 4. Then tests 5, 6, 7, 8, 9, 10, 11, 14, 15, and 16. If any of these tests fail, this test returns a fail status, and indicates the *first* test that failed; if *all* pass, this test displays a PASS status. Each test in the subset retains its own test status. This set of tests is run at every power-up or **[PRESET]**. This same subset is available over HP-IB as "TST?".

2 ROM. Performed at power-on or **[PRESET]** as part of the ROM/RAM tests. Refer to "ROM/RAM" test section of this troubleshooting reference for more information about this test. This test cannot be run separately from this menu. If there is no FAIL message after preset or power-on, it is assumed that the test passed.

3 CMOS RAM. Verifies A9 CPU CMOS (long-term) memory with non-destructive write/read pattern (this does not erase data that is stored there). Also runs at power-up or **[PRESET]** as part of the ROM/RAM tests. If Fail message is not displayed, it assumed that the test passed. A destructive version (writes over data stored there) is available by moving jumpers on A9 CPU; see ROM/RAM tests section for more information.

4 Main DRAM. Verifies the A9 CPU main memory (DRAM) with non-destructive write/read test pattern (this does not erase data that is stored there). Also run at power-up or **[PRESET]** as part of ROM/RAM tests. If Fail message is not displayed, it assumed that the test passed. A destructive version (writes over data stored there) is also available by moving jumpers on A9 CPU; see ROM/RAM tests section for more information.

5 DSP Wr/Rd. Verifies ability of the main processor and Digital Signal Processor (DSP) to communicate with each other through DRAM, both on A9 CPU. Verifies that programs can be loaded to DSP. Verifies most of main RAM access circuits.

6 DSP RAM. Verifies the A9 CPU RAM associated with the Digital Signal Processor by using a write/read pattern.

7 DSP ALU. Verifies A9 CPU high-speed math processing portions of the Digital Signal Processor.

8 DSP Intrpt. Tests ability of the A9 CPU Digital Signal Processor to respond to interrupts from the the A10 Digital IF ADC.

9 **DIF Control.** Tests ability of A9 CPU main processor to write/read to control latches on the A10 Digital IF.

10 **DIF Counter.** Tests ability of the A9 CPU main processor to write/read to triple divider on A10 CPU. Primarily tests A9 CPU data buffers and A10 Digital IF, however, it also requires the 4 MHz clock from A12 Reference to pass.

11 **DSP Control.** Tests ability of the A9 CPU Digital Signal Processor to write to control latches on A10 Digital IF. Feedback is verified by the main processor. Primarily tests A10 Digital IF, but failures may be caused by A9 CPU.

12 **Fr Pan Wr/Rd.** Tests ability of A9 CPU main processor to write/read to front panel processor. Primarily tests the A2 Front Panel Interface and processor, with interrupts, but also requires A9 CPU data buffering and address decoding. (See also Tests 23 and 24 below.)

13 **Rear Panel.** Tests ability of A9 CPU main processor to write/read to rear panel control elements. Primarily tests the A16 Rear Panel, but also requires A9 CPU data buffering and address decoding. (Does *not* test HP-IB. Refer to the Introductory Operating Guide for sample programs to test HP-IB interface.)

14 **Post Reg.** Polls status register of A8 Post Reg, and flags the following conditions: heat sink too hot, inadequate air flow, shutdown on a post-regulated supply (not regulating, over-current, etc.), or shutdown on a probe supply.

15 **Frac N Cont.** Tests ability of the A9 CPU main processor to write/read to fractional N control element on A14 FN (Dig). The control element must be functioning, and the fractional N VCO must be oscillating (although not necessarily phase-locked).

16 **Sweep Trig.** Tests the sweep trigger (L SWP) line, from A14 Frac N Dig to A10 Digital IF, that synchronizes the receiver with the sweep.

17 **ADC Lin.** Tests linearity of the A10 Digital IF ADC using the built-in ramp generator. The test generates a histogram of the ADC linearity, where each data point represents the relative "width" of a particular ADC code. Ideally, all codes have the same width; different widths correspond to non-linearities. (See also Test 25.)

18 **ADC Ofs.** Tests the ability of the offset DAC on the A10 Digital IF to apply a bias offset to the IF signals before the ADC input. Primarily tests the A10 Digital IF. (See also Test 25.)

19 **ABUS Test.** Measures several analog bus reference voltages (all nodes from the A10 Digital IF) to test analog bus accuracy. Primarily tests the A10 Digital IF.

20 **FN Count.** Uses internal counter to test the A13/14 Fractional N. For both a low and high frequency, counts both the A14 fractional N VCO frequency (30 — 60 MHz) and and the divided fractional N frequency (100 kHz). Primarily tests the A13/14 Fractional N assemblies. Requires 100 kHz reference signal from A12 Reference to pass. Also requires counter gate signal from A10 Digital IF to operate counter.

External Tests

This group of tests require either external equipment and connections, or operator interaction of some kind to run. Tests 21 and 22 are used in the Operator's Check procedure, documented in the of the Operating and Programming Manual. Tests 23 and 24 are comprehensive front panel (keys, knob) checks (more complete than Test 12).

21 R&A Op Check. Tests RF OUT, R and A inputs, and phase lock system. Requires an external connection of 20 dB pad, power splitter, and cables. Tests in both ratio and absolute power modes. Refer to Operator's Check section in the Operating and Programming Manual.

22 R&B Op Check. Same as 21, but for R and B inputs.

23 Fr Pan Seq. Tests RPG and all front panel keys (A1), plus front panel microprocessor (A2). Prompts user to rotate RPG, then push each key, in an ordered sequence. Continues to next prompt only if current prompt is correctly satisfied.

24 Fr Pan Diag. Similar to 23 above, except that user rotates RPG or pushes keys in any order, and instrument displays the command it received.

25 ADC Hist. Tests the A10 Digital IF ADC linearity across a user-selectable range of ADC codes. When the test is executed, it prompts for the ADC starting code. The span of codes tested is determined by the current number of points. If averaging is desired, turn it on and select the number of averages. The resulting display is a ADC histogram, where the trace value represents the "width" of each ADC code. Non-linearities appears as deviations from a flat line.

26 Source Ex. Exercises DACs within the A3 Source. Must observe results with a scope.

Sys Ver Tests

This group of tests apply mainly to system-level, error-corrected verification and troubleshooting. Tests 27 – 31 are associated with the System Verification procedure, documented separately under System Verification. Tests 32 – 43 make it possible to examine the calibration coefficient arrays (error terms) resulting from a measurement calibration; refer to Error Term Troubleshooting for details.

27 Sys Ver Init. Recalls the initialization state for system verification from disc, in preparation for a measurement calibration. This must be done *before* 28, 29, 30, or 31 are performed.

28 Ver Dev 1. Recalls verification limits from disc for verification device #1 in all applicable S-parameters. Performs pass/fail limit testing of current measurement.

29 Ver Dev 2. Same as 28 above for device #2.

30 Ver Dev 3. Same as 28 above for device #3.

31 Ver Dev 4. Same as 28 above for device #4.

32-43 Cal Coef 1-12. Copies error term data from a measurement calibration array to display memory. A measurement calibration must be complete and CORRECTION must be on. Definition of calibration arrays depends on type of current calibration. After execution, memory is automatically displayed. Formatting, markers, and graphics dump function normally. Refer to Error Term Troubleshooting for details.

Adjustment Tests

This group of tests is used in the Adjustments and Correction Constants section of this manual.

44 ***Source Def.** Writes default correction constants for source power accuracy. To be used only if 47 below doesn't work, to allow some rudimentary power control.

45 ***Pretune Def.** Writes default correction constants for phase lock pretuning accuracy. To be used only if 48 below doesn't work, to allow some rudimentary phase lock ability.

46 **ABUS Cor.** Measures three fixed voltages on ABUS, and generates new correction constants for ABUS amplitude accuracy in both high resolution and low resolution modes.

47 **Source Cor.** Measures source output power accuracy, flatness, and linearity against an external power meter via HP-IB, and generates new correction constants to meet specifications.

48 **Pretune Cor.** Runs internal phase lock algorithm to determine correct pretune values for accuracy phase locking. Determines new correction constants for pretuning.

49 **Foc/Int Cor.** Stores current values of focus and intensity adjustment (under **[DISPLAY]**) for recall at power-on.

50 **Disp 2 Ex.** Writes the "secondary test pattern" to display for display adjustments. (Refer to HP 1349A/D manual for adjustment details.) This pattern is normally accessed by a jumper, but it is difficult to access in the HP 8753A. (Simply remove the A9 CPU to display the "primary test pattern".)

51 **IF Step Cor.** Measures the actual gain of switchable IF amplifiers (A and B only), located on A10 Digital IF, and determines correction constants for absolute amplitude accuracy. Provides smooth dynamic accuracy and absolute amplitude accuracy in the −30 dBm input power region.

52 **ADC Ofs Cor.** Measures the A9 CPU ADC linearity characteristics, using an internal ramp generator, and stores values for the optimal operating region. During measurement, the receiver adds an offset bias to the IF signals so they are centered in the optimal region. This improves low-level dynamic accuracy.

53 **Sampler Cor.** Measures absolute amplitude response of R sampler against an external power meter via HP-IB. Then compares A and B, magnitude and phase, against R. Determines correction constants for beginning and end of each band.

54 **Cav Osc Cor.** Not available.

55 **Serial Cor.** Stores the instrument's serial number.

56 **Option Cor.** Stores the instrument's option registration number (required for Option 010 only).

57 ***Cal Kit Def.** Loads the default calibration kit definitions (device model coefficients) into EEPROM.

PEEK/POKE

The **[PEEK/POKE]** softkey displays a menu that allows you to access different HP 8753A memory locations and either view or change the contents of that location. The softkey menu can be accessed from the **[SYSTEM]** and **[SERVICE MENU]** keys as shown in Figure 17.

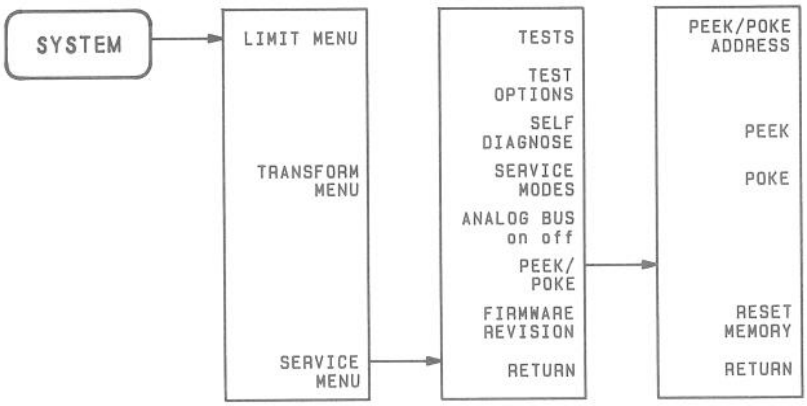


Figure 17. Peek/Poke Menu.

The **[PEEK/POKE]** softkey menu is described below:

[PEEK/POKE ADDRESS]. (PEEL) This softkey accesses and displays any memory address in the active entry area of the CRT. Use the RPG, entry keys, or step keys to enter the memory address of interest.

[PEEK]. (PEEK) This softkey displays the data that is at the memory address indicated by the **[PEEK/POKE ADDRESS]** softkey.

[POKE]. (POKE) This softkey allows you to change the data at the memory address indicated by the **[PEEK/POKE ADDRESS]** softkey. Use the RPG, entry keys, or step keys to change the data.

[RESET MEMORY]. This softkey allows you to reset or clear the memory where instrument states are stored. To do this, press **[RESET MEMORY]**, then **[PRESET]**.

[RETURN]. Returns you to the service menu.

FIRMWARE REVISION

The **[FIRMWARE REVISION]** softkey allows you to display the current firmware revision number. Press **[SYSTEM] [SERVICE MENU] [FIRMWARE REVISION]**, as shown in Figure 18 below. The firmware revision number and the date that it was implemented is displayed in the active entry area of the CRT.

Another way to display the firmware revision is to cycle the HP 8753A line power switch. The firmware revision number and the date that it was implemented will be displayed in the active entry area of the CRT.

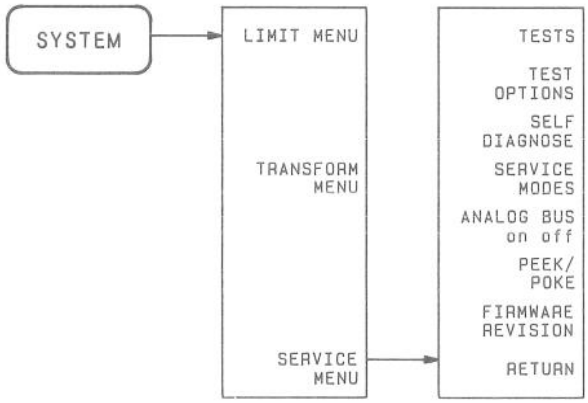


Figure 18. Accessing the Firmware Revision.

ERROR TERM (MEASUREMENT CALIBRATION COEFFICIENT) TROUBLESHOOTING

INTRODUCTION

Measurement calibration coefficients (also known as error terms or E-terms) are numbers generated and stored in internal arrays during a measurement calibration. After measurement calibration, these calibration coefficients are used for error correction (accuracy enhancement) when correction is turned on.

The arrays of E-terms are created by measuring well-defined calibration devices over a frequency range and comparing the measured data with the ideal model for the devices. The differences represent systematic (repeatable) errors due to the network analyzer system. The resulting calibration coefficients are good representations of the systematic error sources. For details on error correction, refer to Chapter 5 of the Operating and Programming Reference or System Specifications in the General Information section.

Using the procedure below, the calibration coefficients (E-terms) may be directly examined and copied. No external controller is required. This information can be useful in two ways:

- **Preventive Maintenance**: A stable, repeatable system should generate repeatable calibration coefficients over long time intervals – for example, six months. Make a hardcopy record (print or plot) of the E-terms, then periodically compare current E-terms with the record. A sudden shift in E-terms reflects a sudden shift in systematic errors, and may indicate the need for further troubleshooting. A long-term trend often reflects drift, connector and cable wear, or gradual degradation, indicating the need for further investigation and preventive maintenance, often simply cleaning connectors or inspecting cables. Note that the system may still conform to specifications.

- **Troubleshooting**: If a subtle failure or mild performance problem is suspected, the magnitude of the E-terms can be compared against specific limits. If the magnitude exceeds its limit, then the corresponding system component may be out of specification.

Consider the following while troubleshooting:

- All parts of the network analyzer system, including cables and calibration devices, can contribute to systematic errors and impact the E-terms.
- Connectors must be clean, gaged, and within specification for E-term analysis to be meaningful.
- Avoid unnecessary bending and flexing of the cables following the measurement calibration to minimize cable stability errors.
- Use good connection techniques during the measurement calibration. The connector interface *must* be repeatable.
- As a troubleshooting technique, this approach (E-term analysis) is usually best for minor, subtle performance problems. If a blatant failure or gross measurement error is evident, other approaches are faster and more direct.
- It is often worthwhile to perform the procedure twice (using two distinct measurement calibrations) to establish the degree of repeatability.

PROCEDURE

1. Set up the HP 8753A to the instrument state desired. Note that many of the instrument state parameters cannot be changed after a measurement calibration without turning correction off. The PRESET conditions are usually adequate.

2. Select the type of calibration to be performed: Press **[CAL] [CALIBRATE MENU]**. The number of calibration coefficient arrays and their meanings depend on the type of calibration performed (in some cases, they also depend on the measurement parameter selected before calibration.) Simple measurement calibrations are faster to perform, but provide less information. The full 2-port calibration takes more time, but separates systematic error sources into unique arrays. See Table 2 below.

Table 2. Calibration Arrays.

Array	Cal Type				Test Number
	Response	Resp & Isol'n[1]	1-port	2-port[2]	
1 2 3	E_R or E_T	E_X (E_D) E_T (E_R)	E_D E_S E_R	E_{DF} E_{SF} E_{RF}	32 33 34
4 5 6				E_{XF} E_{LF} E_{TF}	35 36 37
7 8 9				E_{DR} E_{SR} E_{RR}	38 39 40
10 11 12				E_{XR} E_{LR} E_{TR}	41 42 43

[1] Resp & Isol'n cal yields:
E_X and E_T if a transmission parameter (S_{21}, S_{12})
or
E_D and E_R if a reflection parameter (S_{11}, S_{22})

[2] One path, 2-port cal duplicates arrays 1 to 6 in arrays 7 to 12

NOTES:
- Meaning of first subscript: D=directivity, S=source match, R=reflection tracking, X=cross talk, L=load match, T=transmission tracking.
- Meaning of second subscript: F=forward, R=reverse.

3. Perform the measurement calibration desired. Refer to Chapter 5 of the Operating and Programming Reference manual for the procedure if you are not familiar with the steps involved.

4. Make sure correction is ON, then select the HOLD mode: Press **[MENU] [TRIGGER MENU] [HOLD]**.

5. Select the E-term of interest, and dump it to memory: Press **[SYSTEM] [SERVICE MENU] [TESTS] [test-number] [x1] [EXECUTE TEST]**. (Refer to Table 2 for corresponding test number.) The test copies the selected calibration coefficient array into display memory, then selects memory to display it on the CRT. If correction is turned off, or if the calibration coefficient selected does not exist for the current calibration, no array will be copied.

6. Examine the memory trace. Use the scale, reference, and marker functions to study the trace and determine its magnitude.

7. Compare to the E-term descriptions below and to the uncorrected typical specifications listed in the table of "Residuals after Accuracy Enhancement" in the General Information and Specifications section of the operating manual.

8. If desired, make a hardcopy record of the trace: Connect printer, then press **[COPY] [PRINT]**. Refer to Chapter 9 of the Operating and Programming Reference manual for more copying information.

9. When finished, press **[DISPLAY] [DISPLAY: DATA] [STIMULUS MENU] [TRIGGER MENU] [CONTINUOUS]**.

E-TERM DESCRIPTIONS

Following are descriptions of each E-term, its significance, typical results, and guidelines to interpretation. The same description applies to both the forward (f) and reverse (r) terms. The plots shown with each are *typical* of a working 7mm S-parameter system, after a 1-port or full 2-port calibration, in the PRESET state unless otherwise noted.

Directivity — Edf and Edr. These are the uncorrected forward and reverse directivity E-terms of the test set. Test port cables, if used, have a significant effect. These terms are characterized the load during the measurement calibration. The measurements most affected by directivity errors are low reflection measurements; high reflection measurements will appear normal. These E-terms are usually a direct indication of the test set bridge directivity, *if done without cables*. Refer to the test set specifications for the expected minimum directivity – typically below −30 dB. If the terms are marginally out of spec, inspect and gage connectors, then suspect a defective bridge. Gross errors may indicate a defective transfer switch in the test set.

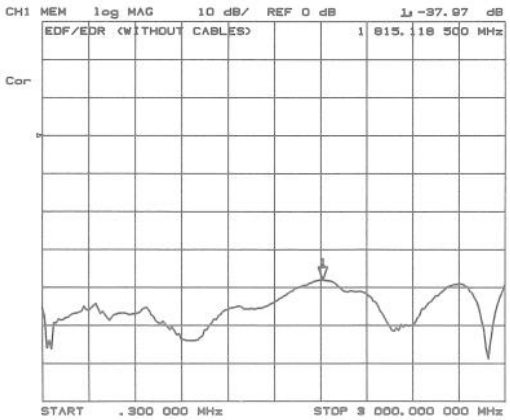


Figure 19a. Edf/Edr without Cables.

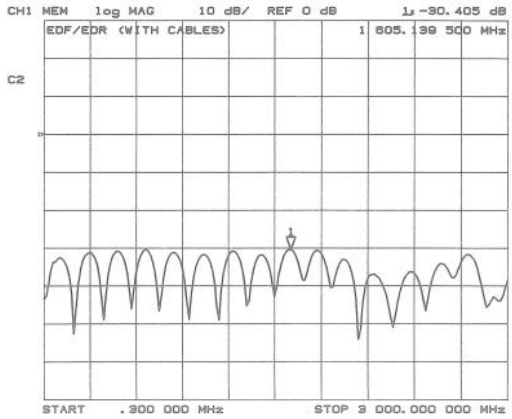


Figure 19b. Edf/Edr with Cables

Source Match — Esf and Esr. These are the forward and reverse uncorrected source match terms (the driven port). If a test port cable is used, its match is included. They are characterized by the open and the short calibration devices during the measurement calibration. The measurements most affected by source match errors are high reflection measurements and transmission measurements of highly reflective DUTs. The source match is a measure of the port match of the test set bridge and test port connector, and the test port extension cables if used. The test set power splitter, bias tees, and step attenuator may also contribute to source match errors. Poor source match combined with poor directivity is probably an indication of a defective bridge (or test port connector) in the test set. Poor source match alone may be caused by a mismatch in the test set, the test set port connector, the cable between the RF source and the test set, or the RF source itself.

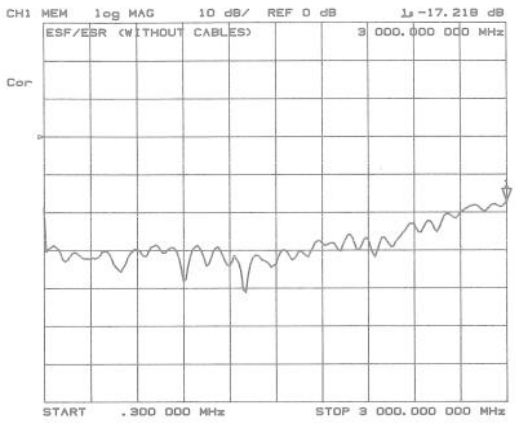


Figure 20a. Esf/Esr without Cables.

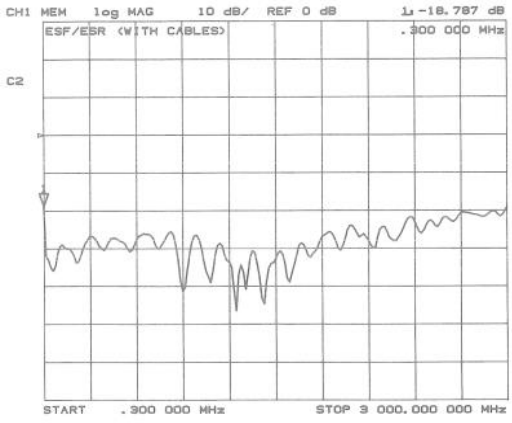


Figure 20b. Esf/Esr with Cables.

Reflection Tracking — Erf and Err. Tracking is the difference between the frequency response of the reference path (including R input) and the frequency response of the reflection test path (including A or B inputs). When using the HP 85046A/B test set, the A and B input used depends on the measurement direction (forward or reverse). If a test port cable is used, its response is also included. These E-terms are characterized by measuring the open and the short during the measurement calibration. All reflection measurements (high or low return loss) are affected by the reflection tracking errors. Large variations in the reflection tracking E-terms may indicate a problem in the reference or reflection signal path in the test set, or corresponding analyzer input. Note that sampler correction is turned off during calibration, so that discontinuities at the band edges (less than 0.5 dB) and overall roll-off (less than 3 dB) of the samplers are included in the E-terms.

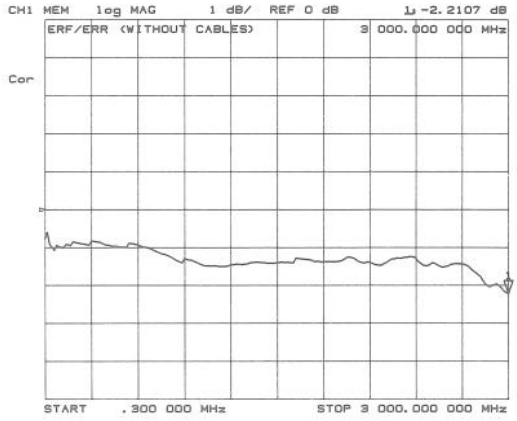


Figure 21a. Erf/Err without Cables.

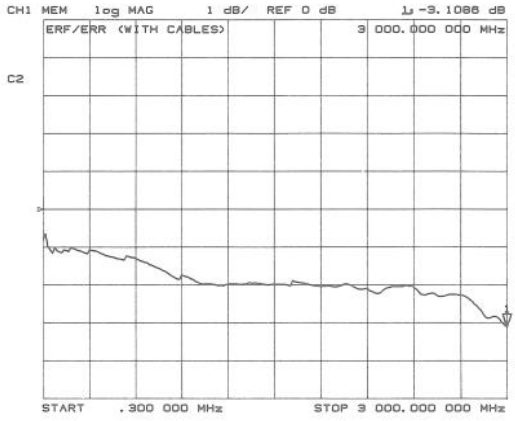


Figure 21b. Erf/Err with Cables.

Isolation (Crosstalk) — Exf and Exr. These are the uncorrected forward and reverse isolation error terms that represent the leakage between test ports and/or the R, A, and B inputs. The isolation error coefficients are characterized with loads attached to both ports during the measurement calibration. Isolation errors affect both reflection and transmission measurements, primarily where the measured signal is at a very low level; i.e. reflection measurements of a well-matched DUT or transmission measurements where the insertion loss of the DUT is large. The isolation E-terms correspond to the crosstalk specification of the HP 8753A (test set crosstalk is usually negligible) – typically below −90 dB with 0 dBm at the R input. Since these terms are low in magnitude, they are usually noisy (not very repeatable). The E-term magnitude changes dramatically with IF bandwidth: a 10 Hz IF bandwidth must be used in order to lower the noise floor beyond the crosstalk specification. Using averaging will also reduce the peak-to-peak noise in this E-term.

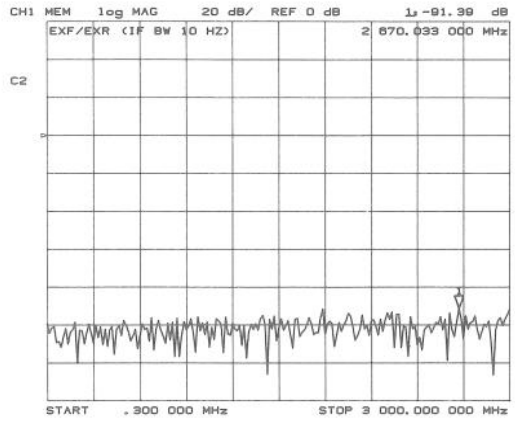


Figure 22a. Exf/Exr with 10 Hz Bandwidth.

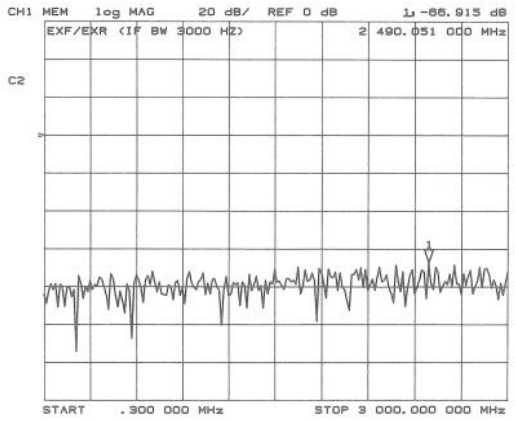


Figure 22b. Exf/Exr with 3 kHz Bandwidth.

Load Match — Elf and Elr. Load match is a measure of the impedance match of the test port that terminates the output of a 2-port device. If test port cables are used, their match is also included. Load match error terms are characterized by measuring the S11 (and S22 for s-parameter test sets) responses of a "thru" configuration during the calibration procedure. The measurements most affected by load match errors are all transmission measurements and reflection measurements of a low insertion loss two-port device (e.g. an airline). Large variations in the forward or reverse load match error terms may indicate a bad "thru" cable or a poor connection of the cable to the test port. In the case of single-bridge test sets, this is normally the B input.

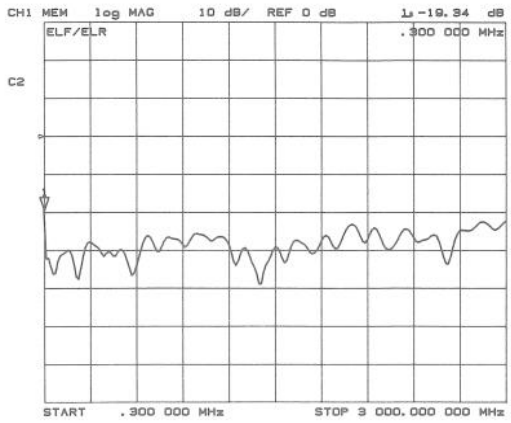


Figure 23. Elf/Elr.

Transmission Tracking – Etf and Etr. Tracking is the difference between the frequency response of the reference path (including R input) and the frequency response of the transmission test path (including A or B input) while measuring transmission. If test port cables are used, their response is also included. These terms are characterized by measuring transmission of the "thru" configuration during the measurement calibration. All transmission measurements are affected by transmission tracking errors. Large variations in the transmission tracking E-terms indicates a problem in the reference or transmission signal path in the test set, or corresponding analyzer input. Note that sampler correction is turned off during calibration, so that discontinuities at the band edges (less than 0.5 dB) and overall roll-off (less than 3 dB) of the samplers are included in the E-terms.

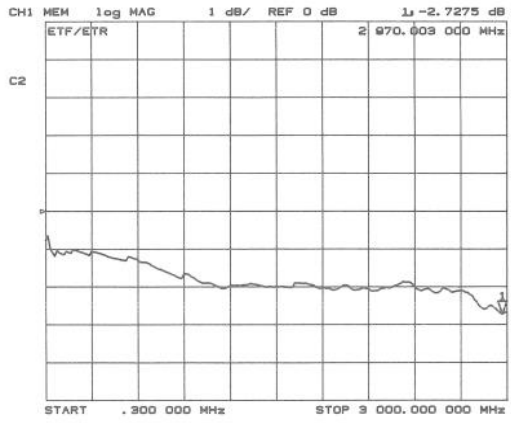


Figure 24. Etf/Etr.

ROM/RAM TESTS

After PRESET or power-on, a sequence of tests are automatically initiated to test the A9 microprocessor, ROM, and RAM. The test status is displayed on the four red LEDs located at the top left side of the A9 CPU assembly. The LEDs are labeled on the board from left to right: HALT-1-2-4.

When the system is operating normally, the HALT LED will light momentarily at preset or power-on, then turn off. The 1-2-4 LEDs will indicate which test is in progress. After the sequence of tests, the HALT LED will be off, the 1 and 4 LEDs will flash in synchronization with the sweep, and the number 2 LED will appear to be on constantly.

If a test fails, one or more of the LEDs will remain lit and the other LEDs will be off instead of flashing. The failed test can be determined by adding together the binary coded values of the lit LEDs. The sum of the values determine the test as follows:

LED Code Sum	Test	Message Displayed
1	Microprocessor	HP Logo
2	ROM1	ROM 1M or 1L FAIL
3	ROM2	ROM 2M or 2L FAIL
4	ROM3	ROM 3M or 3L FAIL
5	CMOS RAM (long term)	CM RAM FAIL m<**>[1]
6	Dynamic RAM (main)	D RAM FAIL m<**********>[1]

[1] m is MSB, l is LSB, * is P or F (for Pass or Fail).

If the **HALT** LED stays lit, the microprocessor has been HALTed and indicates a bad A9 CPU board. If the HALT LED does not come on momentarily at power-on, suspect a problem with A15 Preregulator, A8 Post-regulator, or A9 CPU. If the HALT LED does not come on momentarily at PRESET, suspect a problem with A1/A2 Front Panel assemblies or A9 CPU.

The microprocessor test displays the HP logo on the CRT. If this logo never appears, suspect a problem with the A9 CPU (typically the problem is the address or data lines, ROM address decoding, or ROM0).

If any of the ROM tests fail, the test repeats continually, and the appropriate LEDs light. Suspect the A9 CPU.

If any of the RAM tests fail, the test repeats continually, the appropriate LEDs light, and the current PASS/FAIL status (including which bits passed and failed of the last failure) is displayed on the CRT (if RAM failure has not affected the CRT display). Most probable cause of failure is the A9 CPU.

The tests can be forced to repeat endlessly by setting a jumper on the A9 CPU to one of the five possible positions. The test will loop and continuously update pass or fail information. The jumper positions do the following:

TOP	
* *	Allows you to write to EEPROM. This is used for the entering the correction constants in the Adjustments and Correction Constants section. In this position RAM and ROM tests are not performed.
* *	Loops CMOS RAM test. Destructive test — writes over information stored there.
* *	Loops Dynamic RAM test. Destructive test — writes over information stored there.
* *	Skips ROM and RAM testing.
= = =	Normal position. EEPROM is protected. ROM and non-destructive RAM tests are performed.
BOTTOM	

FRONT PANEL ERROR CODES

INTRODUCTION

This check allows the user to exercise the front panel microprocessor by isolating the front panel from the main microprocessor on the A9 CPU board assembly, and the instrument bus. A unique code is generated for each front panel key pressed by energizing the six amber LEDs located on the front panel. The A9 CPU board assembly may be removed without affecting this check.

PROCEDURE

To initiate the check, press **[PRESET]** and any other front panel key at the same time. Release the **[PRESET]** key first, and then the other key.

Each front panel key should be pressed, beginning with the top softkey (follow the sequence of keys listed in Table 3). As this is done, a code will be generated that is unique to each key. The code is displayed by energizing certain amber LEDs on the front panel (CH 1, CH 2, and R L T S). Refer to Table 3, which shows all front panel keys and their related codes. X denotes a lit LED.

To exit the check, press **[PRESET]**.

Table 3. Front Panel Error Codes Truth Table (1 of 2)

Front Panel Block	Key	CH1	CH2	R	L	T	S
Softkeys (top to bottom)	1			X	X	X	X
	2		X	X	X	X	X
	3				X	X	X
	4	X	X		X	X	X
	5			X			
	6		X		X	X	X
	7	X			X	X	X
	8	X			X		
Active Channel	CH1			X		X	X
	CH2			X	X		
Response	MEAS		X	X		X	X
	FORMAT		X	X	X		
	SCALE REF		X	X			
	DISPLAY					X	X
	AVG				X		
	CAL						
	MKR	X	X			X	X
	MKR FCTN	X	X		X		
Stimulus	MENU		X			X	X
	START		X		X		
	STOP		X				
	CENTER	X				X	X
	SPAN	X					

Table 3. Front Panel Error Codes Truth Table (2 of 2)

Front Panel Block	Key	CH1	CH2	R	L	T	S
Entry	▼	X					X
	▲	X			X		X
	ENTRY OFF	X				X	
	BACK SP	X	X				
	7			X	X	X	
	8			X	X		X
	9			X			X
	G/n			X		X	
	4		X	X	X	X	
	5		X	X	X		X
	6		X	X			X
	M/u		X	X		X	
	1				X	X	
	2				X		X
	3						X
	k/m					X	
	0	X	X		X	X	
	.	X	X		X		X
	-	X	X				X
	x1	X	X			X	
Instrument State	SYSTEM		X		X	X	
	COPY		X		X		X
	SAVE		X				X
	RECALL		X			X	
	LOCAL	X			X	X	

ERROR MESSAGES

INTRODUCTION

This section lists the possible service-related error messages displayed on the HP 8753A CRT or transmitted by the instrument over HP-IB. Each error message is printed in a bold type style, accompanied by a note that attempts to clarify the message and/or help fix the problem.

ERROR MESSAGES

When displayed, all error messages are preceded with the word **CAUTION:**. That part of the error message has been left off. The list appears in alphabetical order.

AIR FLOW RESTRICTED: CHECK FAN FILTER
An inadequate air flow condition has been detected. Clean fan filter. For most efficient cooling, the instrument covers should be in place. If problem persists, troubleshoot power supplies.

NO IF FOUND: CHECK R INPUT LEVEL
The first IF was not detected during the pretune stage. Ensure that the R input is connected with at least −35 dBm input power to R.

NO PHASE LOCK: CHECK R INPUT LEVEL
The first IF was detected at the pretune stage but phaselock could not be acquired thereafter. Refer to the system level troubleshooting in the service manual.

OVERLOAD ON INPUT R, POWER REDUCED
OVERLOAD ON INPUT A, POWER REDUCED
OVERLOAD ON INPUT B, POWER REDUCED
Whenever the power level at one of the three receiver inputs exceeds approximately +2 dBm, the RF OUT power level is reduced to the minimum possible level. A **P↓** appears in the left margin of the display to indicate that the power trip function has been activated. To remedy this condition, decrease the power level at the input below 0 dBm. Then turn the power trip off; refer to **[POWER TRIP on off]** key, chapter 3.

PHASE LOCK LOST
Phase-lock was acquired but then lost. Refer to the Troubleshooting reference section of the Service Manual and execute the phase lock diagnostic routine. See Service Modes.

PHASE LOCK CAL FAILED
An internal phase lock calibration routine is automatically executed at power-on, when a drift in pretune values has been detected, and anytime a phase lock problem is detected (loss of lock). This message indicates that phase lock calibration was initiated and the first IF detected, but a problem prevented the calibration from completing successfully. Refer to the Troubleshooting Reference section of the service manual and execute test 48, Pretune Correction.

POSSIBLE FALSE LOCK
The instrument is achieving phase lock but possibly on the wrong comb tooth. Refer to the Adjustments and Correction Constants section of the Service Manual and execute pretune correction.

POW MET INVALID
The power meter indicates an out-of-range condition. Check the test set up.

POW MET NOT SETTLED
Sequential power meter readings are not consistent. Verify that equipment is set up correctly. If so, preset the instrument and restart the routine.

POW MET NOT FOUND
Power meter does not respond over HP-IB. Check line power and HP-IB connections to the power meter. Verify that the power meter address and model number set in the HP 8753A matches the address and model number of the actual power meter.

POWER SUPPLY HOT!
The temperature sensors on the A8 Post Regulator assembly have detected an over-temperature condition. Note, the power supplies regulated on that assembly have been shut down.

POWER SUPPLY SHUT DOWN!
One or more supplies on the A8 Post Regulator assembly have been shut down due to one of the following conditions: over-current, over-voltage, or under-voltage.

PROBE POWER SHUT DOWN!
The biasing supplies to the probe are shut down due to exessive current draw. Troubleshoot probe.

SELF TEST #n FAILED
Internal test #n has failed. There are many internal test routines. The HP 8753A reports the first failure detected. Refer to the Troubleshooting Reference section of the Service Manual for more information on internal tests and the self-diagnose feature.

SWEEP TIME TOO FAST
The fractional-N and the digital IF circuits have lost synchronization. Refer to the System Troubleshooting section in the Service Manual for more information.

TROUBLE! CHECK SET-UP AND START OVER
Refer to the Adjustments and Corrections Constants section of the Service Manual for the appropriate equipment set up for this routine.