Recent Progress and Challenges for Relay Logic Switch Technology

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Abstract

The energy efficiency of CMOS technology is fundamentally limited by transistor off-state leakage (I_{OFF}). Mechanical switches have zero I_{OFF} and therefore could be advantageous for ultra-low-power digital logic applications. This paper discusses recent advancements in relay logic switch technology and current challenges which must be addressed to realize its promise.

Introduction

Supply voltage (V_{dd}) scaling has not kept pace with transistor scaling in recent generations of CMOS technology [1], so that chip power density has grown and now severely constrains IC design [2]. By improving system throughput despite reduced per-core performance, parallelism has thus emerged as the principal means to facilitate reductions in V_{dd} and hence increased transistor density. However, because the total energy consumed per digital operation reaches a minimum when transistors operate in the sub-threshold regime [3], this approach will become ineffective when V_{dd} is reduced below the transistor threshold voltage (V_T). Nano-electro-mechanical (NEM) relay technology has been proposed to overcome this energy-efficiency limit of CMOS technology [4]. Since mechanical switches have zero sub-threshold leakage current, there is no trade-off between decreasing active energy and increasing leakage energy with V_{dd} scaling; this in principle allows V_{dd} to be reduced to be nearly 0 V. This paper highlights recent progress and remaining challenges for realizing the promise of NEM relay technology for ultra-low-power digital logic applications.

Recent Progress

A. Relay Scaling

The pull-in voltage at which an electrostatically actuated relay turns on is dependent on several design parameters:

$$V_{PI} \propto \sqrt{\frac{EH^3Wg^3}{\varepsilon_0 L^3 A}} \quad (1)$$

where E and H are the Young's modulus and thickness of the structural film, respectively, g is the as-fabricated actuation gap thickness, ε_0 is the permittivity of air, A is the actuation area, and L and W are respectively the length and width of the suspension beam(s) [5]. From Eqn. (1) it can be seen that maintaining low voltage operation requires the thickness of the structural film to be scaled down together with the lateral dimensions of the relay. If there is a strain gradient within the film (leading to a bending moment M [6]), this can result in greater out-of-plane deflection (Δz) which may increase g:

$$\Delta z \propto \frac{ML^2}{EWH^3} \quad (2)$$

Positive strain gradient within a thin structural layer can be compensated by adding a thin, tensile bottom layer. Relays with scaled dimensions using such a bi-layer structural film recently were demonstrated using this approach (Fig. 1) [7].

B. Multi-Input/Multi-Output Relay Designs [8,9]

Since the mechanical (switching) delay of a relay is orders of magnitude larger than its electrical (capacitive charging) delay, a complex logic function is optimally implemented with relays as a single gate comprising minimum-size devices [4]. This often results in significantly reduced device count, especially since the input and output signal paths of a relay are isolated so that it can pass both low and high logic levels and so that the body can be connected to a logic signal. In this circuit design style, both the true and complement versions of logic terms are often computed to avoid incurring an extra mechanical delay for inversion. By incorporating two pairs of source and drain electrodes into each gated structure (Fig. 1), the device count and hence the area required to implement a complex logic gate can be reduced by up to a factor of two. Figs. 2 and 3 show how a two-relay circuit can generate complementary output signals when one source is tied to V_{dd} while the other source is tied to GND for each relay. By partitioning the gate electrode (Fig. 4), a single device can be driven by multiple input signals for even more compact circuit implementation (Fig. 5). The reference (body) electrode bias voltages can be dynamically changed to reconfigure the circuit function (Figs. 6 and 7).

Current Challenges

A. Contact Resistance

For digital logic applications, the ON-state resistance (R_{ON}) of a relay can be as high as ~10 kΩ without significantly affecting circuit performance [4]. This allows for the use of a refractory contacting electrode material such as tungsten (W), which is beneficial for improved resistance to wear and microwelding [10]. However, W is highly susceptible to oxidation, causing R_{ON} to increase undesirably over the device's operating lifetime (Fig. 8) [10], [11]. To address this issue, a wafer-level hermetic encapsulation process or an alternative contact electrode material that is more robust against oxidation is needed.

B. Surface Adhesion Force

The minimum energy required to operate a relay is set by the total surface adhesion force (F_A) between the contacting electrode surfaces of the relay in the ON state [12]. This is because the spring restoring force (F_{spring}) of the suspension beam(s) must be greater than F_A to ensure that the relay turns off when the applied voltage is 0 V. The greater F_A is, the greater F_{spring} must be, and hence the larger V_{dd} and/or the actuation area (*i.e.*, gate capacitance) must be to ensure that the electrostatic actuation force is sufficient to turn on the relay. Therefore, to ensure low-voltage operation of compact relays, F_A should be minimized (*e.g.* by using low-adhesion electrode materials or coatings and by minimizing contact area) while meeting the R_{ON} limit.

Conclusion

Since they have zero off-state leakage and can incorporate multiple input and output electrodes, relays potentially can achieve lower energy per operation and greater functionality per device for digital logic applications. Practical (but not insurmountable) challenges that remain to be solved are contact surface oxidation, minimization of surface adhesion force within R_{ON} limits, and development of ultra-thin structural films with very low strain gradient.

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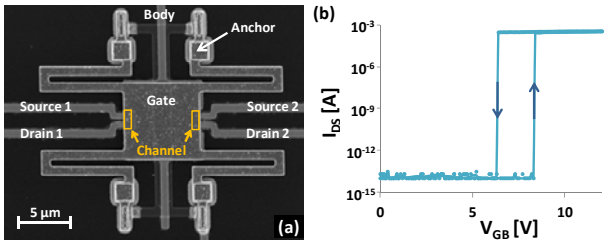

Figure 1: 6-Terminal (6-T) relay (movable Gate electrode, fixed Body and 2×[Source+Drain] electrodes) with scaled lateral dimensions (actuation area: 7.5×7.5 µm^2) and structural layer thickness (200nm LPCVD poly-$Si_{0.4}Ge_{0.6}$ / 10nm ALD tensile TiN): (a) plan-view SEM image with channel regions highlighted, (b) measured I_{DS}-V_{GB} characteristics.

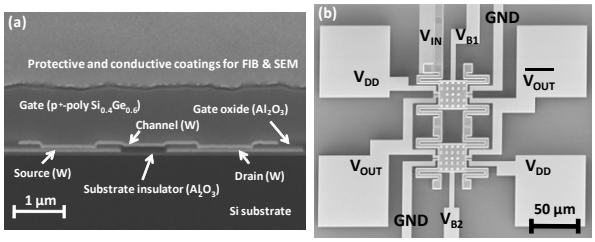

Figure 2: (a) Cross-sectional SEM image showing one of the channel regions of a 6-T relay (with larger dimensions than the device in Fig. 1 and a thick poly-$Si_{0.4}Ge_{0.6}$ structural layer). (b) Plan-view SEM image of a complementary Inverter/Buffer relay circuit comprising two 6-T relays (**Fig. 3**).

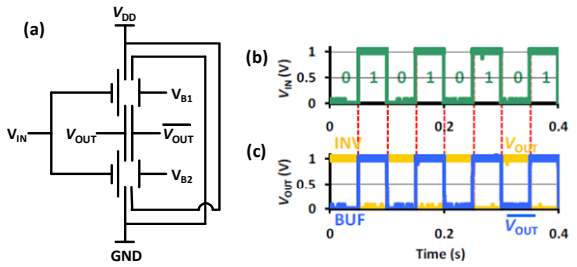

Figure 3: Simple relay logic circuit employing two 6-T relays to generate complementary output signals: (a) circuit schematic, (b) input signal, and (c) corresponding measured output signals. V_{DD} = 1V, V_{B1} = 13V and V_{B2} = -12V.

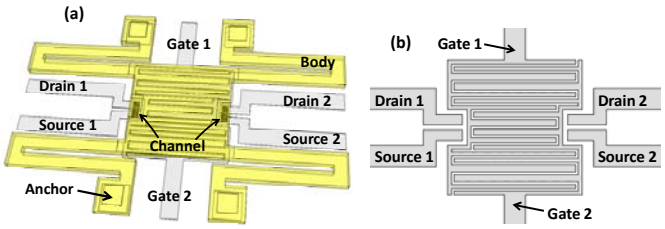

Figure 4: (a) Schematic isometric view of a dual-Gate, dual-Source/Drain relay. Note that the fixed actuation electrode is partitioned into two Gate electrodes and the movable electrode serves as the reference (Body) electrode. (b) Plan-view schematic showing the interdigitated electrode design to ensure that the gates have equal weight. Strain gradient within the structural layer can cause the movable electrode to warp (cf. Eqn. 2), so that the actuation gap is non-uniform from the center to the sides.

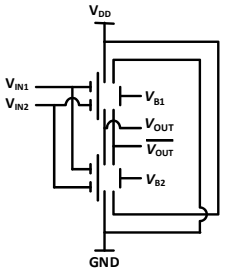

Figure 5: Dynamically configurable complementary relay logic circuit utilizing two dual-Gate, dual-Source/Drain relays.

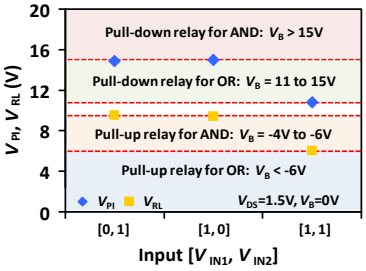

Figure 6: Measured pull-in (V_{PI}) and release (V_{RL}) voltages of a dual-Gate relay, for various input combinations. "1"≡V_G. Note that [1,0] and [0,1] are equivalent input combinations thanks to the interdigitated Gate design (**Fig. 4**).

(a) Bias	AND [V_{OUT}] / NAND [$\overline{V_{OUT}}$]	OR [V_{OUT}] / NOR [$\overline{V_{OUT}}$]
V_{DD}	8V	8V
V_{B2}	15V	12V
V_{B1}	-4V	-6V

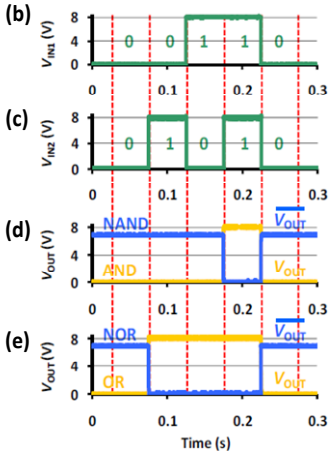

Figure 7: Operation of the circuit design shown in **Fig. 5**: (a) body bias voltages, derived from the data in **Fig. 6**, for AND/NAND and OR/NOR operation, (b,c) input voltage signals, (d,e) corresponding measured output voltage signals.

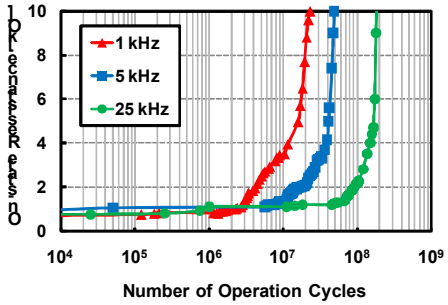

Figure 8: Evolution of ON-state resistance (R_{ON}) with the number of hot switching cycles (50% duty cycle), for a relay with tungsten (W) electrodes, measured at 300K and 5µTorr. The increase in R_{ON} due to oxidation worsens with increasing ON-time (during which Joule heating occurs) and with increasing OFF-time (when the contacting electrode surfaces are exposed).

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