7.9 Demonstration of Integrated Micro-Electro-Mechanical Switch Circuits for VLSI Applications

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Due to transistor leakage, CMOS circuits have a well-defined lower limit on their achievable energy efficiency [1]. Once this limit is reached, power-constrained applications will face a cap on their maximum throughput independent of their level of parallelism. Avoiding this roadblock requires an alternate switching device with steeper sub-threshold slope—i.e., lower V_{DD}/I_{on} for the same I_{on}/I_{off} [2]. One promising class of such devices with nearly ideal I_{on}/I_{off} characteristics are electro-statically actuated micro-electro-mechanical (MEM) switches [6]. Although mechanical movement makes MEM circuit delay significantly larger than that of CMOS, we have recently shown that with optimized circuit topologies MEM switches may potentially enable ~10x lower energy over CMOS at up to ~100MHz frequencies [3].

This work takes an initial step towards experimental validation of these principles by leveraging recently developed switch technology and reliability enhancements [4,5] to demonstrate several monolithically integrated MEM switch-based building blocks. Specifically, our test vehicle (Fig. 7.9.7) includes logic, memory, and clocking structures, and we demonstrate successful basic functionality and circuit composition.

Figure 7.9.1 shows cross-section and layout views of the MEM switch [4] used in this demonstration. The device is actuated by applying an electrostatic force between the poly-SiGe moveable gate electrode and the tungsten body electrode beneath it. When sufficient voltage (V_{pi}) is applied to "pull-in" the gate, a tungsten channel (attached under the gate with an Al_2O_3 gate oxide layer) snaps into contact with the tungsten drain and source electrodes. To turn the switch *off* ("pull-out" the channel), a lower gate-to-body voltage (V_{po}) is required to reduce the electrostatic force below the spring restoring force of the gate when the switch is *on*. Endurance tests of the switch circuits on the demonstration test chip have yet to be performed, but previous results based on identical device designs indicate a lifetime greater than 10^9 cycles [4]. Although the first prototype MEM switches and circuits were fabricated with conservative dimensions (in particular, an actuation gap size of 200nm resulting in ~10V operating voltage), dimensional scaling is predicted to reap similar benefits in terms of supply voltage and energy as for CMOS [5].

Figure 7.9.2 shows the schematic and measured VTC of a MEM Inverter/XOR as well as transient waveforms for a carry-generation circuit demonstrating the use of the MEM switch as a logic element. The VTC of the XOR (*B* static at 10V) shows the expected hysteresis of the switch. This hysteresis window determines the minimum voltage swing required to switch the device *on* and *off*. Unlike CMOS, the MEM "NMOS-only" pass gate is capable of swinging full-rail at the output. This VTC shows that the device is capable of driving the necessary output voltages to overcome its own hysteresis window and switch another device. Like CMOS, this is a critical requirement to enable cascaded levels of digital logic.

The carry-generation circuit shown in Fig. 7.9.2 is designed such that during transients all of the switches will actuate at once and hence only a single mechanical delay is incurred. Circuits are designed this way due to the large disparity between electrical and mechanical time constants [3]. This is highlighted by Fig. 7.9.3, which shows the schematic and measured waveforms for a single switch pseudo-NMOS style oscillator. The waveforms enable calculation of the device's on-resistance and mechanical delay. The rising edge is dominated by the RC time constant of the 100kΩ load resistor and the capacitance due to the test

infrastructure (probecard and oscilloscope), which is estimated to be 150pF. The oscillator's falling edge sees the same load capacitance, but its delay is set by the on-resistance of the switch, which is estimated as 6kΩ for the sub-100ns falling edge. The mechanical delay of the device can be measured from the time the rising edge reaches V_{pi} to when the switch actuates; due to the low gate over-drive, the mechanical delay is measured at ~20-30µs. The estimated capacitance of the switch-gate is ~375fF, resulting in an intrinsic electrical time constant of ~2ns.

The edge rate from the switch pull-down in the oscillator also demonstrates the device's ability to drive capacitive loads. This indicates that the MEM switch may also be suitable as an I/O device. Figure 7.9.4 shows a 2-bit thermometer-coded DAC implemented using 3 MEM switch-based buffers. The measured waveforms show the DAC driving the two intermediate output levels.

The inverter, carry-generation circuit, oscillator, and DAC demonstrate the ability of MEM switches to compute and communicate, to both perform logic functions and to drive loads. Figure 7.9.5 shows a MEM switch-based latch and measured transient waveforms demonstrating correct operation in both the opaque and transparent states. The output of the latch is isolated from the inputs with two resistively-loaded inverters that also drive the feedback keeper switch. Like in CMOS, a cascade of two latches can be used to create a flip-flop.

Given its low leakage current [4], the switch is also well suited for DRAMs. Figure 7.9.6 shows a 10-bit DRAM column composed of MEM switches. The memory is constructed in a NAND configuration. The bit read line (BL_{RD}) is precharged low and the word read line ($WL_{RD}[n]$) is an active low signal that disables the read pull-up path unless the stored bit is a "1". The additional path of nominally *on* switches allows the memory to perform a read operation in a single mechanical *turn-on* delay (for decoding) plus a mechanical *turn-off* delay. Since the *turn-off* delay is much smaller than the *turn-on* delay, this configuration results in reduced read delay. Figure 7.9.6 also shows the measured results for the 10-bit memory cell, which was fully integrated except for (due to lack of vias) the wires between the drain of the storage device and the gate of the memory device (Fig. 7.9.7). Due to measurement setup limitations, the pre-charge switch is bypassed with a 100kΩ pull-down resistor. The waveforms show a simultaneous memory write and read of the same bit.

This work demonstrates the feasibility of several computational and memory building blocks implemented using only passive components and MEM switches. As shown in the exemplary circuits, MEM switches are capable of driving each other to form composable digital circuits. Because of the disparity between their electrical and mechanical time constants, re-architecting at the circuit level is required to efficiently leverage their ideal I_{on}/I_{off} characteristics. Although process scaling, device reliability, and circuit design challenges remain to be tackled before a MEM switch technology could offer an attractive alternative to CMOS, these initial circuit demonstrations confirm that MEM switches satisfy many of the basic requirements for eventually realizing this goal.

References:
[1] B. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and Sizing for Minimum Energy Operation in Subthreshold Circuits," *IEEE JSSC*, Sep. 2005.
[2] H. Kam, et al., "Circuit Level Requirements for MOSFET Replacement Devices," *IEEE IEDM*, Dec. 2008.
[3] F. Chen, et al., "Integrated Circuit Design with NEM Relays," *IEEE/ACM ICCAD*, Nov. 2008.
[4] R. Nathanael, et al., "4-Terminal Relay Technology for Complementary Logic," *IEEE IEDM*, Dec. 2009.
[5] H. Kam, et al., "Design and Reliability of a Micro-Relay Technology for Zero-Standby-Power Digital Logic Applications," *IEEE IEDM*, Dec. 2009.
[6] K. Akarvadar, et al., "Design Considerations for Complementary Nanoelectromechanical Logic Gates," *IEEE IEDM*, Dec. 2007.
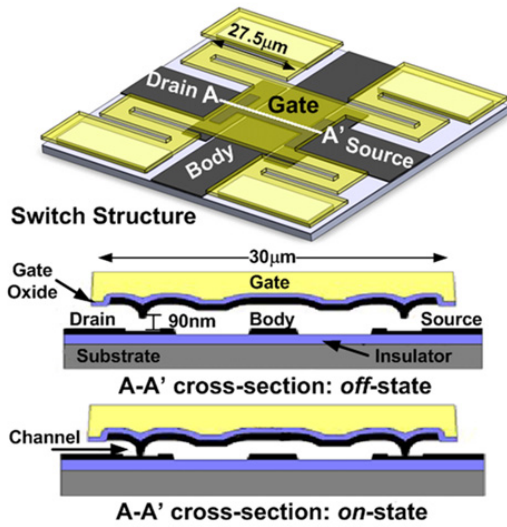
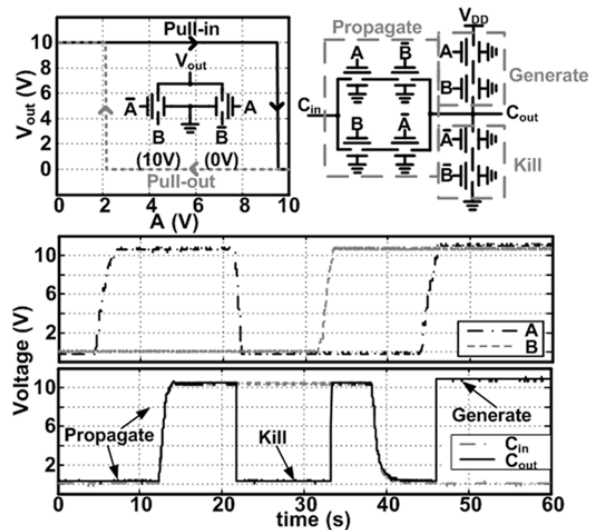Figure 7.9.1: Layout and cross-section of the MEM switch.

Figure 7.9.2: Schematic and measured VTC/transient waveforms for a MEM-switch based inverter and carry-generation circuit.
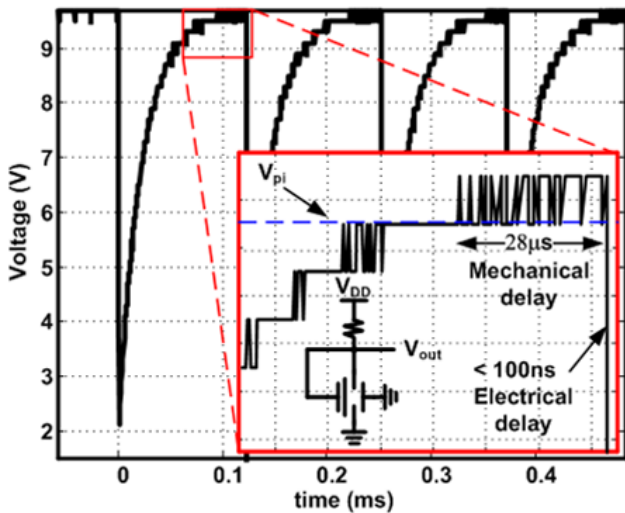

Figure 7.9.3: A single-stage single-switch pseudo-NMOS oscillator showing both electrical and mechanical delays.
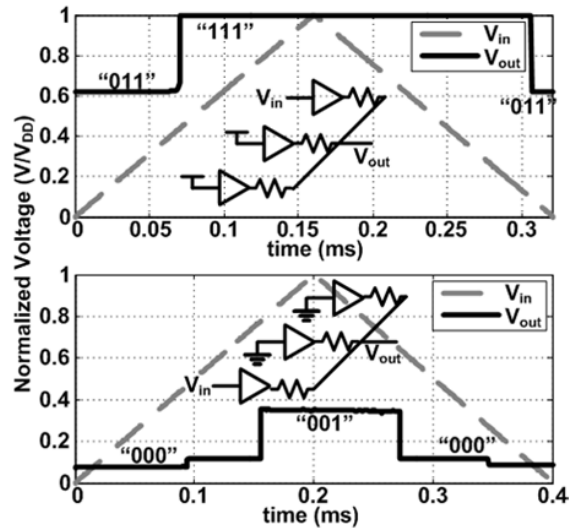

Figure 7.9.4: 2-bit thermometer-coded DAC output for "X11" and "00X" inputs, where X is the V_{in} input.
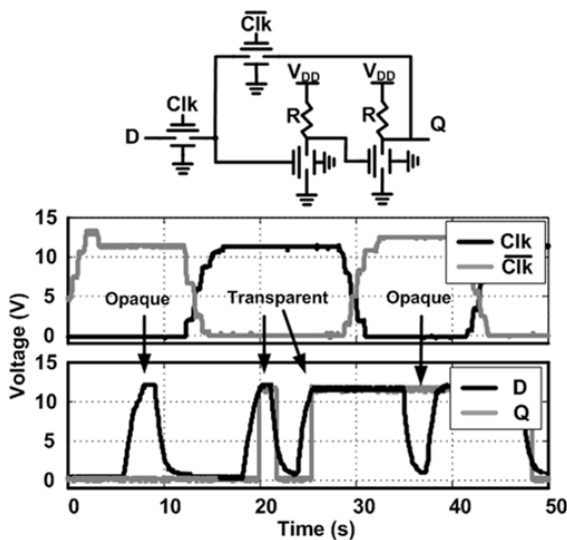

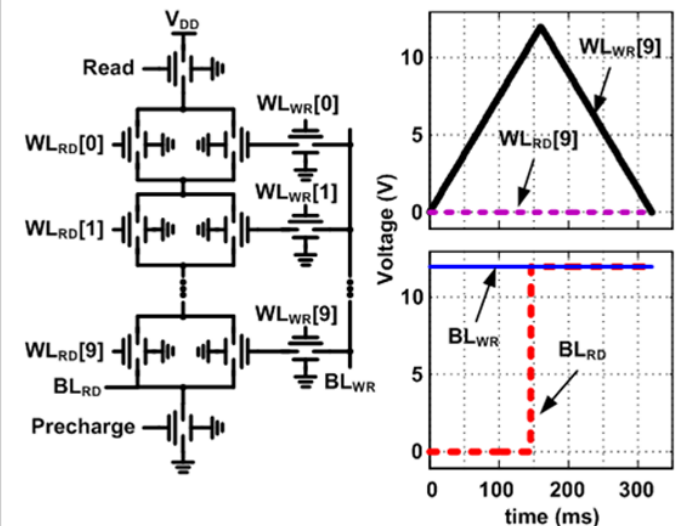Figure 7.9.5: Measured functionality of a MEM-switch based static latch.

Figure 7.9.6: Measured simultaneous read and write of a "1" to the bottom cell of a 10-cell 3-switch DRAM column.
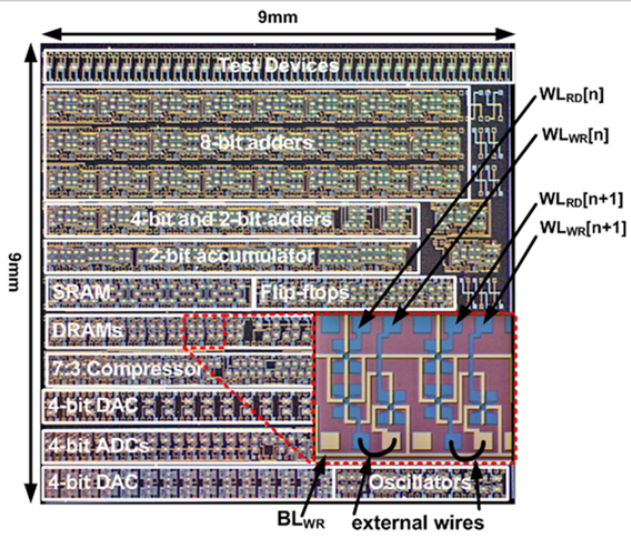
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Figure 7.9.7: Die photo of the MEM switch demonstration chip.