Problem Set 5 Solutions

March 4, 2015

1

1.1

(1 point) A MOSFET with its drain connected to its gate is referred to as a "diode-connected" device. Derive the I-V characteristic of a diode connected device. Include channel length modulation. Refer to the voltage across the two terminals as V and the current between them as I.

Solution: In a diode connected device, V_{ds} is always zero, so the device can't be in the triode region of operation. Since it is always saturated, we can apply the saturation formula.

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V - V_{th}\right)^2(1+\lambda V) \text{ if } V_{gs} > V_{th},\ I = 0 \text{ otherwise} \tag{1}$$

If λ is small and there is a lot of overdrive, this means that $I \propto V^2$.

In a BJT, this relationship would look like $I_{BJT} \propto \exp V$, which is where the term diode-connected comes from. That's no coincidence, in a BJT this connection literally applies the voltage directly across a diode.

1.2

(2 points) Make a small signal model for a diode connected device. Express your model using only the variables V, I, λ and V_{th}.

Solution: We get a small signal model by taking a derivative about an operating point:

$$\frac{dI}{dV} = \frac{d}{dV}\left[\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V-V_{th})^2(1+\lambda V)\right] \tag{2}$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{d}{dV}\left[(V-V_{th})^2(1+\lambda V)\right] \tag{3}$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[\lambda(V-V_{th})^2 + 2(V-V_{th})(1+\lambda V)\right] \tag{4}$$

$$= \frac{I}{(V-V_{th})^2(1+\lambda V)}\left[\lambda(V-V_{th})^2 + 2(V-V_{th})(1+\lambda V)\right] \tag{5}$$

$$= I\left[\frac{\lambda}{1+\lambda V} + \frac{2}{V-V_{th}}\right] \tag{6}$$

Note that if we neglect channel length modulation (i.e. $\lambda = 0$) we have the expression for g_m from the problem set 3.

The fractional change in current with respect to voltage represents a conductance. So our model is a single resistor with a value of

$$R_{model} = \frac{1}{\frac{dI}{dV}} = \frac{1}{I\left[\frac{\lambda}{1+\lambda V} + \frac{2}{V-V_{th}}\right]} \tag{7}$$

1 point setup, 1 point execution including the realization that it's a conductance.

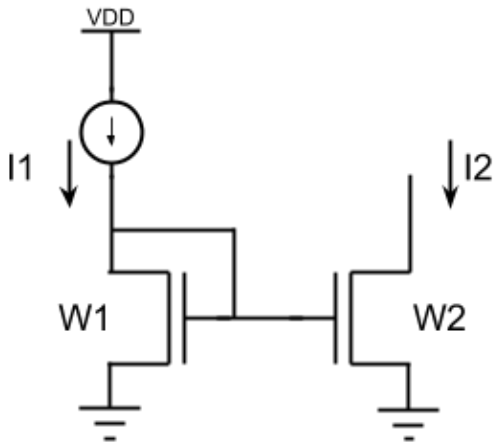

Figure 1: Diode connected device sharing voltage with another gate. An arrangement commonly referred to as a current mirror.

1.3

(1 point) If the drain-gate of a diode-connected device is attached to the gate of another MOSFET of a different width, what is the ratio of the currents in the MOSFETs? This arrangement is pictured in Figure 1.

Solution: The voltage at the drain-gate of the diode connected transistor can be found by inverting the current equation from the first problem. That algebra is hairy so we'll just refer to the inverted equation using function notation, specifically we'll say that $V = f(I)$. We'll also refer to the existing, forward current equation (Equation 1) as $I = g(V)$. By definition, $g(f(I)) = I$.

The voltage generated at the drain gate of transistor 1 is $f(I_1)$. That voltage will excite current in transistor 2 equal to

$$I_2 = \frac{1}{2}\mu C_{ox}\frac{W_2}{L}(f(I) - V_{th})^2 = \frac{W_2}{W_1}g(f(I_1)) = \frac{W_2}{W_1}I_1 \tag{8}$$

This structure, commonly called a current mirror, raises a lot of interesting questions. The mirror linearizes the tremendously non-linear behavior of the transistor. Can we use similar techniques to linearize other stuff? The answer is "yes," and the family of techniques used to accomplish that linearization are referred to as pre-distortion. Also, The W ratio seems to amplify our current if $W_2 > W_1$, can we use this structure as an amplifier?

This solution assumes transistor 2 is in saturation, which is a safe assumption in most systems where this structure is used.

1.4

(1 point) Would a current be applied at $I2$ to have the same behavior as in question 1.3? Why or why not?

Solution: It would not. The voltage at the gate of transistor 2 is much more poorly controlled by the voltage at the drain. Injecting a current at the drain would result in wild swings of the gate voltage or a triode region of operation depending on other conditions in the circuit.

1.5

(1 point) Draw a PMOS equivalent of the circuit from question 1.3.

Solution: The PMOS version is found in Figure 2. Notice that PMOS devices have to be referenced against V_{dd} for their V_{gs} to be in the proper direction.

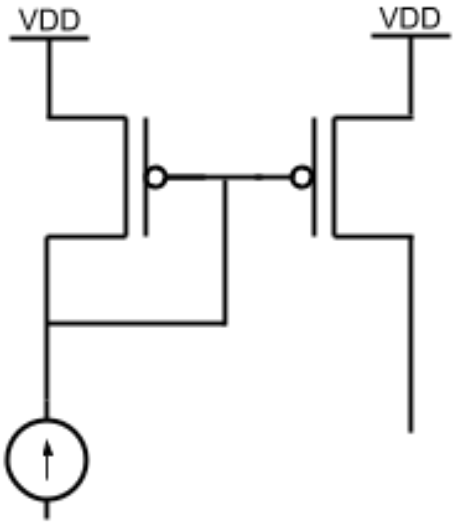

Figure 2: PMOS current mirror.

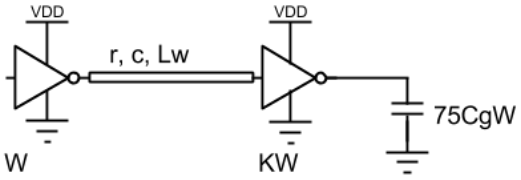

Figure 3: A digital system.

2

This question is concerned with Figure 3. r and c are the wire resistance and capacitance per unit length, L_w is the length of the wire. The NMOS in the first transistor has a width of W. As a designer, you have control of V_{dd}, K, and to some extent L_w.

Grading: For all questions in this section, give yourself a point if you set the problem up correctly. Don't be overly harsh on algebra errors.

2.1

(2 points) What is the delay of the system, t_p? You may leave your answer in terms of R_{0n}.

Solution: We treat the wire as a π model, so that we can lump the capacitance with the gate of the second inverter and the drain of the first. Each inverter turns into a single resistor with a value

of R_{0n}/W. After that, we apply Elmore delay.

$$t_p = \ln(2)\left[\frac{R_{0n}}{W}\left(3C_DW + \frac{cL_w}{2}\right) + \left(\frac{R_{0n}}{W} + rL_w\right)\left(\frac{cL_w}{2} + 3KC_GW\right) + \frac{R_{0n}}{KW}\left(3C_DKW + 75WC_G\right)\right] \tag{9}$$

$$= \ln(2)\left(\frac{R_{0n}cL_w}{2W} + 3C_DR_{0n} + \frac{R_{0n}cL_w}{2W} + 3R_{0n}C_G + \frac{rcL_w^2}{2} + 3KrL_wC_GW + 3C_DR_{0n} + \frac{75R_{0n}C_G}{K}\right) \tag{10}$$

$$= \ln(2)\left(6C_DR_{0n} + \frac{rcL_w^2}{2} + \frac{R_{0n}cL_w}{W} + 3KrL_wC_GW + 3KR_{0n}C_G + \frac{75R_{0n}C_G}{K}\right) \tag{11}$$

2.2

(2 points) What is the dynamic energy consumption per cycle of the system, E_{dyn}?

Solution: The dynamic power is given by the total capacitance being toggled multiplied by V_{dd}^2.

$$E_{dyn} = \left(3C_DW + cL_w + 3C_GKW + 3C_DKW + 75C_GW\right)V_{dd}^2 \tag{12}$$

2.3

(2 points) What is the leakage energy consumption per cycle of the system, E_{leak}? You may leave your answer in terms of t_p.

Solution: This is given by the leakage energy equation from class. Notice that we need to account for the total width of leaking transistors.

$$E_{leak} = 3W(1+K)V_{dd}I_0\exp\left(\frac{-V_T + \eta V_{dd}}{\phi_{th}}\right)t_p\,. \tag{13}$$

2.4

(2 points) What is the sensitivity of the system to L_w?

Solution: Sensitivity is defined as $\frac{\partial E}{\partial X}/\frac{\partial t_p}{\partial X}$, in this case X is L_w.

$$\frac{\partial t_p}{\partial L_w} = rcL + \frac{R_{0n}c}{W} + 3KrC_GW \tag{14}$$

$$\frac{\partial E_{dyn}}{\partial L_w} = cV_{dd}^2 \tag{15}$$

$$\frac{\partial E_{leak}}{\partial L_w} = 0 \tag{16}$$

$$\rightarrow S_{L_w} = \frac{V_{dd}^2}{rL + R_{0n}/W + 3KrWC_G/c} \tag{17}$$

Note that both derivatives are positive for all values of L, which means the sensitivity is also positive.

2.5

What is the sensitivity of the system to K?

Solution: We invoke the same reasoning here.

$$\frac{\partial t_p}{\partial K} = \ln(2)(3rC_GLW + 3R_{0n}C_G - 75R_{0n}C_G/K^2) \tag{18}$$
$$= \ln(2)(3C_GW(rL_w + R_{0n}/W(1 - 25/K^2))) \tag{19}$$
$$= \ln(2)(3rC_GL_wW(1 + R_{0n}/(rL_wW) \cdot (1 - 25/K^2))) \tag{20}$$
$$\frac{\partial E_{dyn}}{\partial K} = 3C_GW(1 + C_D/C_G)V_{dd}^2 \tag{21}$$
$$\frac{\partial E_{leak}}{\partial K} = 3WV_{dd}I_0 \exp\left(\frac{-V_T + \eta V_{dd}}{\phi_{th}}\right) \frac{\partial}{\partial K}(1 + K)t_p \tag{22}$$
$$= 3WV_{dd}I_0 \exp\left(\frac{-V_T + \eta V_{dd}}{\phi_{th}}\right) \left[t_p + (K + 1)\frac{\partial t_p}{\partial K}\right] \tag{23}$$
$$= 3WV_{dd}I_0 \exp\left(\frac{-V_T + \eta V_{dd}}{\phi_{th}}\right) t_p(K + 1)\left[\frac{1}{K + 1} + \frac{\frac{\partial t_p}{\partial K}}{t_p}\right] \tag{24}$$
$$= E_{leak}\left[\frac{1}{K + 1} + \frac{\frac{\partial t_p}{\partial K}}{t_p}\right] \tag{25}$$

The delay derivative may be negative for values of K less than 5, the dynamic energy derivative is contant with K, and the leakage derivative could be positive or negative depending on the relative values of $\frac{\partial t_p}{\partial K}/t_p$ – the fractional derivative of t_p with respect to K – and K. The derivative has the same condition for maybe being negative – $K < 5$ – but the "gain" on it is different since the derivative is compared to $1/(K + 1)$ and is normalized to t_p.

The equation for the leakage derivative is written so that it depends on the leakage energy. This is an extremely common shorthand. It is even more common to divide both sides by the leakage energy, so that we are expressing a fractional or normalized change in leakage. Of this normalized change is a simple expression. It makes the tradeoffs at any given design point easier to reason with: If you adjusting K to get a 10% fractional change in delay, then you'll get a fractional change in leakage energy equal to $1/10 + 1/(K + 1)$.

$$S_K = \frac{1}{\ln(2)}\frac{(1 + \frac{C_D}{C_G})V_{dd}^2}{rL + \frac{R_{0n}}{W}(1 - \frac{25}{K^2})} + E_{leak}\left[\frac{1}{(K + 1)\frac{\partial t_p}{\partial K}} + \frac{1}{t_p}\right] \tag{26}$$
$$= \frac{1}{\ln(2)}\frac{(1 + \frac{C_D}{C_G})V_{dd}^2}{rL + \frac{R_{0n}}{W}(1 - \frac{25}{K^2})} + 3WV_{dd}I_0 \exp\left(\frac{-V_T + \eta V_{dd}}{\phi_{th}}\right)\left[1 + K + \frac{t_p}{\ln(2)3C_GW(rL_w + R_{0n}/W(1 - 25/K^2)}\right] \tag{27}$$

2.6

(2 points) What is the sensitivity of the system to V_{dd}?

Solution: Same deal, though it's worth noting that we need to use the R_{0n} expression from class:

$$R_{0n} = \frac{1}{2\ln(2)}\frac{V_{dd}}{\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{dd} - V_T)^2} \equiv \frac{1}{\beta\ln(2)}\frac{V_{dd}}{(V_{dd} - V_T)^2} \tag{28}$$

We can express our usual set of derivatives

$$\frac{\partial t_p}{\partial V_{dd}} = \left(\frac{6C_D}{\beta} + \frac{cL_w}{\beta W} + \frac{3C_G K}{\beta} + \frac{75C_G}{\beta K}\right) \frac{d}{dV_{dd}} \frac{V_{dd}}{(V_{dd} - V_T)^2} \tag{29}$$

$$= \left(\frac{6C_D}{\beta} + \frac{cL_w}{\beta W} + \frac{3C_G K}{\beta} + \frac{75C_G}{\beta K}\right) \left(\frac{1}{(V_{dd} - V_T)^2} - \frac{V_{dd}}{(V_{dd} - V_T)^3}\right) \tag{30}$$

$$= \ln(2) \left(6C_D + \frac{cL_w}{W} + 3C_G K + \frac{75C_G}{K}\right) \frac{1}{\ln(2)\beta} \frac{V_{dd}}{(V_{dd} - V_T)^2} \left(\frac{1}{V_{dd}} - \frac{1}{V_{dd} - V_T}\right) \tag{31}$$

$$= \ln(2) \left(6C_D + \frac{cL_w}{W} + 3C_G K + \frac{75C_G}{K}\right) R_{0n} \left(\frac{1}{V_{dd}} - \frac{1}{V_{dd} - V_T}\right) \tag{32}$$

This is always negative, though it becomes close to zero for large V_{dd}.

$$\frac{\partial E_{leak}}{\partial V_{dd}} = 3W(1+K) I_0 \exp(-V_T/\phi_{th}) \frac{\partial}{\partial V_{dd}} \left[V_{dd} \exp(\eta V_{dd}/\phi_{th}) t_p\right] \tag{33}$$

$$= 3W(1+K) I_0 \exp(-V_T/\phi_{th}) \left[V_{dd} \exp(\eta V_{dd}/\phi_{th}) \frac{\partial t_p}{\partial V_{dd}} + t_p \left(\exp(\eta V_{dd}/\phi_{th}) + \frac{\eta V_{dd}}{\phi_{th}} \exp(\eta V_{dd}/\phi_{th})\right)\right] \tag{34}$$

$$= 3W(1+K) I_0 \exp((-V_T + \eta V_{dd})/\phi_{th}) V_{dd} \left[\frac{\partial t_p}{\partial V_{dd}} + t_p \left(\frac{1}{V_{dd}} + \frac{\eta}{\phi_{th}}\right)\right] \tag{35}$$

$$= E_{leak} \left[\frac{\partial t_p}{\partial V_{dd}} + t_p \left(\frac{1}{V_{dd}} + \frac{\eta}{\phi_{th}}\right)\right] \tag{36}$$

$$= E_{leak} t_p \left[\frac{\frac{\partial t_p}{\partial V_{dd}}}{t_p} + \left(\frac{1}{V_{dd}} + \frac{\eta}{\phi_{th}}\right)\right] \tag{37}$$

$$\tag{38}$$

This can be either positive or negative in theory, but will be positive in a normal system. The fractional derivative of delay should be small, maybe 10%, and η/ϕ_{th} should be large, around 40. So the η/ϕ_{th} term should swamp out the fractional delay derivative.

$$\frac{\partial E_{dyn}}{\partial V_{dd}} = 2V_{dd}(3C_D W + cL_w + 3C_G KW + 3C_D KW + 75C_G W) \tag{39}$$

$$= 2E_{dyn}/V_{dd} \tag{40}$$

This is always positive, and it is most positive when V_{dd} is high.

$$S_{V_{dd}} = \frac{2E_{dyn}}{V_{dd} \frac{\partial t_p}{\partial V_{dd}}} + E_{leak} \left[1 + \frac{t_p}{\frac{\partial t_p}{\partial V_{dd}}} \left(\frac{1}{V_{dd}} + \frac{\eta}{\phi_{th}}\right)\right] \tag{41}$$

2.7

(2 points) Given this information, can you make any assertions about the correct values for L_w, K and V_{dd}? Specify the design point at which you are making those assertions.

Solution: The sensitivity to wire length is always positive. Wire length should be minimized.

K has a odd behavior around its inflection point at $K = 5$. If $K > 5$ then the sensitivity to K becomes guaranteed positive, so K should never be higher than 5. If the "gain" ratio $(R_{0n}/W)/(rL_w)$ is known, then a firmer lower bound can be put on K. Note that $K = 5$ implies an equal fanout of both stages in the absence of the wire, which is a distribution of fanouts that can be shown to minimize delay. Obviously, increasing K past that optimal point will slow you down and burn more energy.

V_{dd} should be lowered until $S_{V_{dd}}$ is equal to S_K.

1 point for L_w behavior. 0.5 point for "they should be equal". Remaining 0.5 point for otherwise interesting discussion.