Problem Set 5

February 18, 2015

1

1.1

A MOSFET with its drain connected to its gate is referred to as a "diode-connected" device. Derive the I-V characteristic of a diode connected device. Include channel length modulation. Refer to the voltage across the two terminals as V and the current between them as I.

1.2

Make a small signal model for a diode connected device. Express your model using only the variables V, I, λ and V_{th}.

1.3

If the drain-gate of a diode-connected device is attached to the gate of another MOSFET of a different width, what is the ratio of the currents in the MOSFETs? This arrangement is pictured in Figure 1.

1.4

Would a current be applied at $I2$ to have the same behavior as in question 1.3? Why or why not?

1.5

Draw a PMOS equivalent of the circuit from question 1.3.

2

This question is concerned with Figure 2. r and c are the wire resistance and capacitance per unit length, L_w is the length of the wire. The NMOS in the first transistor has a width of W. As a designer, you have control of V_{dd}, K, and to some extent L_w.

2.1

What is the delay of the system, t_p? You may leave your answer in terms of R_{0n}.

2.2

What is the dynamic energy consumption per cycle of the system, E_{dyn}?

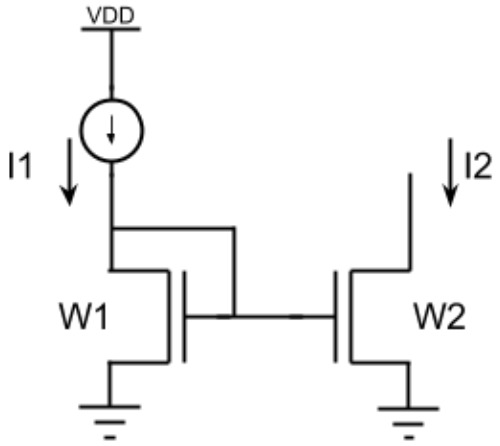

Figure 1: Diode connected device sharing voltage with another gate.

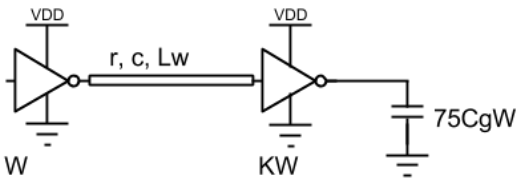

Figure 2: A digital system.

2.3

What is the leakage energy consumption per cycle of the system, E_{leak}? You may leave your answer in terms of t_p.

2.4

What is the sensitivity of the system to L_w?

2.5

What is the sensitivity of the system to K?

2.6

What is the sensitivity of the system to V_{dd}?

2.7

Given this information, can you make any assertions about the correct values for L_w, K and V_{dd}? Specify the design point at which you are making those assertions.