Problem Set 4

February 13, 2015

1

1.1

Two devices of width W and length L are connected in parallel as pictured in Figure 1a. Calculate the Id-Vg characteristic for the pair of devices. Could they be replaced by a single device?

1.2

Two devices of width W and length L are connected in series as pictured in Figure 1b. Calculate the Id-Vg characteristic for this pair of devices. Could they be replaced by a single device?

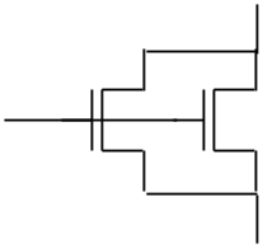
2

2.1

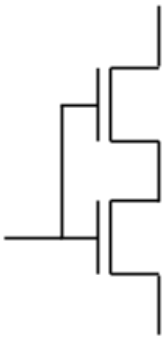
A NAND2 gate is pictured in Figure 2. Calculate the leakage current in the gate for each value of A and B. The gate is sized to match the pull-down delay of an inverter with width W.

2.2

If inputs A and B each have a 50% chance of being one each cycle, what is the average leakage energy per cycle through the gate? The logic is being run at a frequency f_s.



(a) Parallel connection of transistors.



(b) Series connection of transistors.

Figure 1: Interesting transistor connections.

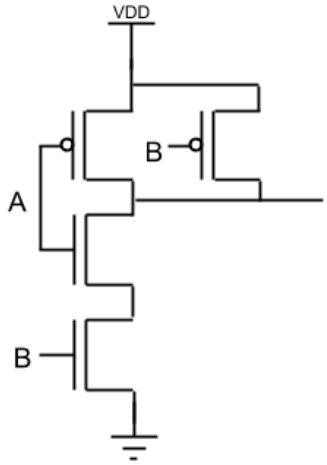


Figure 2: A NAND2 gate.

3

3.1

Draw the band diagram for a NPN transistor in all three modes of operation and indicate the qualitative directions and magnitudes of carrier flow. As background, npn transistors consist of two back-to-back pn junctions with the p region being very small. It is doped as n_+, p, n.

3.2

Repeat for a PNP transistor.

4

4.1

Find an expression for electron concentration and hole concentration as a function of doping by using the law of mass action for electrons and holes ($np = n_i^2$) and the law of charge conservation for electrons and holes.

4.2

What do these expressions simplify to if $N_A >> N_D$.