Problem Set 3

February 8, 2015

1

Draw a NOR2 gate and include the widths of its transistors in terms of W_{inv}, the width of an NMOS in an inverter. Assume $R_{0p} = 2R_{0n}$ and recall that we ignore C_D when sizing a gate.

2

Calculate the pull-up and pull-down delays in a NAND4 gate sized, by our normal algorithm, to match delay with an inverter that has an NMOS width of W. Be sure to include C_D in these calculations.

3

3.1

It is possible to express the delay of an inverter as $t_d = t_{inv}(f+\gamma)$ where $f = C_l/C_{in}$ and $\gamma = C_D/C_G$. What is t_{inv}? Note that $C_{in} = C_{GN,tot}+C_{GP,tot} = 3W_{inv}C_G$. Note that C_G and C_D are capacitance densities (capacitance per unit width).

3.2

Express the delay of three inverters in series driving a load of $C_L = 48C_GW_{inv}$ using this form of the delay. Assume the first inverter has a NMOS width of W_{inv}, the second has an NMOS width of $4W_{inv}$ and the last has a width of $16W_{inv}$. Also assume $\gamma = 1$. Could the delay of this series of inverters be reduced by changing the widht of the second or third inverter? Would it change the power consumption?

4

A capacitor is connected to a voltage source which has a variable value (i.e. a "step source"). The source steps from 0 to $V_{dd}/2$, remains at that value until the capacitor is fully charged, and then steps from $V_{dd}/2$ to V_{dd}. What is the total amount of energy pulled from the source?

5

Assume $C_D = 1\text{fF}/\mu\text{m}$, $V_{th,p} = V_{thn} = 0.4\text{V}$ and $V_{dd} = 1\text{V}$. Make sure all plots capture interesting features of the curves they depict, vary the range of sweeps to capture this if necessary.

5.1

Plot the bandwidth vs. power curve for a common source amplifier. Use the minimum width amplifier for any given bandwidth. Finding this minimum width will require an interative solution. Include curves for gains of 2, 3, 5, and 10.

This question requires us to formalize the relationship between g_m and I_d, it is

$$g_m = \frac{2I_D}{V_{gs,dc} - V_{th}} \text{ when } I_d/W < J_{crit} \tag{1}$$

where J_{crit} is some critical current density. We'll use $J_{crit} = 100\mu\text{A}/\mu\text{m}$.

In a common source amplifier, the $V_{gs,dc}$ would probably be ≈ 0.8V. This limits the maximum input swing the amplifier can accept, but figuring out how to fix that is a subject for another class. Let $C_L = 20$fF.

5.2

Plot the delay vs. energy curve for an inverter driving the load capacitance. Include curves for $C_L = 12\text{fF}, 40\text{fF}$ and 200fF. Assume $R_{0n} = 1\text{k}\Omega \cdot \mu\text{m}$.