

Problem Set 2 Solutions

February 3, 2015

1

This question is based off of material from B. Boser at UC, Berkeley.

1.1

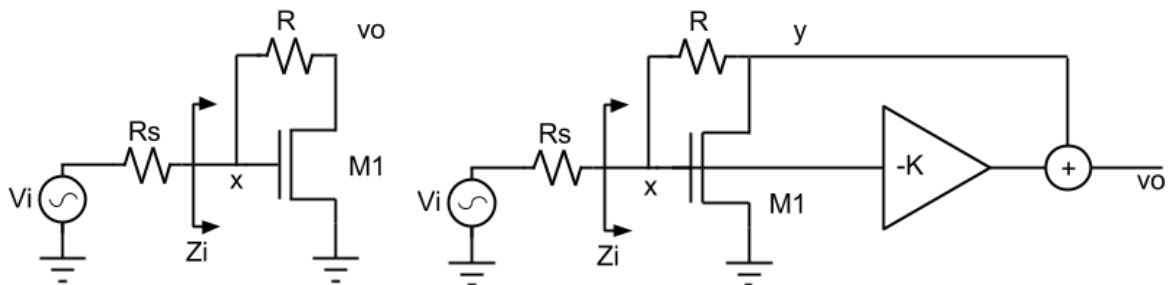
(5 points) Figure 1a represents a common type of amplifier which consists of $M1$ and R called a transimpedance amplifier. R_s in this model could represent the output of any number of sensors. Often R_s will be quite high, which means the sensor will have a great deal of voltage noise and will output very little current. Per the maximum power transfer theorem, the most power will be pulled out of the sensor when the input impedance of the sensor is the same as the source impedance: i.e. when $Z_i = R_s$.

Use our standard analog model to find the following: Z_i , the relationship between g_m and R_s , the gain from v_i to v_o , and the noise factor of the circuit. Assume the system is impedance matched, R is noiseless, C_{in} is insignificant (we're going slow), r_o is large and C_d is small. Note that R_s doesn't count as "part of the amplifier" for purposes of calculating the noise factor. Instead it is considered to be input noise.

Solution: If we are neglecting C_{in} , C_D , and r_o , the amplifier can be represented by the equivalent circuit in Figure 2. There's only a single branch in that circuit, so applying a test current source between the left nodes implies that i_t will be flowing through the dependent g_m source on the right. Because $i_{gm} = g_m v_i$, we can conclude that $v_i = i_t / g_m$. v_i is the voltage across our test current source, so $Z_i = 1/g_m$.

Under impedance matched conditions $Z_i = R_s$, so $g_m = 1/R_s$.

We can find v_o in two ways, using current continuity or feedback. We'll look at feedback later in the semester. With current continuity we use the nodal method and KCL to observe that any



(a) Transimpedance Amplifier

(b) Modified Transimpedance Amplifier

Figure 1

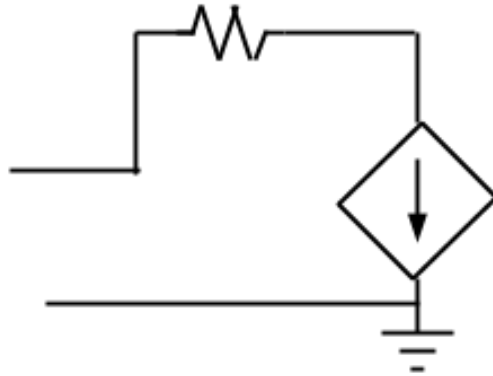


Figure 2: Equivalent Circuit for Transimpedance Amplifier.

current which passes into node x also passes out through the g_m source.

$$i_{sys} = \frac{V_i - V_x}{R_s} = V_x g_m \rightarrow \frac{V_x}{V_i} = \frac{1}{g_m R_s + 1} = \frac{1}{2} \quad (1)$$

$$\frac{V_i - V_o}{R + R_s} = g_m V_x = \frac{V_i}{2R_s} \quad (2)$$

$$\frac{V_o}{V_i} = 1 - \frac{R + R_s}{2R_s} = \frac{1}{2} \left(1 - \frac{R}{R_s} \right) \quad (3)$$

There are two sources of noise in this amplifier, noise from the source resistor and the transistor. The R_s noise appears across the same nodes as the input would, so referring it to the output just involves multiplying by the square of the the voltage gain. Modeling the transistor as a current source it is easy to see that it can be referred to the output through Z_o^2 , the impedance of the output.

We can find Z_o by attaching a test voltage source at the output, which is depicted in Figure 3. The test voltage source will see two legs, one of which is the two resistances R and R_s in series, and one which is a the g_m source. The current in the resistor leg will control the g_m source based on the divided test voltage.

$$i_t = i_{res} + i_{gm} = \frac{v_t}{R + R_s} + \frac{g_m R_s v_t}{R + R_s} = \frac{v_t}{R + R_s} (1 + g_m R_s) \rightarrow Z_o = \frac{R + R_s}{2} \quad (4)$$

Using the derivation from lecture:

$$NF = \frac{SNR_i}{SNR_o} = \frac{S_i}{S_o} \cdot \frac{N_o}{N_i} = \frac{4}{\left(1 - \frac{R}{R_s}\right)^2} \cdot \frac{\frac{1}{4}\left(1 - \frac{R}{R_s}\right)^2 4kTR_s \Delta f + \frac{1}{4}(R + R_s)^2 4kT\gamma g_m \Delta f}{4kTR_s \Delta f} \dots \quad (5)$$

$$NF = 1 + \gamma \left(\frac{1 + \frac{R}{R_s}}{1 - \frac{R}{R_s}} \right)^2 \quad (6)$$

This implies that n_F is $(1 + R/R_s)^2$.

This is a bad noise factor. If $R/R_s = 3$ so that the amplifier has a gain of -2, $NF = 13/3$ (13 dB). That's a tremendous SNR hit.

1 point for each specification. 1 point for recognizing equivalent circuit.

1.2

(5 points) Figure 1b, shows a modification to this amplifier. Is this a good modification? How much power is the K amplifier allowed to consume relative to the transistor in order to be considered a

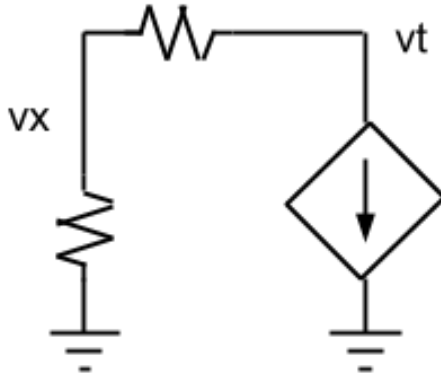


Figure 3: Equivalent Circuit for Transimpedance Amplifier.

good power tradeoff?

Solution: Nothing can be done about the R_s noise at the amplifier input since it is indistinguishable from a real signal. However, this modification to the amplifier does address the noise contribution of the MOSFET because the MOSFET noise contribution at nodes y and x will be correlated.

The total output noise density considering that correlation is given by the transfer function from the noise current source to v_y and v_x .

$$v_{on}^2 = A_v v_i^2 + 4kt\gamma g_m \left(\frac{1}{2}(R + R_s) - KR_s \right)^2 \quad (7)$$

If we pick $K = \frac{1+R/R_s}{2}$ then the contribution of the MOSFET will be perfectly cancelled, our n_F will be zero and our NF will be one.

$$NF = \frac{S_i N_o}{S_o N_i} = \frac{1}{A_v^2} \frac{4kTR_s \Delta f A_v^2 + 4kT\gamma g_m \Delta f(0)}{4kTR_s \Delta f} = 1 \quad (8)$$

Using our expression for amplifier dynamic range, $DR = V_{dd} \sqrt{C/8kTn_F}$, we can show that doubling n_F cost less than 4x the amplifier power to be competitive with simply increasing the output capacitance. In this case, $n_{F,candidate}/n_{F,baseline} = \infty$ so we're willing to pay any amount of power to implement the K amplifier.

Or are we? This analysis neglects noise contributed by the K amplifier. If you can make a very low noise K amplifier that works over the whole band you're interested in, why bother with the transimpedance amplifier at all? The reason you might consider this set up is to achieve both impedance matching and low noise – notice that the MOSFET noise is given by g_m , which we picked to match the impedance.

2 points for correlated noise setup/concept, 1 point for correlated noise evaluation, 1 points for allowing infinite power to K amplifier, 1 point for critical reasoning about answer

2

2.1

(1 point) Consider the composite ADC+amplifier system from problem set 1. The Figures for that problem are reprinted in Figure 4. Now that we have the machinery to include quantization noise in our calculations, recalculate the dynamic range of the system. The amplifier still has an input referred thermal noise of $NkT\Delta f$ and a bandwidth of ω . $\sqrt{NkT\omega} = V_{i,sw}/20$ is also still true.

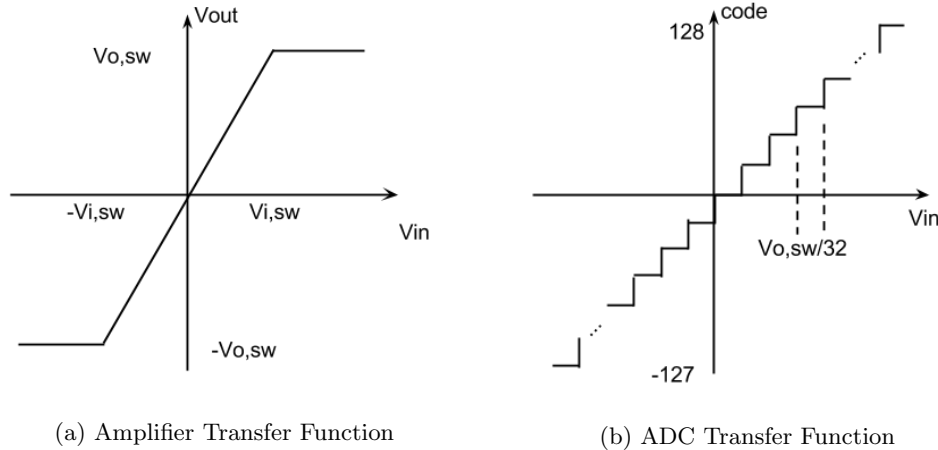


Figure 4: Transfer functions for dynamic range calculation

Solution: The total thermal noise at the node between the amplifier and the ADC can be pulled from last week's solutions

$$v_{on}^2 = \frac{1}{4} NkT\omega \left(\frac{V_{o,sw}}{V_{i,sw}} \right)^2 = \frac{V_{o,sw}^2}{1600} \quad (9)$$

and the quantization noise can be readily expressed as

$$q^2 = \frac{\Delta^2}{12} = \frac{V_{o,sw}^2}{12288} \quad (10)$$

We can write the dynamic range easily:

$$DR = \frac{V_{o,sw}/\sqrt{2}}{\sqrt{v_{on}^2 + q^2}} = \frac{1}{\sqrt{2}\sqrt{\frac{1}{1600} + \frac{1}{12288}}} = 26.6 \quad (11)$$

This is significantly lower than last week's result. Recall that we swept thermal noise under the rug last time by saying that it was smaller than a single LSB. Including it here has obviously reduced our DR dramatically, so be sure you include all relevant noise sources in your calculations.

2.2

(1 point) Assume the amplifier + ADC system is being used to measure the potential around a shank inserted into a brain. The peaks of the voltage spikes caused by ion channels are $V_{NP} = 10\mu\text{V}$, and contain frequency components up to 10kHz. Fluctuations of other, slightly more distant, neurons causes a random, white (within the band where neuronal activity happens), background fluctuation of $v_{NN} = 1\mu\text{V}$ RMS. What is the dynamic range of this signal? Report the dynamic range in both linear scale and decibels.

Solution: The dynamic range is the max RMS value over the total RMS noise voltage:

$$DR = \frac{(V_{NP}/2)/\sqrt{2}}{v_{NN}} = \frac{0.5 \cdot 0.707 \cdot 10\mu\text{V}}{1\mu\text{V}} = 3.53 \quad (12)$$

Converting to decibels, with a dramatic emphasis that decibels represent ratios of power:

$$DR_{\text{dB}} = 10 \log \frac{P_1}{P_2} = 10 \log \left(\frac{V_1}{V_2} \right)^2 = 20 \log \frac{V_1}{V_2} = 20 \log 3.53 = 10.95\text{dB} \quad (13)$$

Notice that taking the DR in decibels is the same as measuring the SNR in decibels since we surreptitiously square the signal and the noise when we calculate the DR .

2.3

(8 points) Let's examine what it would take for our Amplifier+ADC system to be used as the front end of an implanted brain monitoring chip. Such a chip might be used to detect and prevent seizures, and obviously its ongoing power consumption would be an important consideration to avoid having to perform surgery to change the batteries.

Assume we need at least 6dB of SNR for our signal processing algorithms, and the the ADC energy/sample is 50pJ for a 100 μ V LSB at the frequencies we're interested in. Reducing the LSB size by half increases the ADC power by 8x and increasing the LSB size by a factor of two reduces the ADC power by 8x. Assume the neural signals are the same as the previous problem.

We are also changing the noise model we use for our amplifier in this problem. Assume the amplifier has the same noise figure as that of a common source amplifier rather than our tusty, fixed $NkT\Delta f$ of input noise. The size of our chip limits us to 10nF of capacitance, all of which are used in the amplifier. The amplifier consumes 2 μ W of power when operating at 10kHz with 10 nF of capacitance and a gain of 2.

How much gain should the amplifier have and what size should the ADC LSB be to minimize power? What is the bandwidth of the amplifier and the conversion rate of the ADC?

Solution: Easy parts first: the amplifier needs a bandwidth of $BW = 10\text{kHz}$ in order to capture all of the frequency components of the neural spikes. That means the ADC needs to have a sampling rate of $f_s = 20\text{ks/s}$.

To figure out the rest of the question, we need a picture of our SNR . We'll calculate it for the input of the ADC. Note that the total noise power of the neural activity is unaffected by our amplifier. The neural activity is white out to 10kHz and then doesn't exist anymore, so it's integral is unaffected by the first order roll-off of the amplifier. That means it just appears as a noise variance, in the same way as quantization noise.

$$SNR = \frac{A_v^2(V_{NP}/2)^2/2}{A_v^2 v_{NN}^2 + \frac{kT}{C}(1 + \gamma A_v) + \frac{\Delta^2}{12}} \quad (14)$$

$$\frac{1}{SNR} = \frac{8v_{NN}^2}{V_{NP}^2} + \frac{8kT/C}{A_v^2 V_{NP}^2} + \frac{8\gamma kT/C}{A_v V_{NP}^2} + \frac{8\Delta_0^2}{12B^2 A_v^2 V_{NP}^2} \quad \text{where } \Delta_0 = 100\mu\text{V}, B \equiv \Delta_0/\Delta \quad (15)$$

$$\frac{V_{NP}^2/v_{NN}^2}{8SNR} = 1 + \gamma \frac{(kT/C)/v_{NN}^2}{A_v} + \frac{(kT/C)/v_{NN}^2}{A_v^2} + \frac{\Delta_0^2/v_{NN}^2}{12B^2 A_v^2} \quad (16)$$

$$0 = A_v^2 \left(1 - \frac{V_{NP}^2/v_{NN}^2}{8SNR}\right) + A_v \gamma \frac{kT/C}{v_{NN}^2} + \frac{kT/C}{v_{NN}^2} + \frac{\Delta_0^2/v_{NN}^2}{12B^2} \quad (17)$$

$$(18)$$

Applying the quadratic formula with SNR set to 2 gives us a relation between A_v and B where the SNR constraint is satisfied:

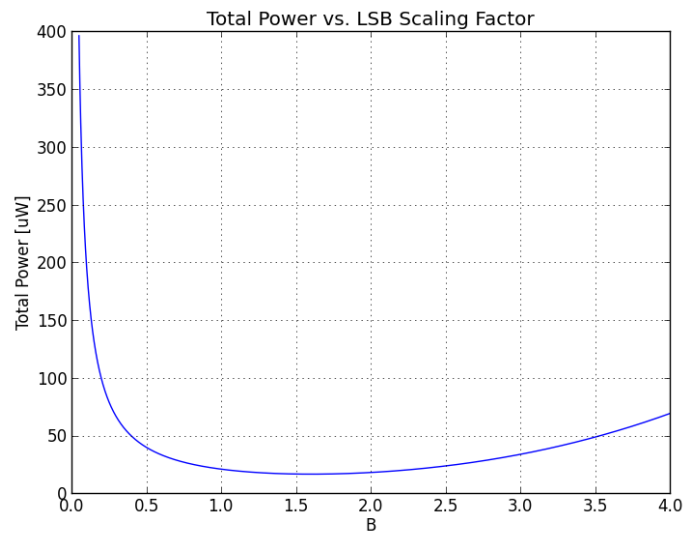
$$A_v = 0.07 + \sqrt{0.21 + \frac{392.2}{B^2}} \quad (19)$$

Our noise constraint leaves us with a decision about how much power to devote to increasing our gain and how much power to devote to reducing the size of our LSB. Our gain is equal to $g_m R$, so we can increase it linearly with power, i.e. $P_{amp} = 1\mu\text{W}A_v$. The B variable above represents scaling the power of the ADC and gives us $P_{adc} = f_s E_{0,ADC} B^3$ where $E_{0,ADC}$ is the energy per conversion with a 100 μ V step size. Combining these expressions:

$$P_{tot} = 1\mu\text{W}A_v + 50\text{pJ} \cdot 20\text{ks/s} \cdot B^3 = 1\mu\text{W} \cdot A_v + 1\mu\text{W} \cdot B^3 \quad (20)$$

The relation of A_v and B is fixed by our noise constraint, and we can substitute Equation 19 into the total power to optimize for B . The algebra for that is hairy, so I opted to do so graphically in Figure 5. There is a minimum at $B = 1.6$, which suggests that we want to make our LSB $\approx 62\mu\text{V}$ and our amplifier gain ≈ 12.4 (by Equation 19).

3 points for noise constraint, 1 point for ADC power, 1 point for amp power, 1 points for power optimization setup, 2 points for evaluation.

Figure 5: Optimization of P_{tot} vs. B