E190V Lab 3

There are two options for this lab: building a phase-locked loop or building a Buck converter. Instructions for each are below. As usual, the deliverables for the lab are a circuit and a thorough report discussing the design and measurement of the circuit. Like lab 2, the report should focus on the control aspects of your design, including carefully characterized transfer functions and/or Bode plots for each block.

Fractional-N PLL:

Use 74LS series logic and a CD4046 monolithic PLL chip to build a fractional-N PLL. Adjust the compensation network to achieve the best possible performance under the specifications below. Analyze the feedback loop carefully and be sure to report waveforms and transfer functions for each significant block that you can measure.

A fractional-N PLL is a complex system, getting an integer-N PLL and a fractional logic system working first can be a good step.

Specifications:

- Zero steady state error to a step in frequency
- Frequency step-up ratio greater than four.
- Transient settling time less than 200 cycles.
- Input clock frequency of 100 kHz

Required Measurements:

- Charge Pump Output
- VCO Control
- Frequency & Phase
- Transient response
- Output spectrum, with justifications for an spurious content
- Jitter

We don't have access to equipment to measure the output spectrum and jitter directly, but capturing many cycles in a single time-domain measurement and doing post-processing in Matlab can extract both. Discuss the jitter and spurs in your output measurement in the report.

Buck Regulator:

Use a MC34063 monotlithic buck converter, a Schottky diode and any other components you need to build a buck converter and control circuit that meets the specifications below. Characterize the converter carefully. Think about the power handling capacity of your load resistors, it is easy to blow them out if you don't pay careful attention to the delivered power.

Specifications:

- Efficiency >= 80%, best efficiency will receive a small award in bonus points
- 200 us transient settling time
- Transient current overshoot less than 2%
- Two programmable conversion ratios from 5V to 3.3 and 5V to 1.8.
- <100mV of ripple.
- Max load resistance 100 ohm, min load resistance 20 ohm.

Required measurements:

- Efficiency, including a characterization of where your loss is coming from (series resistance of the inductor? breadboard capacitance? Etc.)
- Transient response of output voltage and current as the load is switched between extreme values.
- Dynamics of feedback loop
- Ripple measurements and steady state time domain measurement of all significant nodes in the circuit.

Be sure to comment on design decisions about the operating speed and mode of the converter as well as the design of any feedback elements.