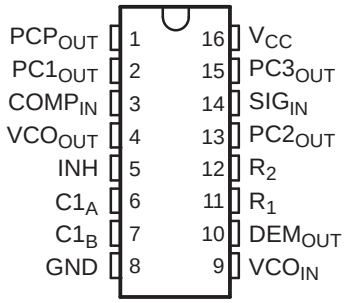
SN74LV4046A
HIGH-SPEED CMOS LOGIC PHASE-LOCKED LOOP WITH VCO

SCES656C – FEBRUARY 2006 – REVISED APRIL 2007

FEATURES

- **Choice of Three Phase Comparators**
  - **Exclusive OR**
  - **Edge-Triggered J-K Flip-Flop**
  - **Edge-Triggered RS Flip-Flop**
- **Excellent VCO Frequency Linearity**
- **VCO-Inhibit Control for ON/OFF Keying and for Low Standby Power Consumption**
- **Optimized Power-Supply Voltage Range From 3 V to 5.5 V**
- **Wide Operating Temperature Range . . . –40°C to 125°C**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

D, DGV, NS, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74LV4046A is a high-speed silicon-gate CMOS device that is pin compatible with the CD4046B and the CD74HC4046. The device is specified in compliance with JEDEC Std 7.

The SN74LV4046A is a phase-locked loop (PLL) circuit that contains a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2, and PC3). A signal input and a comparator input are common to each comparator.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the SN74LV4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear operational amplifier techniques.

ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOP – NS	Tube of 50	SN74LV4046ANS	74LV4046A
		Reel of 2000	SN74LV4046ANSR	
	SOIC – D	Tube of 40	SN74LV4046AD	LV4046A
		Reel of 2500	SN74LV4046ADR	
	TSSOP – PW	Tube of 90	SN74LV4046APW	LW046A
		Reel of 2000	SN74LV4046APWR	
	TVSOP – DGV	Reel of 2000	SN74LV4046ADGVR	LW046A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	Phase comparator pulse output
2	$PC1_{OUT}$	Phase comparator 1 output
3	$COMP_{IN}$	Comparator input
4	VCO_{OUT}	VCO output
5	INH	Inhibit input
6	$C1_A$	Capacitor C1 connection A
7	$C1_B$	Capacitor C1 connection B
8	GND	Ground (0 V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	Demodulator output
11	R_1	Resistor R1 connection
12	R_2	Resistor R2 connection
13	$PC2_{OUT}$	Phase comparator 2 output
14	SIG_{IN}	Signal input
15	$PC3_{OUT}$	Phase comparator 3 output
16	V_{CC}	Positive supply voltage

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	DC supply voltage range		–0.5	7	V
V_I	Input voltage range		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output curent	V_O = 0 to V_{CC}		±35	mA
I_{CC}	DC V_{CC} or ground current			±70	mA
θ_{JA}	Package thermal impedance(2)	D package		73	°C/W
		DGV package		120	
		NS package		64	
		PW package		108	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	125	°C
V_{CC}	Supply voltage	3	5.5	V
V_I, V_O	DC input or output voltage	0	V_{CC}	V

Electrical Specifications

PARAMETER				TEST CONDITIONS		V_{CC} (V)	MIN	TYP	MAX	UNIT
				V_I (V)	I_O (mA)					
VCO										
V_{IH}	High-level input voltage	INH				3 to 3.6	$V_{CC} \times 0.7$			V
						4.5 to 5.5	$V_{CC} \times 0.7$			
V_{IL}	Low-level input voltage	INH				3 to 5.5			$V_{CC} \times 0.3$	V
						4.5 to 5.5			$V_{CC} \times 0.3$	
V_{OH}	High-level output voltage	VCO_{OUT}	CMOS	V_{IL} or V_{IH}	–0.05	3 to 3.6	$V_{CC} - 0.1$			V
						4.5 to 5.5	$V_{CC} - 0.1$			
			TTL		–12	4.5 to 5.5	3.8			
V_{OL}	Low-level output voltage	VCO_{OUT}	CMOS	V_{IL} or V_{IH}	0.05	3 to 3.6			0.1	V
						4.5 to 5.5			0.1	
			TTL		12	4.5 to 5.5			0.55	
		C1A, C1B (test purposes only)			12	4.5 to 5.5			0.65	
I_I	Input leakage current	INH, VCO_{IN}		V_{CC} or GND		5.5			±1	µA
	R1 range(1)					3 to 5.5	3		50	kΩ
	R2 range(1)					3 to 5.5	3		50	kΩ
	C1 capacitance range					3 to 3.6	40		No Limit	pF
						4.5 to 5.5	40			
	Operating voltage range	VCO_{IN}		Over the range specified for R1 for linearity(2)		3 to 3.6	1.1		1.9	V
						4.5 to 5.5	1.1		3.2	
Phase Comparator										
V_{IH}	DC-coupled high-level input voltage		SIG_{IN}, $COMP_{IN}$			3 to 3.6	$V_{CC} \times 0.7$			
						4.5 to 5.5	$V_{CC} \times 0.7$			
V_{IL}	DC-coupled low-level input voltage		SIG_{IN}, $COMP_{IN}$			3 to 3.6			$V_{CC} \times 0.3$	V
						4.5 to 5.5			$V_{CC} \times 0.3$	
V_{OH}	High-level output voltage	PCP_{OUT}, PCN_{OUT}	CMOS	V_{IL} or V_{IH}	–0.05	3 to 5.5	$V_{CC} - 0.1$			V
					–6	3 to 3.6	2.48			
			TTL		–12	4.5 to 5.5	3.8			
V_{OL}	Low-level output voltage	PCP_{OUT}, PCN_{OUT}	CMOS	V_{IL} or V_{IH}	0.02	3 to 3.6			0.1	V
						4.5 to 5.5			0.1	
			TTL		4	4.5 to 5.5			0.4	
I_I	Input leakage current		SIG_{IN}, $COMP_{IN}$	V_{CC} or GND		3 to 3.6			±11	µA
						4.5 to 5.5			±29	
I_{OZ}	3-state off-state current		$PC2_{OUT}$	V_{IL} or V_{IH}		3 to 5.5			±5	µA
R_I	Input resistance		SIG_{IN}, $COMP_{IN}$	V_I at self-bias operating point, V_I = 0.5 V		3		800		kΩ
						4.5		250		
Demodulator										
R_S	Resistor range			R_S > 300 kΩ, Leakage current can influence V_{DEMOUT}		3 to 3.6	50		300	kΩ
						4.5 to 5.5	50		300	
V_{OFF}	Offset voltage VCO_{IN} to V_{DEM}			$V_I = V_{VCOIN} = V_{CC/2}$, Values taken over R_S range		3 to 3.6		±30		mV
						4.5 to 5.5		±20		
I_{CC}	Quiescent device current			Pins 3, 5, and 14 at V_{CC}, Pin 9 at GND, I_I at pins 3 and 14 to be excluded		5.5			50	µA

(1) The value for R1 and R2 in parallel should exceed 2.7 kΩ.
(2) The maximum operating voltage can be as high as V_{CC} – 0.9 V; however, this may result in an increased offset voltage.

Switching Specifications

C_L = 50 pF, Input t_r, t_f = 6 ns

PARAMETER			TEST CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNIT
Phase Comparator								
t_{PLH}, t_{PHL}	Propagation delay	SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		3 to 3.6			135	ns
				4.5 to 5.5			50	
t_{PLH}, t_{PHL}	Propagation delay	SIGIN, $COMP_{IN}$ to PCP_{OUT}		3 to 3.6			300	ns
				4.5 to 5.5			60	
t_{PLH}, t_{PHL}	Propagation delay	SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		3 to 3.6			200	ns
				4.5 to 5.5			50	
t_{THL}, t_{TLH}	Output transition time			3 to 3.6			75	ns
				4.5 to 5.5			15	
t_{PZH}, t_{PZL}	3-state output enable time	SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		3 to 3.6			270	ns
				4.5 to 5.5			54	
t_{PHZ}, t_{PLZ}	3-state output disable time	SIG_{IN}, $COMP_{IN}$ to PC2OUT		3 to 3.6			320	ns
				4.5 to 5.5			65	
	AC-coupled input sensitivity	(P-P) at SIG_{IN} or $COMP_{IN}$	$V_{I(P-P)}$	3 to 3.6		11		mV
				4.5 to 5.5		15		
VCO								
$\Delta f/\Delta T$	Frequency stability with temperature change		V_I = VCO_{IN} = 1/2 V_{CC}, R_1 = 100 kΩ, R_2 = ∞, C_1 = 100 pF	3 to 3.6		0.11		%/°C
				4.5 to 5.5		0.11		
f_{MAX}	Maximum frequency		C_1 = 50 pF, R_1 = 3.5 kΩ, R_2 = ∞	3 to 3.6		24		MHz
				4.5 to 5.5		24		
			C_1 = 0 pF, R_1 = 9.1 kΩ, R2 = ∞	3 to 3.6		38		
				4.5 to 5.5		38		
	Center frequency (duty 50%)		C_1 = 40 pF, R_1 = 3 kΩ, R_2 = ∞, VCO_{IN} = V_{CC}/2	3 to 3.6	7	10		MHz
				4.5 to 5.5	12	17		
				4.5[(1)]	15[(1)]		17.5[(1)]	
ΔfVCO	Frequency linearity		C_1 = 100 pF, R_1 = 100 kΩ, R_2 = ∞	3 to 3.6		0.4		%
				4.5 to 5.5		0.4		
	Offset frequency		C_1 = 1 nF, R_2 = 220 kΩ	3 to 3.6		400		kHz
				4.5 to 5.5		400		
Demodulator								
V_{OUT} vs f_{IN}			C_1 = 100 pF, C_2 = 100 pF, R_1 = 100 kΩ, R_2 = ∞, R_3 = 100 kΩ	3		8		mV/kHz
				4.5		330		

(1) Data is specified at 25°C

APPLICATION INFORMATION

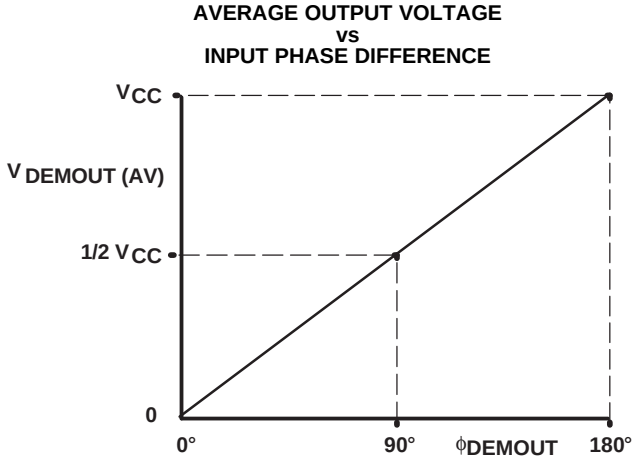


Figure 1. Phase Comparator 1: $V_{DEMOUT} = V_{PC1OUT} = (V_{CC}/\pi)$ $(SIG_{IN} - COMP_{IN})$; DEMOUT = $(SIG_{IN} - COMP_{IN})$

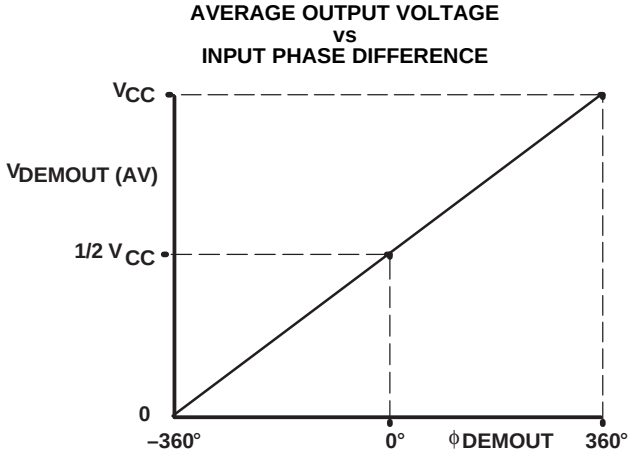


Figure 2. Phase Comparator 2: $V_{DEMOUT} = V_{PC2OUT} = (V_{CC}/4)$ $(SIG_{IN} - COMP_{IN})$; DEMOUT = $(SIG_{IN} - COMP_{IN})$

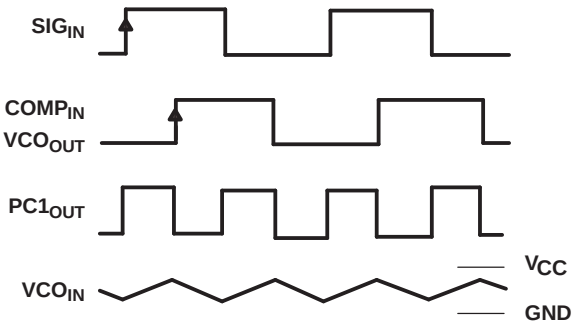


Figure 3. Typical Waveforms for PLL Using Phase Comparator 1, Loop Locked at f_o

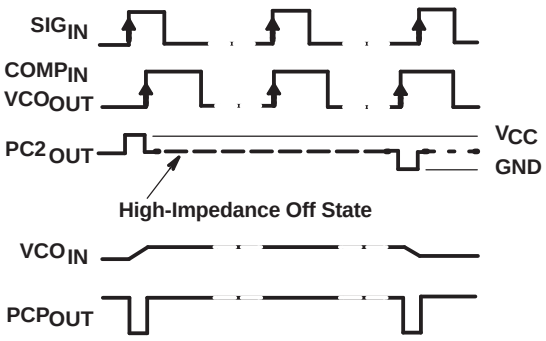


Figure 4. Typical Waveforms for PLL Using Phase Comparator 2, Loop Locked at f_o

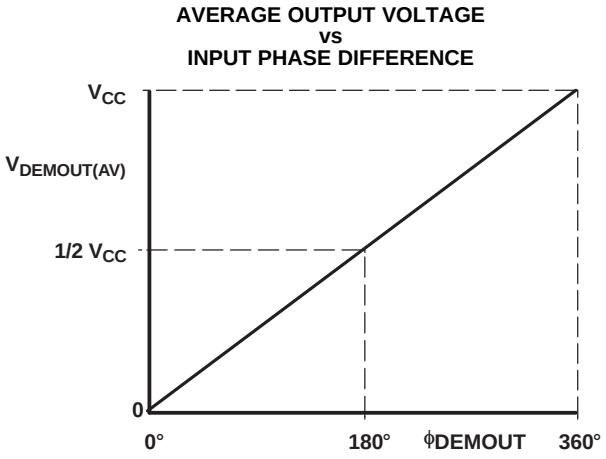


Figure 5. Phase Comparator 3: $V_{DEMOUT} = V_{PC3OUT} = (V_{CC}/2\pi)$ $(SIG_{IN} - COMP_{IN})$; DEMOUT = $(SIG_{IN} - COMP_{IN})$

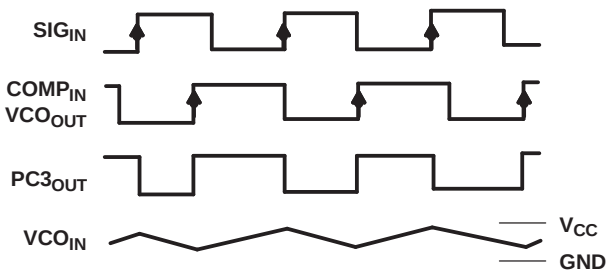


Figure 6. Typical Waveforms for PLL Using Phase Comparator 3, Loop Locked at f_o

APPLICATION INFORMATION (continued)

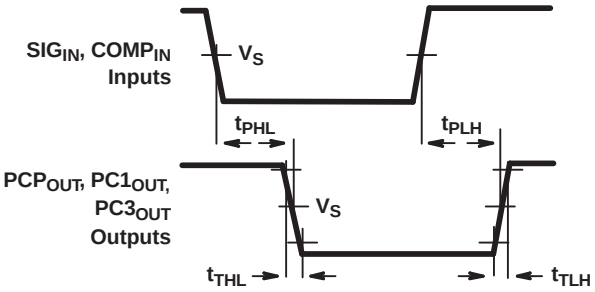


Figure 7. Input-to-Output Propagation Delays and Output Transition Times

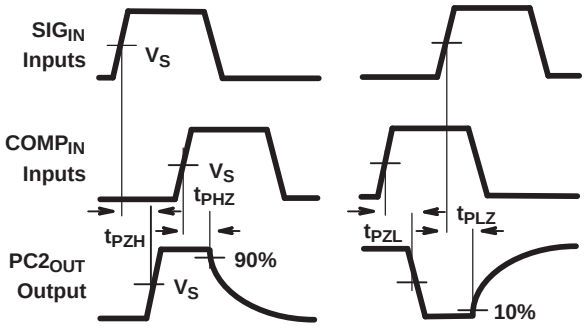


Figure 8. 3-State Enable and Disable Times for $PC2_{OUT}$

C_{PD} (1)

CHIP SECTION	C_{PD}	UNIT
Comparator 1	120	pF
VCO	120	

(1) R1 between 3 kΩ and 50 kΩ
R2 between 3 kΩ and 50 kΩ
R1 + R2 parallel value > 2.7 kΩ
C1 > 40 pF

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4046AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4046AN	Samples
SN74LV4046ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4046AN	Samples
SN74LV4046ANS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4046A	Samples
SN74LV4046ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4046A	Samples
SN74LV4046APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

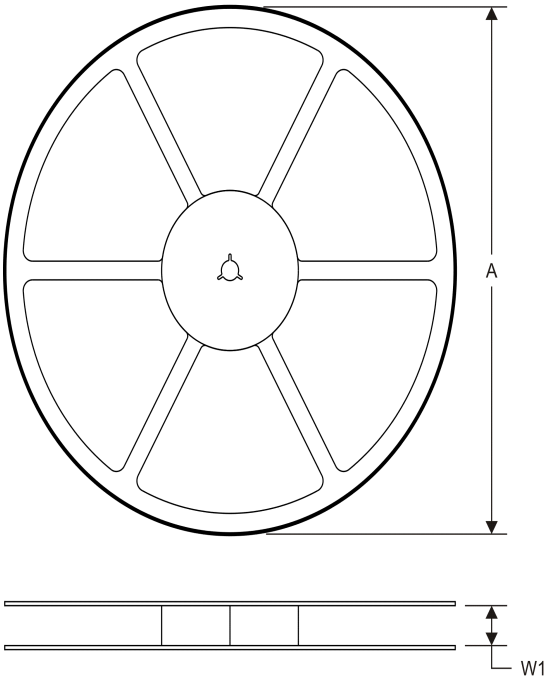
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

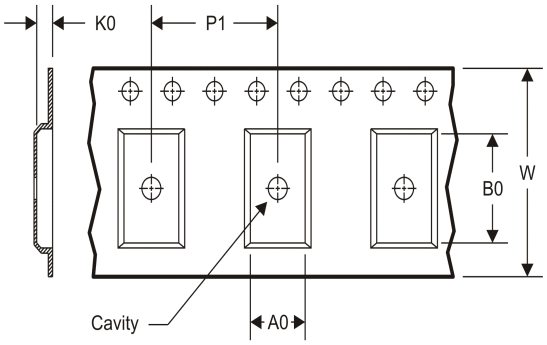
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



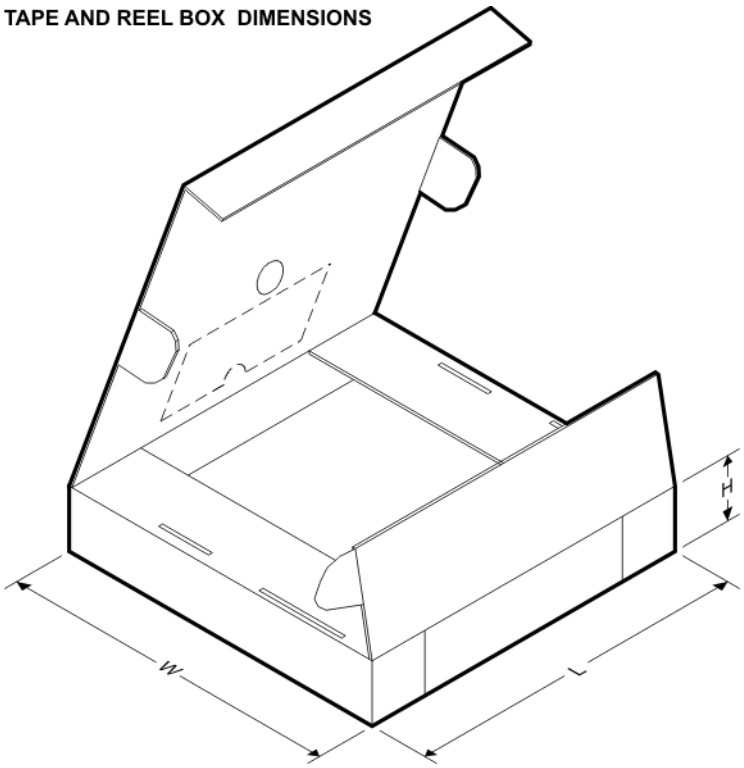
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4046ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4046ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4046ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4046APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

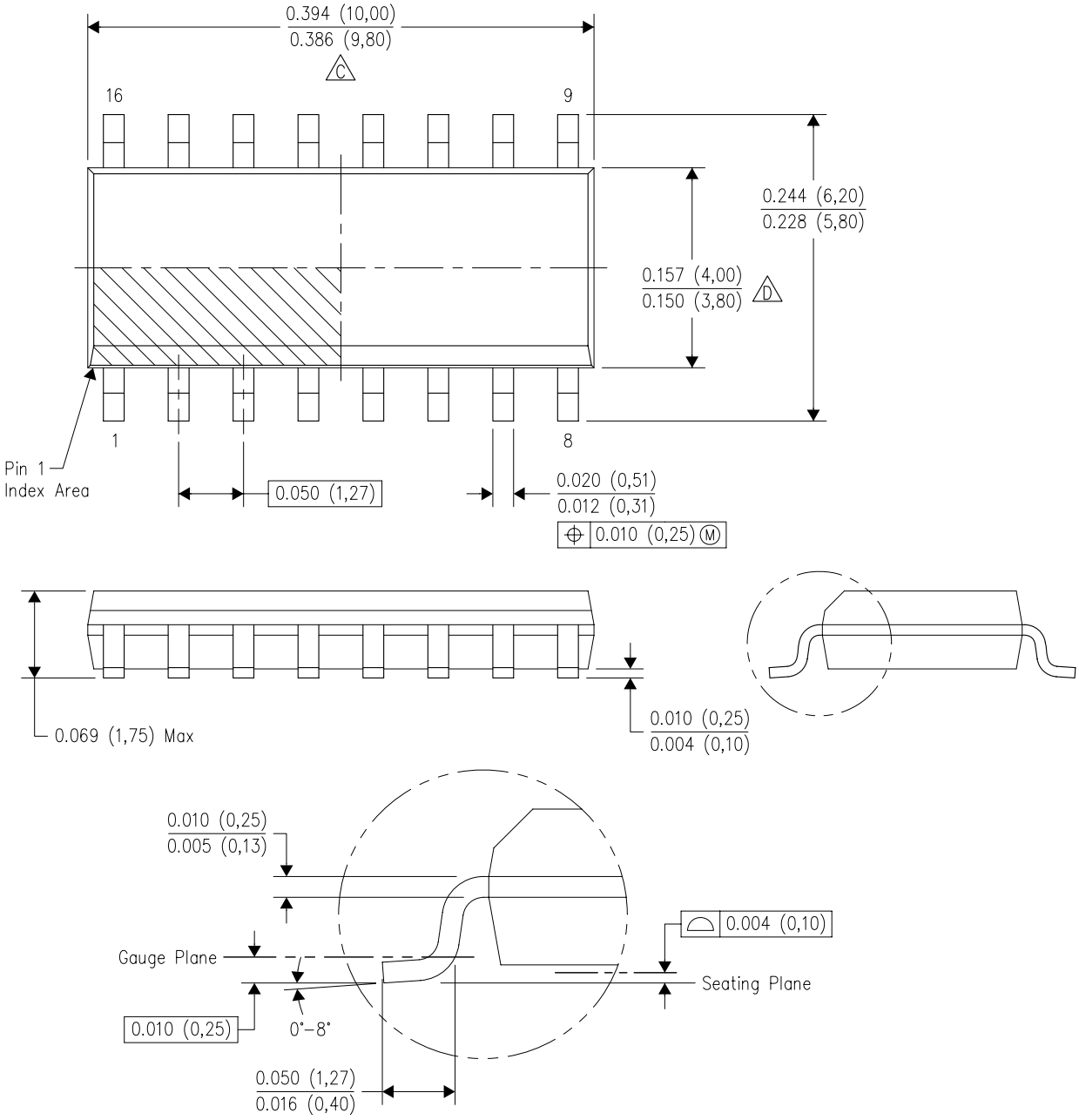
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

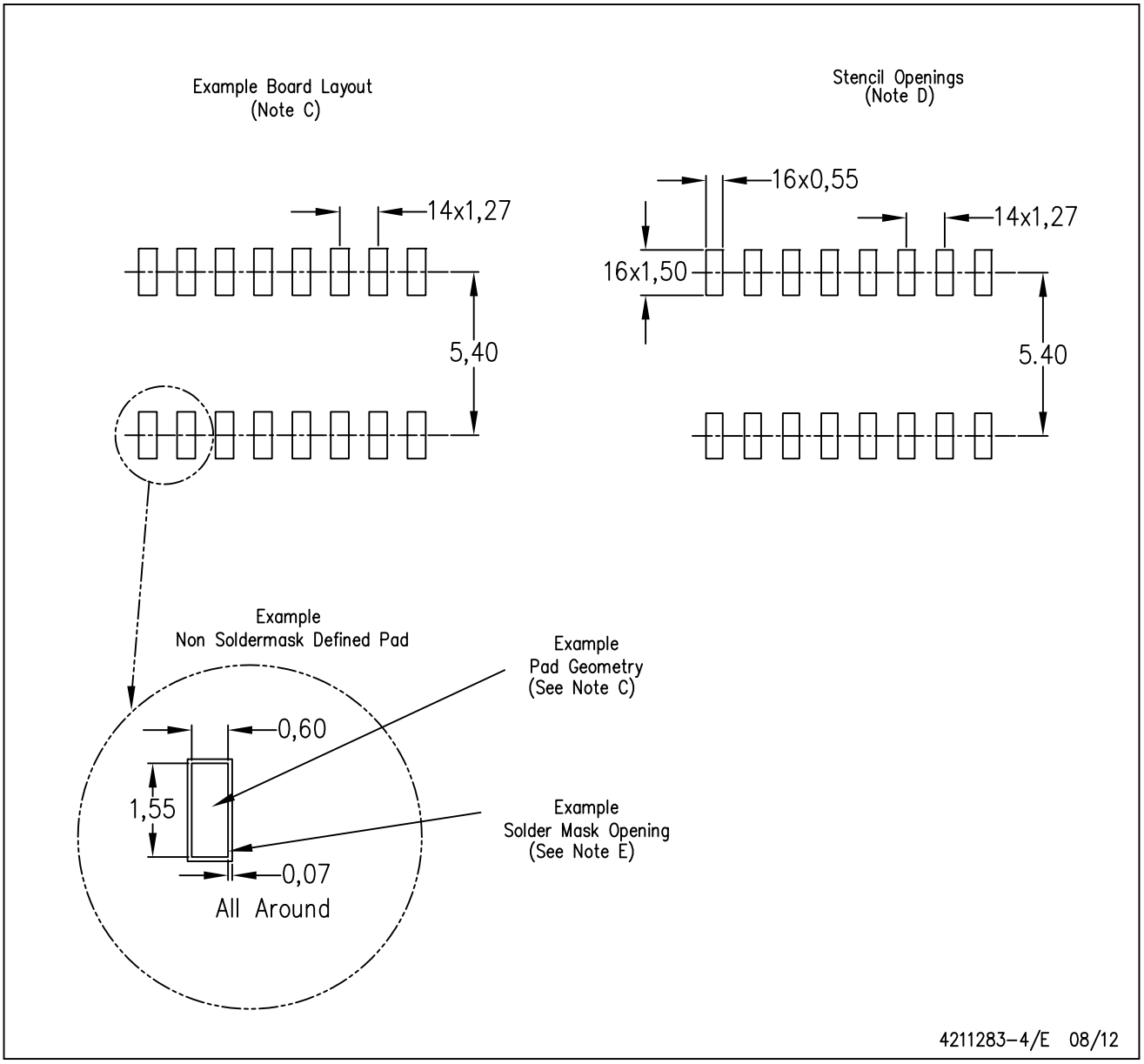
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4046ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV4046ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV4046ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV4046APWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



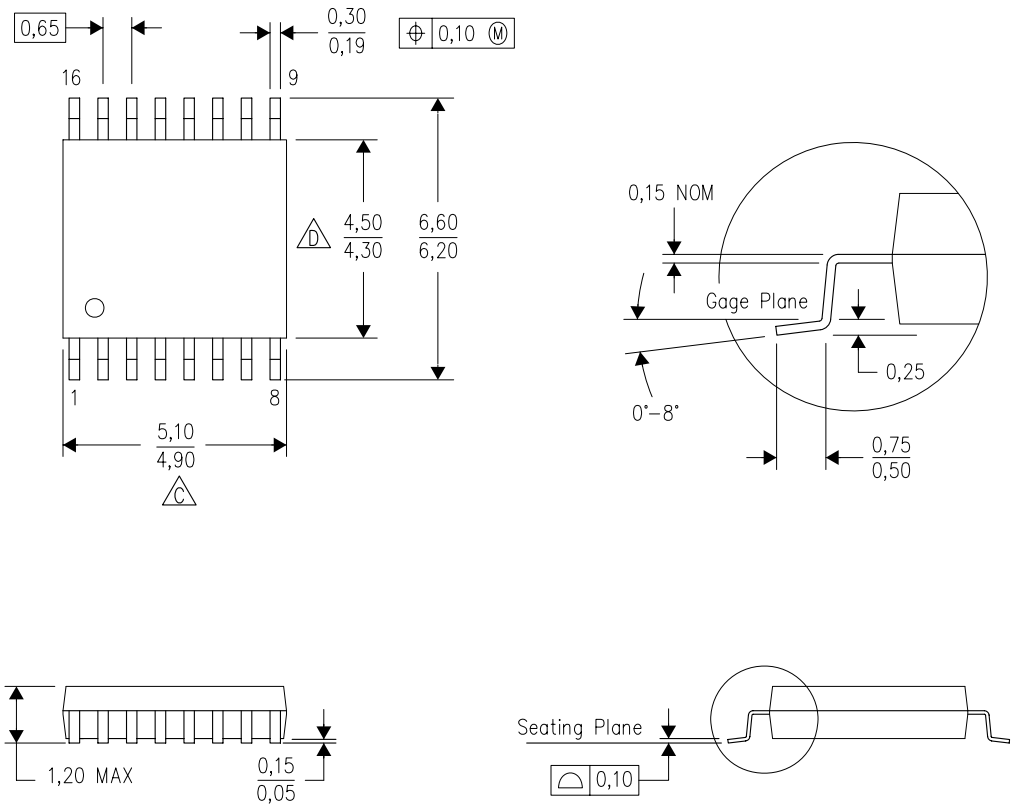
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

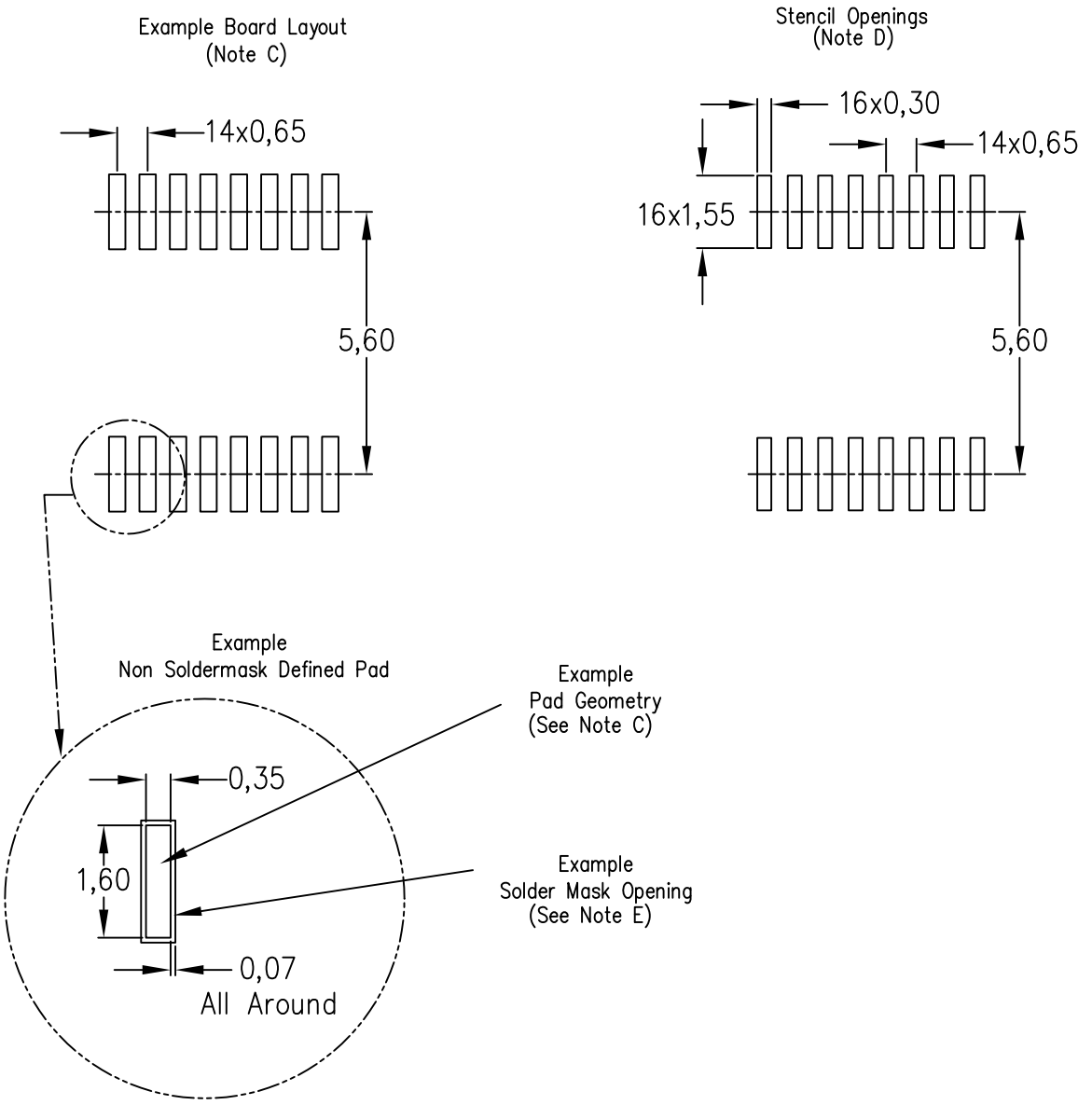
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

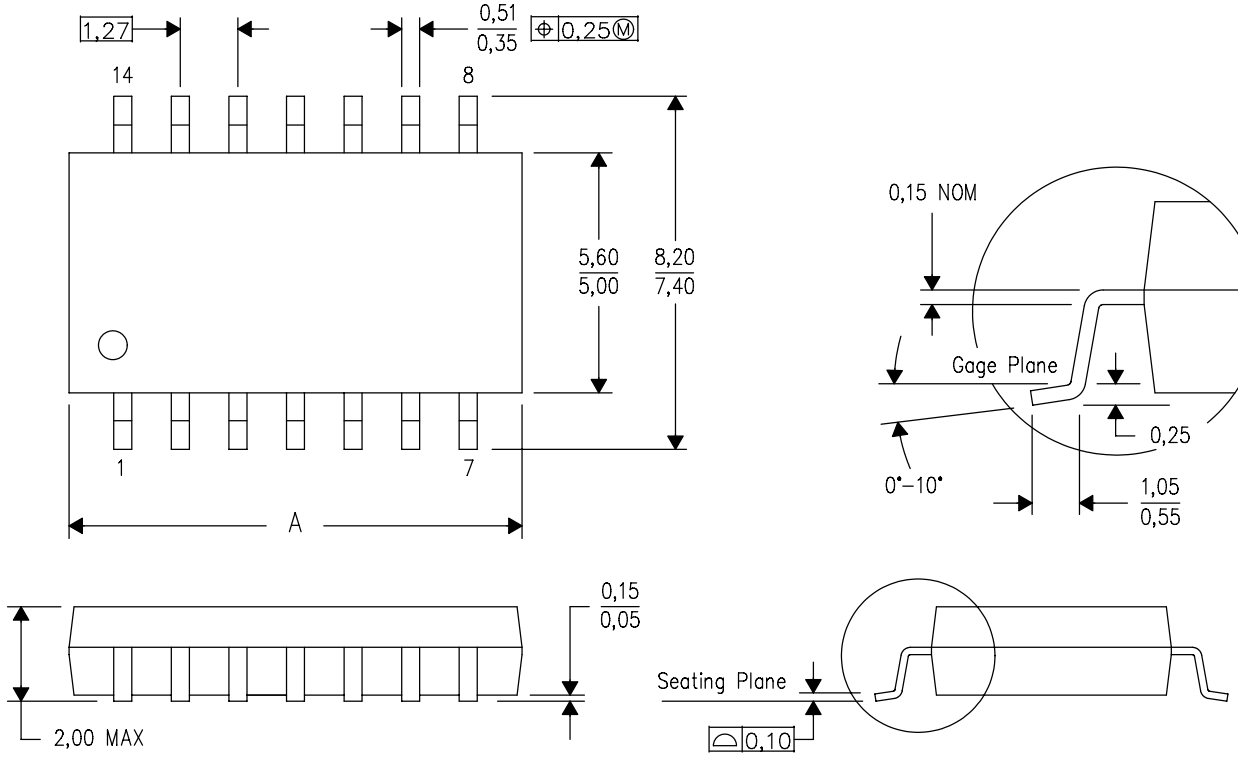


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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