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Active Loads

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In this video series we're going to start analyzing amplifiers that use transistors as their load devices instead of resistors. These transistors are referred to as active loads, in contrast with loads made of passive devices like resistors. This is a sharp deviation from every amplifier we've analyzed up until now, so we're going to start the video series by taking a moment to review resistively loaded single stage amplifiers. That review will highlight our road map for the rest of the semester, which includes building up our repertoire of analog support circuitry. Active loads are a great leaping off point into these new analog building blocks.

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Review of Single Stage Amplifiers

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In this video we're going to take a step back to survey where we are in the class and reflect on all the amplifiers that we've seen thus far.

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Single-Stage Amplifiers Lead Us to Op-Amps

- Class goal: build an op-amp
- Intermediate goal: build interesting multistage amplifier
- Path there: Diodes, BJTs, CE, multistage model, interesting stages
- We've noticed patterns in analysis as we added new stages
- Handout 1 ~ summary of properties of all single stage amps
- Handout 2 ~ summary of (3) small signal tricks to get rin, rout, av

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Our overall goal this semester is to build an op-amp. So it's worth asking how our current work relates to that goal. We're currently working on an intermediate goal of building an interesting multistage amplifier, and we have largely achieved that goal by learning about an assortment of single stage amplfiiers and coming up with rules to combine them into multistage amps. Getting there required us to cover some basic device physics: we started with diodes, then learned about BJTs, then our first amplifier, the common emitter, and then we were studying various single stage amps and the multistage model.

As we have analyzed our collection of single stage amplifiers we noticed that we were doing the same math over and over again, which we started calling small signal patterns.

I've tried to summarize some of this information on a few handouts you can find on the website. One of them is the handout for today, which contains a table summarizing the properties of single stage amplifiers. The other is a reminder of how to analyze small signal patterns.

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Summary Table for Amplifier Parameters

Name	a_v	r_{in}	r_{out}
Common Emitter	$-g_m(R_C\|\|r_O) \approx -g_m R_C$	r_π	$R_C\|\|r_O$
Emitter Follower	$\frac{\beta(R_E\|\|R_L)}{r_\pi + (\beta+1)(R_E\|\|R_L)} \approx 1$	$r_\pi + (\beta+1)(R_E\|\|R_L)$	$\approx \frac{1}{g_m} + \frac{R_S}{\beta}$
CE w/ Degeneration	$\frac{\beta R_C}{r_\pi + (\beta+1)R_E} \approx -\frac{R_C}{R_E}$	$r_\pi + (\beta+1)R_E$	$\approx R_C\|\|\beta r_o$
Common Base	$g_m R_C$	$\approx \frac{1}{g_m} + \frac{R_C}{g_m r_o}$	$\approx R_C\|\|\beta r_o$
Cascode	$-g_m R_C$	r_π	$\approx R_C\|\|\beta r_o$

≈ indicates a "lab approximation", some of which are more accurate than others.
Use exact expressions to dial in matches between analysis & simulation or to debug mismatches.

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However, you don't need to wait for the handout to see a table summarizing what we know about single stage amplifiers because I've included it here. Each cell contains a model for one amplifier parameter, and that model often contains a "lab approximation" that is a simplification of the full model. The lab approximations are great design tools, but if you're trying to get an analysis exactly right or debug a discrepancy in your model, then you should use an exact model. Also note that some of these approximations are more or less detailed than others. For instance, all of the entries that show RC in parallel with beta*ro are actually combining a handful of approximations to get to the beta*ro impedance, but beta*ro is so much bigger than RC that I didn't bother getting more accurate. Finally, note that the rin and rout entries for a common base are the behavior for finite ro, which is different than what we derived in our common base video.

Summary

- We're done with resistively loaded single stage amplifiers
- Resistively loaded single stage amplifiers are important components of multistage amplifiers, which in turn are used to build op-amps.
- We're moving on to other analog building blocks and tricks to enhance our op-amps.

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In this video we're going to talk about replacing the collector resistors in our amplifiers with transistors, a technique that's called using an active load. That name comes from transistors being "active" devices that require power, as opposed to resistors being "passive" devices that don't.

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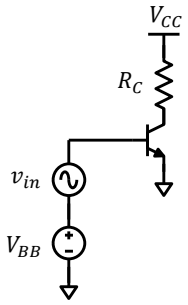
Resistors Loads Link Gain and Bias Point

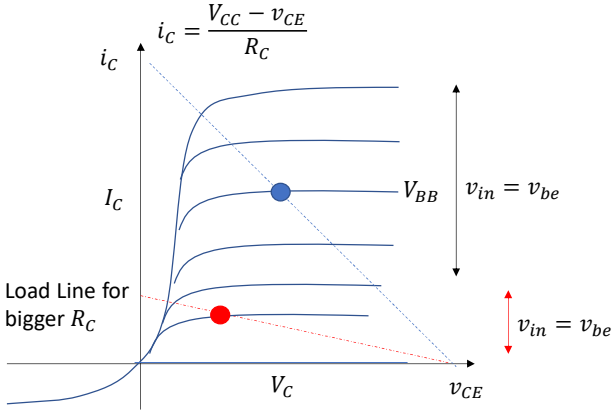


$$a_v = -g_m R_C$$

$$g_m = \frac{I_C}{\phi_{th}}$$

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$$a_v = \frac{V_{CC} - V_C}{\phi_{th}}$$



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We'll start the comparison between active and passive loads by looking at resistive loads again. We're revisiting a derivation we've seen before on this slide, and the upshot of it is that gain and the bias point, specifically the dropout of the collector resistor, are linearly related in a common emitter.

As a reminder, we found that result by noting that av is –gm*RC, gm is IC/phi_th, and IC is the dropout divided by RC. If you substitute all of those together, IC and RC fall out of the equation to show that our gain is equal to our dropout over phi_th.

We can also see that graphically by looking at a resistive load line superimposed over the NPN iC-vCE curves. Recall that our load line describes the IV relationship of the collector resistor in terms of vCE and iC. Because the load line and the NPN curves describe non-linear equations that both have to be true for applied vCE and iC, we know that their intersections describe the operating point of the circuit. However, there's one interesting difference between this circuit and the last one we examined with a load line, which is that the BJT is described by a family of curves parameterized in vbe. That means changing vbe will cause the instantaneous operating point of the circuit to move up and down the load line. We can see that if we raise vbe too high then our operating point will bump into saturation, and if we lower it too far then it will bump into cutoff.

CLICK This second curve describes a load line for a larger collector resistor. Notice that this makes the slope steeper because we traverse the same range of vce with smaller changes in vin. That's the same thing as saying the gain is higher, which matches our equations on the left. However, the larger RC also means we're operating at a much lower IC and VC, which means we have much less swing downward before we saturate. A bigger VCC could fix this, but we'd like to break the link between gain and VCC.

… Elaborate on consequences of lower IC
… This curve requires a very high VCC to pull off because the intercept is VCC/RC
… We'd like to be able to get very high gain without significantly changing VC

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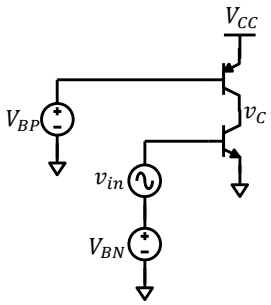
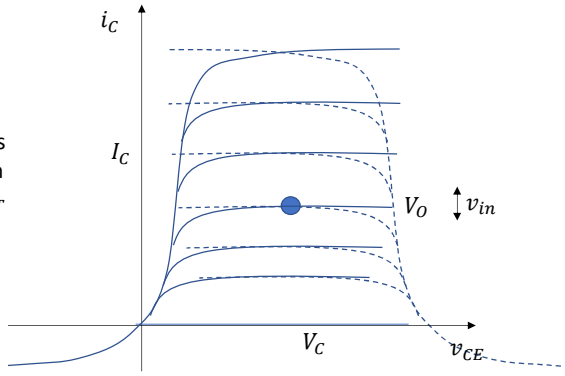
Transistor Loads Can Break Bias/Gain Link



Both transistors in FAR as long as V_C stays between $V_{CC} - V_{CESAT}$ and V_{CESAT}



Hard to make analytical calculations of bias point.

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We can do that by using a PNP device as an active load for our common emitter as pictured on the left. A quick large signal analysis of this structure is interesting: we know that both transistors will be in FAR as long as VCC is greater than 2*VCESAT and as long as vC stays between VCESAT and VCC-VCESAT. However, the large signal analysis doesn't actually tell us the large signal value of VC or what values of VBN and VBP we need to use to make this work. We'll circle back on these biasing details soon.

However, even without hammering out biasing details, we can get some quick intuition about how active loads work from load lines. Instead of superposing resistive load lines on the NPN iC-vCE curves, I've added PNP iC-vCE curves. Like NPN curves, the intersection of the load and device curves tell us where the circuit will operate. And that intersection is interesting because both the NPN and PNP curves are almost flat in FAR, so even a small deviation of vin will result in big vCE swings. That shows there's a huge gain in this structure, and we'll analyze that gain in a video soon. Even more notably, that gain is almost independent of our bias point because we see the same interaction of flat NPN and PNP curves everywhere that they are both in the forward active region.

Summary

- Resistive loads link gain and your bias point.
- Using transistors as loads (active loads) allows us to create high gain amplifiers without needing a very high V_{CC} to control the bias point.
- The bias point of a circuit with an active load is hard to predict.
- Load line analysis helps see this.

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Actively Loaded Common Emitter and Cascode

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In this video we're going to analyze some actively loaded circuits. This will give us some practice with analysis and reveal some of the neat properties that we can achieve with active loads. We're going to sidestep the problem of biasing active loads for now and instead focus on the cool tricks they can do.

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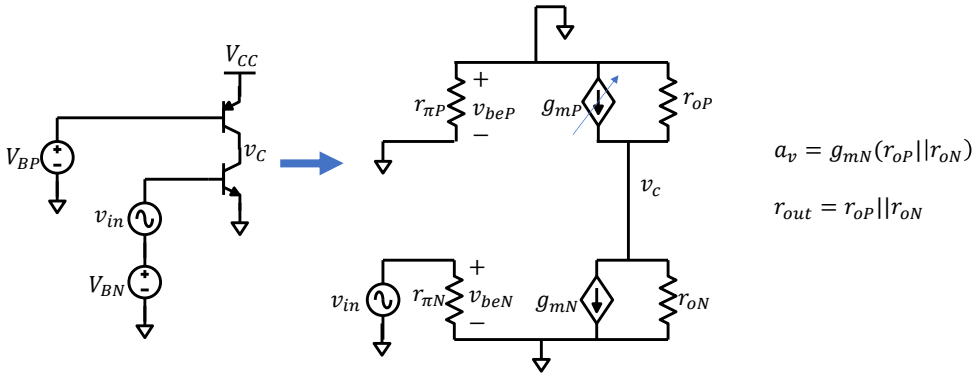
Actively Loaded CE, $a_v = g_{mN}(r_{oP}||r_{oN})$



$a_v = g_{mN}(r_{oP}||r_{oN})$

$r_{out} = r_{oP}||r_{oN}$

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We'll start by returning to a classic, the common emitter, and modifying it to use an active load. A schematic showing an actively loaded common emitter is on the left. I'd like you to pause the video, then draw a small signal model of this amplifier and find its av and rout.

CLICK Here's my version. We have a standard NPN hybrid-pi model on the bottom of the small signal model, and a PNP hybrid pi model hanging out on the top. The rpi of the PNP transistor is grounded on both sides, so the gm generator of the P transistor is shut off. That means roP is effectively acting like a load resistor for the common emitter stage at the bottom of the amplifier in a small signal sense. Accordingly, the gain is gm times roP||roN and the output resistance is the parallel combination of the resistors we see at the output: roP||roN. We do need to include roN in our models because it's about the same scale as roP, which is a deviation from our prior habit of approximating roN away when it's in parallel with a collector resistor.

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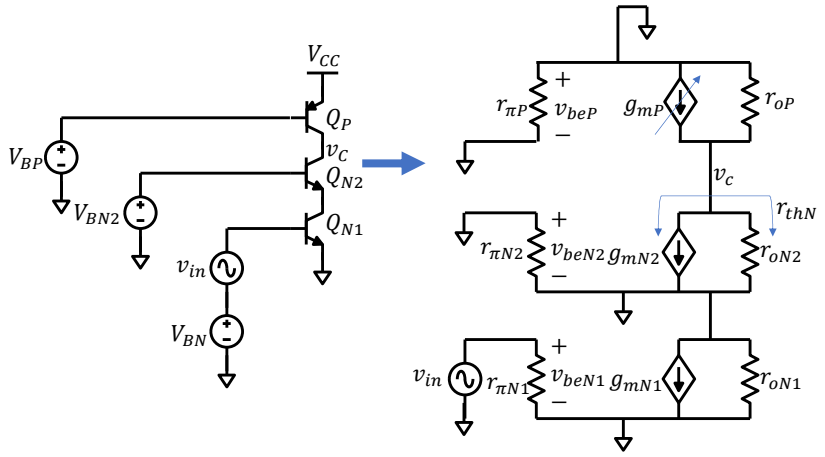
Actively Loaded Cascode, $a_v = g_{mN} r_{oP}$



$r_{thN} \approx \beta_{N2} r_{oN2}$

$r_{out} = \beta_{N2} r_{oN2} || r_{oP} \approx r_{oP}$

$a_v = -g_{mN1} r_{oP}$

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That was cool, but I wonder if we can push our gain further. Let's imagine that we used an active load on a cascode instead of on a common emitter. Pause the video, draw a small signal model of this circuit and make an estimate of its output resistance and gain.

CLICK Here's my small signal model and my answers. I reached these answers using cascode formulas that I had memorized, so I'm not going to go through the derivation step by step. The active load behaves the same way as the last slide, so it provides a resistor of value roP attached the collector of the cascode in the small signal model. The impedance looking down into the cascode, rthN, is about betaN2*roN2, which is much greater than roP, so that means our output resistance is about roP and our gain is now back to the standard cascode formula of –gm*RC, where in this case RC is roP. So using a cascode approximately doubled our gain because its very high output resistance forced all the current from gmN1 into roP.

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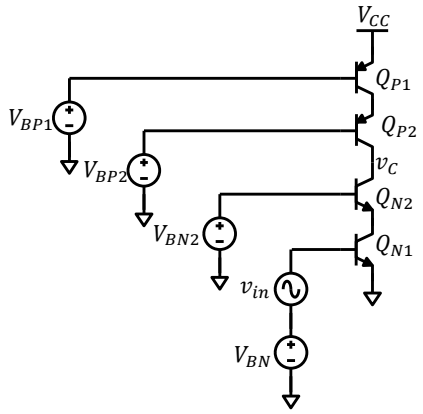
Cascode Loaded Cascode, $a_v = \beta_P r_{oP} || \beta_N r_{oN}$



See cascode impedance looking into either collector

$r_{out} = \beta_{P2} r_{oP2} || \beta_{N2} r_{oN2}$

$a_v = -g_{mN1}(\beta_{P2} r_{oP2} || \beta_{N2} r_{oN2}) \approx -\beta g_m r_o/2$

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Finally, let's go crazy and imagine a cascode loaded cascode. Here we've made an active load that looks like a cascaded amplifier, and though we won't go through the derivation, you can assume the resistance looking into the PNP cascode collector uses the same formula as the NPN cascode collector. (That makes sense because PNP and NPN devices use the same small signal model, so the PNP connected load will also have a left-right small signal pattern hidden inside of it.) Pause the video and try to estimate the rout and gain of this amplifier, but don't bother drawing the small signal model.

CLICK We see a cascode impedance looking into either collector, so our output resistance must be the upper cascode impedance in parallel with the lower cascode impedance, so betaP2*roP2 in parallel with betaN2*roN2. The voltage gain is given by the current from gm working its way to ground from the collector node, so it comes out to gmN1 times rout. Making the inaccurate assumption that all betas and ros are the same, reveals the overall gain to around beta*gm*ro/2. That's close to 400,000 if you made this amplifier out of standard transistors in our lab. And you can get that huge gain with a VCC as low as 4*VCESAT!

Summary

- Analyze active loads by drawing small signal models for all transistors, including PNPs.
- Active loads will result in output resistances or small signal patterns in the place of collector resistors.
- The very high impedance of cascodes lets us achieve high voltage gains. (Though using them is hard b/c of the comparably high rout.)

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Diode Connected Loads

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In this video we're going to look at a variation of active loads that partially solves our biasing problem. On our way there, we're going to look at the small signal model of a diode connected transistor. The amplifiers we'll look at won't come up for us too often, though they're popular in some situations, but the impedance of a diode connected load is an important take away.

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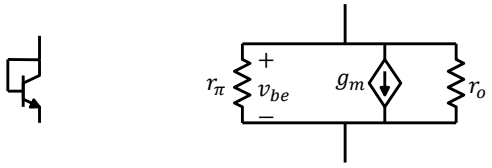
Diode Connected BJTs have $r_{th} = 1/g_m$



$$i_{th} = \frac{v_{th}}{r_\pi} + g_m v_{th} + \frac{v_{th}}{r_o}$$

$$r_{th} = r_\pi || r_o \,||\frac{1}{g_m} \approx \frac{1}{g_m}$$

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As a reminder, diode connected devices have their bases shorted to their collectors. I've included a diode connected device on this page. Pause the video, draw a small signal model of this diode connected device and then calculate its Thevenin impedance.

CLICK The small signal model just has rpi, gm and ro in parallel. You can write a KCL equation, divide off vth and flip the equation upside down to find that the impedance of the structure is rpi, in parallel with ro in parallel with 1/gm, which is approximates as 1/gm very well. An even quicker way to see this is to notice that vbe is in parallel with the gm generator, so we can replace it with a resistance of 1/gm then collapse the three resistances in parallel.

Any rate, the big takeaway is that diode connected devices have an impedance of 1/gm.

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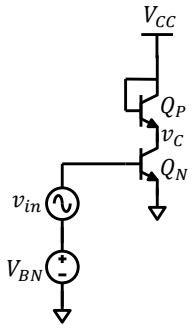
Diode Connected Loads Make Low Gain Amps



$$a_v = g_{mN} \cdot \frac{1}{g_{mP}}$$

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Even though 1/gm is a very small impdedance, you can use diode connected loads to make amplifiers. A quick large signal analysis of this amplifier reveals the large signal VC is just VCC-VBEON, which is a drawback for this type of load. Other transistors, like MOSFETS, don't have the same tight relation between their base-equivalent and emitter-equivalent terminals, so this loading technique is more popular for MOSFETS than BJTS.

The gain of this structure is easy to calculate because it's still a common emitter. We find that its gmN/gmP. You can play some tricks to change the relative gM values of these transistors. For example, you can put multiple NPNs in parallel. That lets you create small gains with large swings using this amplifier structure. The amplifier can also take advantage of the usually good local matching between transistors in integrated circuits. So you'll see these amplifiers come up in some corner cases.

Transistor matching
More common in MOSFETS, which don't have this super strict VBEON drop.
Can play some tricks to make gmN and gmP a bit different, like using several parallel BJTs to make up QN

Summary

- Diode connected transistors have an impedance of $1/g_m$.
- You can make low gain amplifiers with diode connected loads.
- This technique is more common in MOSFETs.