

Department of Engineering

## Common Emitter Linearity and a Design Example

Matthew Spencer Harvey Mudd College E151 – Analog Circuit Design

In this video series we're going to talk about our ways that our generic amplifier model fails. Though we use small signal models to describe amplifiers, we're describing a system that is non-linear at it's heart, and we'll capture that behavior with the idea of output voltage swing and percent transconductance deviation. We're also going to go through a design example for a common emitter amplifier, which I hope will be useful in your next lab, and round up a few more amplifier design specs.



In this video we're going to talk about how to identify a common failure mode of common emitter amplifiers: forcing the transistor out of the forward active region. When the transistor leaves the forward active region, our small signal model to fail because it was derived presuming forward active operation of the transistor. This will result in a non-sinusoidal outut waveform that is referred to as "clipped".



The behavior we see when our amplifier leaves the forward active region is called clipping, and a clipped waveform is pictured at the bottom of the slide. vOUT is no longer able to track the input voltage at the peaks and troughs of the wave because the transistor turns off or saturates. This example was drawn presuming a sinusoidal input, and we can see the output is no longer a sinusoid.

Clipping at VCC can be conceived of as a pretty pedestrian problem: our voltage obviously can't go outside of the voltage rails that supply our amplifier. However, there are more subtleties involved in this clipping behavior. For example, our low clipping level isn't at ground, so what's stopping the voltage from going lower?

CLICK We're going to make this circuit a little more concrete to imagine what's going on. Let's assume VCC is 10V, IC is 1mA, RE is 2kiloohms and RC is 4kilo-ohms.

CLICK We can then calculate the large signal voltages at a few important nodes. The large signal output voltage is given by VCC-IC\*RC, which is 6V. The large signal emitter voltage is given by IC\*RE, which is 2V. We are assuming IC is about the same as IE to make that last calculation.

CLICK However, wiggling our base around will cause small signal changes to be

superimposed on the large signal collector voltage at the output. That means the total signal vOUT moves around. If total signal vOUT increases by 4V, which happens when the base is decreased by some amount, then we can calculate the instantaneous collector current to be zero because the total signal vOUT is given by VCC-iC\*RC too, so iC has to be zero when vOUT=VCC. However, we only have no current in our collector when our transistor is cut off, so decreasing IC to 0mA causes the transistor to enter the cutoff region. Trying to increase our voltage further doesn't work because a cut off transistor won't respond to further decreases in vBE.

We call the maximum voltage our transistor can achieve VOMAX, and VOMAX will usually be VCC in NPN amplifiers. However, VOMAX is actually a bit shy of VCC in practice because BJTs act a bit weird at very low current levels. You should make sure to give yourself an additional volt or two of safety margin on your upward voltage swing in your designs.

CLICK On the other hand, decreasing vOUT implies that iC has increased, so we don't have to worry about cutting off the transistor. However, if vOUT reaches 2.2V, then we no longer have VCESAT across the transistor, which causes it to enter the saturation region. We call the minimum acceptable output voltage for an amplifier VOMIN.

CLICK We summarize these two behaviors by defining a new amplifier design parameter called the output voltage swing, or VSW. The swing depends on the large signal output voltage and its distance from both the maximum and the minimum output voltages. Specifically, the voltage swing captures the peak-to-peak size of the largest wave you could have at the output without leaving forward active. That peak-to-peak size is going to be given by twice the distance from the large signal output voltage to the closer of VOMAX and VOMIN. For instance, in our example vOUT can travel 4V upward before cutoff, but only 3.8V downward before saturation, therefore VSW would be 2\*3.8V or 7.6V.

Note that VSW is a large signal calculation. It only depends on large signal voltages in the circuit. That said, students find calculating VSW as a large signal value a bit funny because large signal voltages never change. That's because finding VOMAX and VOMIN implicitly acknowledges that your total signal output voltage is moving around enough to force the transistor into other regions of operation. So even though we call VSW a large signal property, it only exists because we know there is a small signal superimposed on VOUT.





In this video we're going to observe another effect that can cause a non-linear response, which is that gm often changes during the operation of a common emitter amplifier.



You can see a cartoon depicting another non-linear output from a common emitter amplifier at the bottom of this page. Here the output sine wave looks different on top than on bottom, appearing pinched and probably not reaching the full zero-to-peak value you see at the bottom of the sine wave. We refer to any non-linear behavior in an amplifier's output as distortion, and common emitter amplifiers are very distortion prone for even modest output swings.

As a side note, this distortion can often be subtle, and I have trained myself to compare the top and bottom halves of sine waves at my output to pick up the first whiffs of a distorted signal.

CLICK Like last video, we'll make the amplifier a bit more concrete to see why. Here we presume that IC is 1mA and RC is 4kiloohms.

CLICK This implies that our gm is 40mS, which we calculated at IC over the thermal voltage, and that our voltage gain is -160.

CLICK However, when our output voltage moves around, that's because the instantatneous total signal current is also changing. I've captured that by rearranging the usual vOUT=VCC-iC\*RC equation here.

CLICK That has a lot of knock-on effects. Changing vOUT means changing iC, which means changing instantaneous gm, and because gm shows up in our voltage gain it measn changing av.

CLICK If av changes as our output wave moves around, that will result in an output wave that looks different than the input wave. Predicting the exact shape of the wave is involved, but you can get a quick guess at your % error by taking the ratio of your current gain to the gain you were aiming for, which reduces to the instantaneous total signal current over the large signal current.

This is a big problem with common emitters, but you can still use a common emitter amplifier as long as your output is still a legitimately small signal. We'll learn about other circuits that let us make lower distortion gains in the near future. Department of Engineering

## Summary

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- Our CE gain is  $-g_m R_c$ , but  $g_m$  changes with changing  $i_c$  (equivalently, changes with changing  $v_{OUT}$ ).
- This produces distortion, which looks like misshapen sinusoids. Often easy to spot if top half of wave doesn't match bottom.
- % distortion is given by  $i_C/I_C$ .



In this video we're going to go through the process of designing an amplifier together so that you can see my process. Designing your first amplifier can be intimidating, but I hope this example will demystify the process.



Designing an amplifier is going from a set of specifications, like rin, rout and av, back to values of resistors, voltages and currents. In the amplifier pictured here, that means we need to pick R1, R2, RC and RE to set useful values of VOUT, VE, VB and IC. That's eight variables we have to pick or derive from other relationships. As a result, designing can feel like trying to wrangle a big pile of interconnected equations. It's even trickier because lots of designs are underconstrained, there's more than one set of values that would make them work. However, I find that if I pick a few constraints that let me pin down some values early, then you can follow the implications of those constraints through the rest of the design. Let's see an example.

For convenience, I've included the rin, rout and av for this amplifier. rout and av are our standard expressions for a common emitter, and I've modified rin to reflect that our bias network falls in parallel with rpi, which is the small signal impedance see from the base.

CLICK We're going to start with a set of constraints, some of which are technically device properties rather than design constraints. Here we set VCC to 10V, beta to 100, and say that we want rout less than 2kiloohms, rin greater than 1kiloohm and an av of -100.

CLICK We can launch from one of these constraints to a resistor value right away. rout is just equal to RC, so we know RC has to be less than 2kiloohms. This statement doesn't give

us an exact RC value, which is a problem. Life is a lot easier if we pick just one RC value because we can use that to specify other values., so I'm going to pick an RC value here. Specifically, I'm going to set RC equal to 2kiloohms.

It can be tempting to try to leave RC defined by an inequality, maybe in hopes of getting a mathematically perfect value for it later. That way lies madness. There are a lot of moving variables in a circuit design, and you'll do better if you just pick values for some elements for your first few designs.

Though it undermines my previous point a bit, it's worth noting that I picked RC=2kiloohms because that means I can use a smaller IC to get the gain I want, which will minimize power consumption in the amplifier. One unspoken constraint in almost every design is that you want to minimize power consumption. It's rare that you have so much power available that you don't want to think about it.

CLICK If we know RC, then we can find the gm we want in order to get our gain at the right value.

CLICK and that in turn implies an IC value because gm is equal to IC over phi\_t. Finding IC is a big deal in an amplifier design, and it usually cracks the design wide open. In our case, it tells us that our large signal VO, which is VCC-IC\*RC, will be 7.5V, and that rpi, which is beta\*phi\_t/IC, is going to be 2kiloohm.

CLICK We have some freedom in picking VB and VE, which makes this next step a bit fuzzy. However, we haven't guaranteed that our rin is going to work right yet, so it makes sense to start picking values that will help us meet the rin constraint. Because R1 and R2 are in parallel with rpi, we need them to be bigger than rin and possibly significantly bigger than rpi. Further, because the parallel operator favors the minimum value it operates on, it doesn't help to make R1 much bigger or smaller than R2. So let's assume they're about the same, which will put VB at 5V. VE is a VBEON drop below VB, so it will be at 4.3V. If VE is going to be at 4.3V, then we can use that knowledge to pick RE, which will set IC in turn. So we write VE=IE\*RE and remember that IE is about the same as IC, and we find that RE should be 3.44kiloohm.

This is a pretty specific value for a resistor, and we may not be able to find it in lab. That raises a lot of questions, like "Could I get away with a 3.3k resistor I have lying around? And in turn, "how exact does IC need to be"? Which further suggests, "Does our gain need to be right at -100"? These are important questions you should kick back to your client. You could also adjust your design a bit to avoid needing this weird resistor by picking a different RC. I strongly recommended partially automating your design process using a spreadsheet so you can repeat earlier steps if your find yourself asking these questions.

CLICK Finally, we need to pick R1 and R2, and I've let them be 5kiloohms. I double checked that this value will meet our rin constraint, and this value also means that a fairly high

current, of 1mA, passes through the bias network. That means we're likely to get the base voltage we're looking for without the base current of 12.5microamps messing with our bias point. That said, there are a plenty of other choices you could have made for these resistors. It's also possible to go through this design in the opposite direction, setting R1, R2 and rpi first, and using those values to inform RC and RE. Puzzling out the many paths through a design and the hidden relationships underneath them can be a really fun exerecise.

... can I find a 3.4k resistor? How close do I need to be to -100 gain?

... draw small signal models?

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## Summary

• Amplifier design can be intimidating.

• Use constraints to pin down key values, then propagate them.

• Where you have freedom, pick values that are convenient.