E151 Lecture 19 – Cascode & Mirror Dynamics
Matthew Spencer
Harvey Mudd College
ENGR151

Disclaimer

These are notes for Prof. Spencer to give the lecture, they were not intended as a reference for students. Students asked for them anyway, so I’m putting them up as a courtesy. Remember that they are not intended as a substitute for attending lecture.
Cascodes Make Your Circuit Faster

- Don’t Millerize input Cmu (you will find Cmu OCTC is rather small)
- Most caps see the 1/gm from the common base
- In general, only need OCTC for caps you know will matter ~ Millerized
- The common base rin can be higher if really big Rc, like active loads

Common Base and Mirrors are Fast

- Mirrors
  - See 1/gm from diode connected device
  - Often add a big bypass cap to stabilize mirror nodes

- Common Base
  - Cmu and Cpi both grounded on one side
  - Cpi sees 1/gm input impedance
  - Cmu sees load impedance
  - (note: CB rout is really big even with ro included)
Emitter Followers: Fast with a Zero

- Grounded Cmu makes this OK, but zero makes this hard to approx.
- Follow identical analysis from DC, but use zpi instead of rpi

\[ z_l = z_n + (g_m z_n + 1) Z_L \quad \text{with} \quad z_n = \frac{r_n}{r_n C_n + 1} \quad z_L = \frac{R_L}{R_L C_L + 1} \]

\[ z_I = \frac{r_n}{r_n C_n s + 1} + \frac{R_L}{R_L C_L s + 1} + \frac{\beta R_L}{(r_n C_n + 1)(R_L C_L s + 1)} \]

\[ z_I(j\omega) = \frac{r_n}{j\omega r_n C_n + 1} + \frac{R_L}{j\omega R_L C_L + 1} + \frac{\beta R_L}{(1 - r_n C_n R_L C_L \omega^2) + (r_n C_n + R_L C_L) \omega} \]

Emitter Follower Stability Issues w/ Cap Loads

- Potentially negative real part of rin at big w with capacitive load
- rout looks like an inductor at high frequencies

\[ z_{out} = R_k || r_0 || \frac{1}{C \mu \omega s} || \frac{z_n + R_s}{1 + g_m^2 \omega^2} \]

Dominates, goes from 1/gm up to Rs, zero/pole pair rising!
Some Device Review

- MOS cap physics
  - In Linear: $C_{gs}$ and $C_{gd}$ both have channel ($C_{ox}*WL$) and overlap cap, assign $\frac{1}{2}$ channel charge to each because it can reach
  - In Sat: $C_{gd}$ from gate-source overlap capacitance + fringe (really want overlap)
  - In Sat: $C_{gs}$ from gate-to-channel charge ($\frac{2}{3}*C_{ox}*WL$) + tiny overlap
  - In Cutoff: small $C_{gb}$ // Capacitive Divider from $C_{gc}$ & $C_{cb}$ sets non-ideality
  - Always junction caps, model complicated cap with cap matrix

- BJTs leave saturation slowly
  - Big influx of $C_b$
  - Big increase in $C_{jc}$ because it is forward biased
  - Charge transport models exist