E151 Lecture 19 – Cascode & Mirror Dynamics

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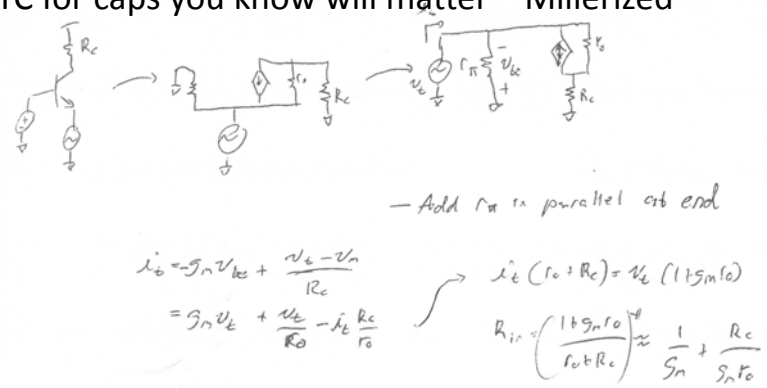
Disclaimer

These are notes for Prof. Spencer to give the lecture, they were not intended as a reference for students. Students asked for them anyway, so I'm putting them up as a courtesy. Remember that they are not intended as a substitute for attending lecture.

Cascodes Make Your Circuit Faster

- Don't Millerize input Cmu (you will find Cmu OCTC is rather small)
- Most caps see the 1/gm from the common base
- In general, only need OCTC for caps you know will matter ~ Millerized
- The common base rin can be higher if really big Rc, like active loads

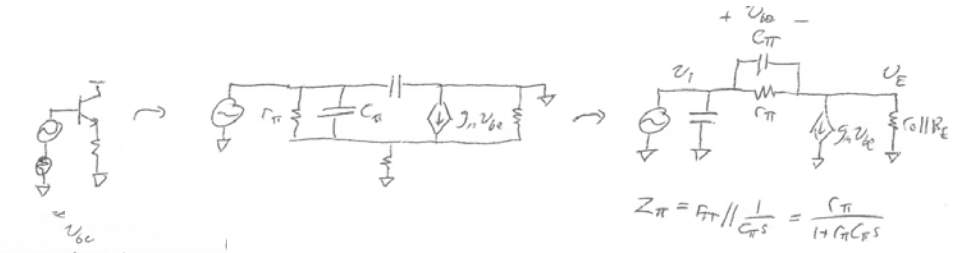


Common Base and Mirrors are Fast

- Mirrors
  - See 1/gm from diode connected device
  - Often add a big bypass cap to stabilize mirror nodes
- Common Base
  - Cmu and Cpi both grounded on one side
  - Cpi sees 1/gm input impedance
  - Cmu sees load impedance
  - (note: CB rout is really big even with ro included)

Emitter Followers: Fast with a Zero

- Grounded Cmu makes this OK, but zero makes this hard to approx.
- Follow identical analysis from DC, but use zpi instead of rpi



$$v_E = (i_\pi + g_m i_\pi Z_\pi) R_E$$

$$v_i = v_{be} + v_E = i_\pi (R_E + Z_\pi + g_m Z_\pi R_E)$$

$$Av = \frac{\beta+1}{\beta+1+\frac{r_\pi}{R_E}} \cdot \frac{1+\frac{r_\pi C_\pi}{\beta+1}s}{1+\frac{r_\pi C_\pi}{\beta+1+\frac{r_\pi}{R_E}}s}$$

$$Z_\pi = r_\pi \| \frac{1}{C_\pi s} = \frac{r_\pi}{1+r_\pi C_\pi s}$$

$$Zin = \frac{1}{C_m s} \| R_E + \frac{r_\pi}{1+r_\pi C_\pi s} + \frac{\beta R_E}{1+r_\pi C_\pi s}$$

Emitter Follower Stability Issues w/ Cap Loads

- Potentially negative real part of rin at big w with capacitive load
- rout looks like an inductor at high frequencies

$$z_i = z_\pi + (g_m z_\pi + 1) Z_L \quad \text{with} \quad z_\pi = \frac{r_\pi}{r_\pi C_\pi + 1} \quad z_L = \frac{R_L}{R_L C_L + 1}$$

$$z_i = \frac{r_\pi}{r_\pi C_\pi s + 1} + \frac{R_L}{R_L C_L s + 1} + \frac{\beta R_L}{(r_\pi C_\pi + 1)(R_L C_L s + 1)}$$

$$z_i(j\omega) = \frac{r_\pi}{j\omega r_\pi C_\pi + 1} + \frac{R_L}{j\omega R_L C_L + 1} + \frac{\beta R_L}{(1 - r_\pi C_\pi R_L C_L \omega^2) + (r_\pi C_\pi + R_L C_L) j\omega}$$

$$i_t = \frac{v_t}{r_o} + \frac{v_t}{Z_\pi + R_s} + g_m v_t \frac{Z_\pi}{z_\pi + R_s}$$

$$z_{out} = R_E || r_o || \frac{1}{C_\mu s} || \frac{z_\pi + R_s}{1 + g_m z_\pi}$$

Dominates, goes from 1/gm up to Rs, zero/pole pair rising!

Some Device Review

- MOS cap physics
  - In Linear: Cgs and Cgd both have channel (Cox*WL) and overlap cap, assign ½ channel charge to each because it can reach
  - In Sat: Cgd from gate-source overlap capacitance + fringe (really want overlap)
  - In Sat: Cgs from gate-to-channel charge (2/3*Cox*WL)+ tiny overlap
  - In Cutoff: small Cgb // Capacitive Divider from Cgc & Ccb sets non-ideality
  - Always junction caps, model complicated cap with cap matrix
- BJTs leave saturation slowly
  - Big influx of Cb
  - Big increase in Cjc because it is forward biased
  - Charge transport models exist