Design Project 2 Report Template

Names:

|  |  |  |
| --- | --- | --- |
| Parameter | Analytical | Simulated |
| Open loop gain |  |  |
| Steady State Error |  |  |
| Gain-bandwidth Product |  |  |
| Open Loop Time Constant |  |  |
| Max Capacitive Load |  |  |
| Slew Rate |  |  |
| Output Resistance |  |  |
| Input Resistance |  |  |
| Input Capacitance |  |  |
| Input Bias Current |  |  |
| Power Consumption |  |  |
| Diff Stage Bias Current |  |  |
| Gain Stage Bias Current |  |  |
| Output Stage Bias Current |  |  |
| Level Shift Bias Current |  |  |

Schematic of your circuit with labeled component values
(Draw by hand or use circuit program, LTSpice schematics are too hard to read)

Oscilloscope trace showing normal unity-gain operation on a sine wave

Open and closed loop Bode plots

Step responses for small steps and large, slew-limited steps.

Optional: Description of special feature and desired effect (~ 1/2 page max)

Screenshot of LTSpice schematic