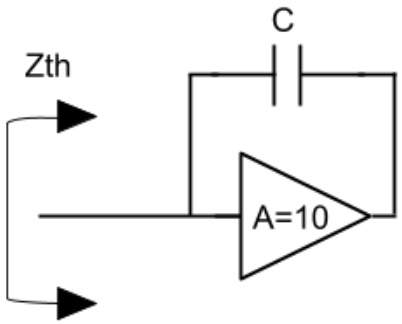

Figure 1: A gyrator circuit.

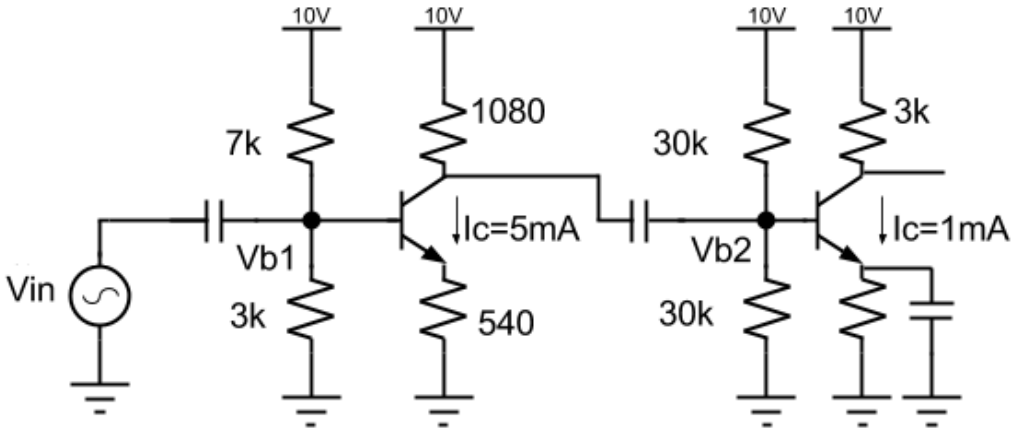

Figure 2: Two common emitter ampmlifiers for open circuit time constant analysis.

1 Warmup Problems 1 – Due Tues of 1st Dynamics Week

1. Dynamic models of MOSFETs are similar to the Hybrid-π model of a BJT: they modify our low frequency MOSFET model with a gate-to-drain capacitance, C_{gd}, and a gate-to-source capacitance C_{gs}.

   (a) Find the small signal current gain of a MOSFET and calculate its f_t.

   (b) Comment on the differences in current gain between a BJT and a MOSFET with the same g_m as the input current frequency is changed. Assume $C_\pi + C_\mu < C_{gd} + C_{gs}$. Sketching some Bode plots might help with your explanation.

2. It is difficult to build inductors on chips, so circuit designers have come up with clever substitutes including the circuit in Figure 1, which is called a gyrator. Calculate Z_{th} for the gyrator and draw an equivalent circuit which has the same Z_{th} but only uses passive components. Express your answer in terms of C and A.

2 Warmup Problem 2 – Due Tues of 2nd Dynamics Week

1. Use open circuit time constants to estimate the bandwidth of the cascade of two common emitter amplifiers pictured in Figure 2. Unlabeled components dont matter for the analysis. What capacitance dominates the bandwidth?

3 Lab Introduction

In this lab you will simulate amplifiers, measure their frequency and step responses, and compare them to various analytical models The learning goals are listed below:

- See the full frequency response of an amplifier and appreciate its complexity
- Understand how well the Miller approximation and exact models frequency models work
- Observe the effect common parastiics that matter at high frequencies
- Mitigate the Miller effect using a Cascode
- Get practice calculating open circuit time constants

4 Common Emitter Frequency Response

1. Assume the row-to-row capacitance of your breadboard is 2pF.
2. Build two common emitter amplifiers with gains of 120, collector currents of 1mA and supply voltages of 15V. Use the same design for both (i.e.: same R_c, R_e, C_e, etc.), but add parasitic elements to your design to represent the two different breadboard layouts shown in Figure 1: one device has its terminals on adjacent rows while the other has the rows between terminals grounded. We will refer to the amplifier with layout A as amplifier A and the amplilfier with layout B as amplifier B.
3. Simulate a Bode Plot of a_v for each amplifier. Simulate to a frequency high enough to capture the second order pole and the feed-forward zero.
4. Build analytical models for both amplifier layouts using your values of row-to-row capacitance, information from the datasheet, and the full common emitter transfer function from lecture. Consider how the breadboad parasitics interact with C_π and C_μ.
5. Build yet more analytical models for both amplifier layouts using the Miller approximation instead of the exact transfer function.
6. Compare your data and your models by making Bode plots with the sets of data listed below overlaid. Comment on the accuracy of the models and the difference between the layouts.
   (a) simulated data from amplifier A and simulated data from amplifier B
   (b) simulated data from amplifier A, full transfer function model of amplifier A, and Miller model of amplifier A
   (c) simulated data from amplifier B, full transfer function model of amplifier B, and Miller model of amplifier B
7. Simulate the step responses of both amplifiers and explain their features (time constants, initial values, etc.) using your analytical models. How can you measure a step response when your input is AC coupled? Does the amplifier step response appear to be first or second order? Does the feed-forward zero appear in the step response?
8. Simulate r_{in}, r_{out} and V_{SW} of amplifier B.

Required Data: designs for your amplifiers, Bode plots listed above, one paragraph of discussion for each Bode plot, step response traces, answers to questions about step response

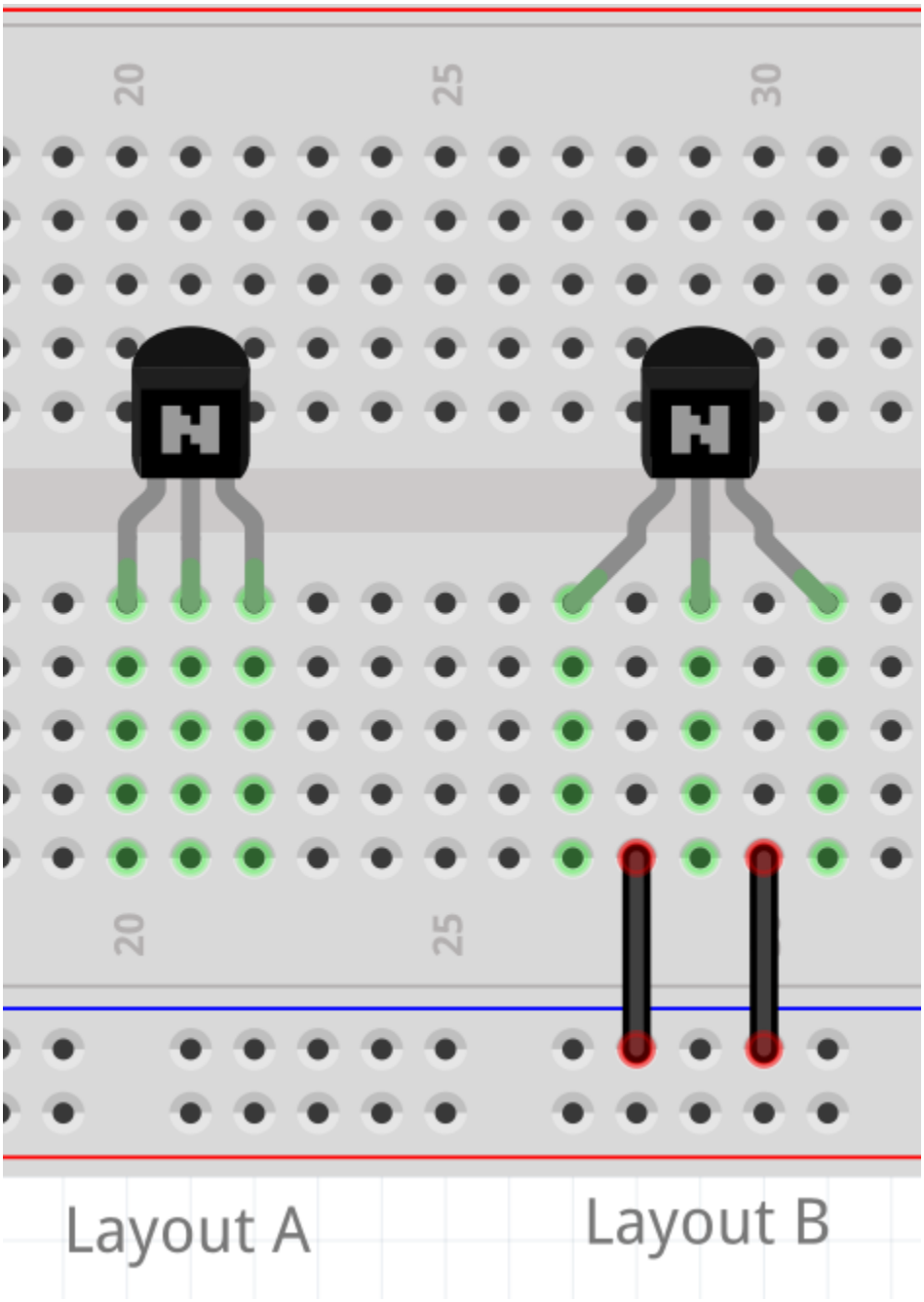

Figure 3: Different layouts for transistors.

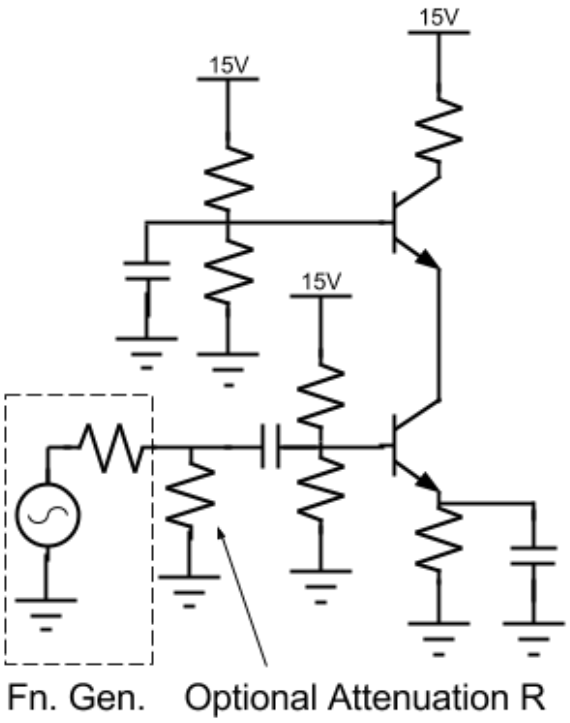

Figure 4: A sample design for a cascode amplifier.

5 Compare Cascode Amplifier Measurements to OCTC

Design a cascode amplifier using the reference design pictured in Figure 4 such that it has a gain of 120 and collector current of 1mA. Use the same R_c, R_e, C_e etc. as the common emitters in the last section. Add parasitics as if you are using layout B for the NPN devices. One explicit challenge of the lab is deciding what the bias voltage of the common base stage's base should be. Another challenge is applying open circuit time constants to the circuit in order to get an accurate prediction of the bandwidth of the circuit. A third is that this design is sometimes unstable, remove the capacitor on the common base's base if you have stability issues (which you can only see with transient simulations).

You must start this lab by making hand calculations which predict the amplifier specifications and bandwidth. These hand calculations should include calculations of open circuit time constants and short circuit time constants. After that you should simulate your design to make sure those component values work in simulation. Finally, you must extract r_{in}, r_{out}, a Bode plot of a_v and a step response for your Cascode from simulations.

Plot bode plots of simulated and OCTC analytical a_v on the same axis and justify any differences between them. The expectation in this lab is that you will refine your design and models until you get fairly good agreement (OCTC may be off my as much as 50% in the worst case, but you should do better than that).

Compare the corner frequencies and V_{SW} of amplifier B wtih your cascode amplifier and comment on the design tradeoffs between the two circuit topologies.

Required Data: Schematic of cascode amplifier, values for r_{in}, r_{out} and V_{SW}, the bode plot requested above, some OCTC calculations, comparison between cascode and common emitter