

# E151 Lecture 10 – Emitter Follower and Multistage

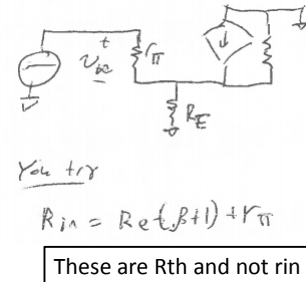
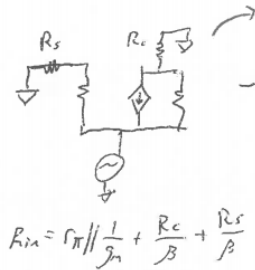
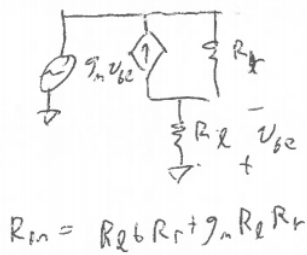
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## Disclaimer

These are notes for Prof. Spencer to give the lecture, they were not intended as a reference for students. Students asked for them anyway, so I'm putting them up as a courtesy. Remember that they are not intended as a substitute for attending lecture.

## Small Signal Patterns – repeat just in case

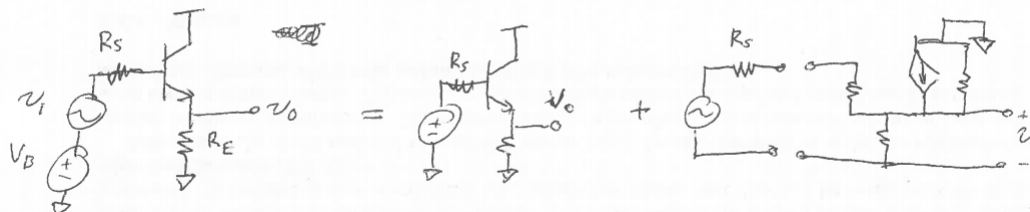
- We've just seen two common small signal models that are used a lot
- Here are more, can analyze fast if you understand / memorize
  - Thevenize aggressively, can remove from circuit
- Watch for variations: dividers to vbe, parallel stuff, ro, care w/ signs.



## Emitter Follower (Common Collector)

- We don't yet have the ability to generate a small rout
- Need a new amplifier topology. I do rin, they do av, I do rout
- rin follows same patters as CE w/ degen, rout is a new pattern (1/gm)

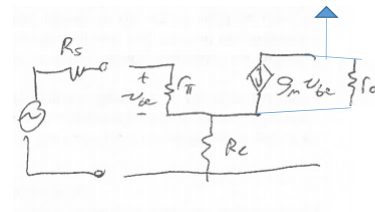
→ Emitter follower! ←



# rin

- Same pattern as CE with degen

$$\begin{aligned}
 v_{be} &= i_t r_{\pi} \\
 \text{KCL: } i_t &= \frac{v_o}{R_E} + \frac{v_o}{r_o} - g_m v_{be} \\
 &= v_o \left( \frac{1}{R_E} + \frac{1}{r_o} \right) - g_m r_{\pi} i_t \\
 i_t (\beta + 1) &= v_o / (R_E \parallel r_o) \\
 v_o &= i_t (\beta + 1) R_E \parallel r_o \\
 v_t = v_{be} + v_o &= i_t (r_{\pi} + (\beta + 1)(R_E \parallel r_o)) \\
 R_{in} = r_{\pi} + (\beta + 1)(R_E \parallel r_o) &\approx \beta R_E
 \end{aligned}$$



## Exercise: you find av

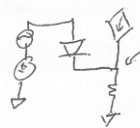
- Gain of 1 isn't very high, level shift is nice interpretation

Calc Av  $v_o = i_t (\beta + 1)(R_E \parallel r_o)$  from above

$$A_v = \frac{(\beta + 1)(R_E \parallel r_o)}{r_{\pi} + (\beta + 1)(R_E \parallel r_o)} v_i \quad \text{b/c } i_t = v_i / R_{in}$$

$$\rightarrow A_v \approx 1$$

Let's look @ large signal to check this



$$v_E = v_B - 0.7$$

- Gain is 1, level shifted down
- Used to get DC voltages right
- $v_{BE}$  stays  $\approx 0.7$ , small sig captures changes

## rouT – a new small signal pattern (1/gm)

- Need to include Rs b/c not pure 1 directional
- Breaks our 2 port model a bit

calc  $R_{out}$

- Need to include  $R_s$  - start w/  $V_{be}$  this time!

$$i_b = \frac{V_b}{R_E} + \frac{V_b}{C_c} + \frac{V_b}{r_{\pi} + R_s} - g_m V_{be}$$

and  $V_{be} = -\frac{R_{\pi}}{r_{\pi} + R_s} V_b$

so  $i_b = V_b \left( \frac{1}{R_E} + \frac{1}{C_c} + \frac{1}{r_{\pi} + R_s} + \frac{g_m r_{\pi}}{r_{\pi} + R_s} \right)$

$$R_{out} = R_E \parallel r_o \parallel \left. \frac{r_{\pi} + R_s}{\beta + 1} \right\} \approx \frac{1}{\beta} + \frac{R_s}{\beta + 1} \approx \frac{1}{g_m}$$

- Backwards gain of  $\frac{r_{\pi}}{R_s + r_{\pi}}$  we ignore in 2 port model

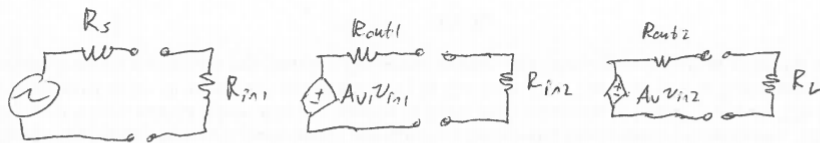
- say it's small --

- why  $\frac{1}{g_m}$ ? Voltage applied directly across gm control terminals & receives controlled current

↳ watch for this pattern!

## Multistage Picture and 2 Ports

- Large signal notes: separate bias points with AC coupling
- $r_{in\_tot} = r_{in\_1}$ ,  $r_{out\_tot} = r_{out\_3}$ ,
- $V_{SW,tot} = \min VSW \leftarrow$  Need to use FFT to tell if you violate VSW



- Capture interstage loading w/ voltage div btwn  $R_{in}$  &  $R_{out}$ !

$$A_{v,tot} = A_{v1} A_{v2} \frac{R_{in1}}{R_{in1} + R_s} \cdot \frac{R_{in2}}{R_{out1} + R_{in2}} \cdot \frac{R_L}{R_{out2} + R_L}$$

-  $R_L$  &  $R_s$  represent rest of world