E151 Lecture 8
Amplifier Design and Voltage Swing

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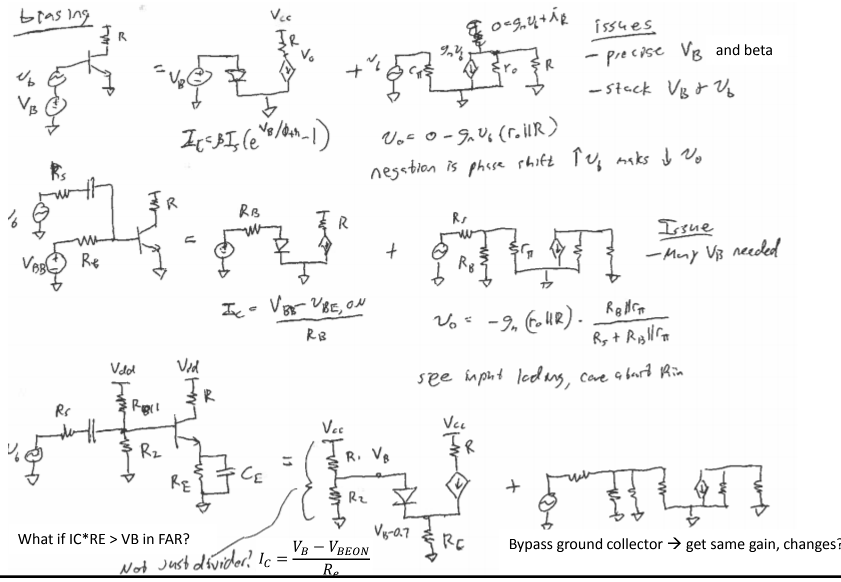
ENGR151

Disclaimer

These are notes for Prof. Spencer to give the lecture, they were not intended as a reference for students. Students asked for them anyway, so I'm putting them up as a courtesy. Remember that they are not intended as a substitute for attending lecture.

Built an Amplifier, Biasing Improvements

- Get to av, rin and rout indirectly
- Invoke voltage swing with final example
- We have been building up a sense of design specs for amps



Design Specifications for Amplifiers

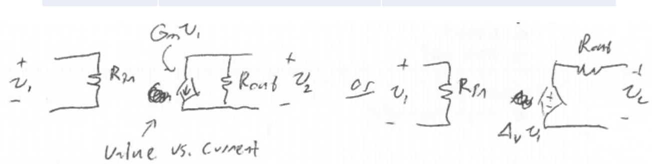
- Suggests a generalized 2 port model for amplifiers … no Z12, so easy

Symbol	Name	Calc
a_v	Voltage gain	dvo/dvi | out open
r_in	Input resistance	dii/dvi | out short
r_out	Output resistance	dio/dvo | in short
V_SW	Voltage swing	VO_MAX-VO_MIN
I_IN	Input bias current	Large signal I_IN
f_low	Low f -3dB corner	Measure for now

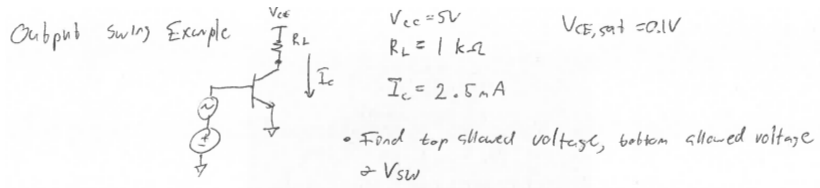
Sometimes care about a_i dio/dii | out short = beta

Fall straight out of small signal, **Must measure with power on!** (small sig. open/short, not big)

Must find nominal V_O and figure out allowed excursions
2*min(V_OMAX-V_O, V_OMIN-V_O)



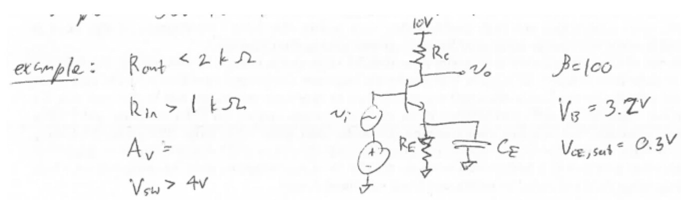
Output Swing Example

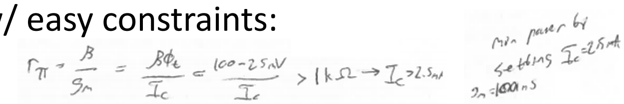


1. Find V_O = V_CC-I_C*R_L
2. If V_O down, when do we leave FAR? V_MIN = V_CE,SAT
3. If V_O up, when do we leave FAR? V_MAX = V_CC (cutoff)
4. Check at input: Av=gm*RL=100, so +2.5V V_O/2 is ~ 25mV @in

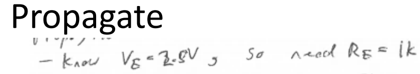
Approximate: get distortion before sat/cutoff → use FFT & 1-2V margin

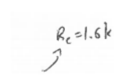
Design Process: Specs to I_C / R values



- Start w/ easy constraints:
  - Eg: 

  - Unusual, easy constraints are usually at output: V_SW or rout contraints
- Propagate





  - V_OMAX = 10V, V_OMIN=V_E+V_CE,SAT=2.8V, ½ way max swing → V_O=6.4V