



Figure 1: An op-amp model suitable for calculating the maximum capacitive load for the op-amp.

## 1 Warm Up Problem

Maximum capacitive load is a common specification on op-amp datasheets. When the capacitive load of an op-amp is too high, the op-amp can become unstable. In this figure,  $C_l$  is the load capacitance,  $r_{out}$  is the op-amp's output impedance and  $a_{ol} = a_{dc}/(\tau s + 1)$  is the op-amp's open loop gain. Find an expression for the maximum capacitive load of the op-amp. Assume  $R_1 + R_2 \gg r_{out}$  and  $r_{out}C_l \ll \tau$ . Express your solution in terms of  $a_{dc}$ ,  $\tau$ ,  $r_{out}$  and the desired feedback factor  $f = R_2/(R_1 + R_2)$ .

## 2 Lab Introduction

In this lab you will finalize the design of your operational amplifier and explore the stability of the amplifier.

The learning goals are listed below:

- See how many analog subcircuits can come together into a more complex analog system.
- Appreciate the power of op-amp compensation.

## 3 Build Your Op-Amp

1. Design a (optionally degenerated) common emitter gain stage for your operational amplifier.
  - (a) It must operate on the same 12V voltage rail as your differential and output stages and it must operate when DC coupled to the output of the differential stage.
  - (b) Bias the amplifier output so that it can be DC coupled to the class AB output stage on your board.
  - (c) The amplifier should have a gain of at least 10, higher is better.
  - (d) A PNP device may be easier to DC couple to your NPN differential stage.
  - (e) Be careful of loading effects: don't load the differential stage or let yourself be loaded by the output stage.
2. Test your gain stage on its own, be sure it is working with a DC coupled input voltage.
3. Complete your op-amp by connecting one of the outputs from your differential amplifier to the input of your gain stage and connecting the output of the gain stage to the class AB output stage. Add a 10nF compensation capacitor to the gain stage.

## 4 Assess Your Stability

1. Is the amplifier open-loop stable? If not, improve your bypassing, biasing and compensation. Is it stable without the compensation capacitor?
2. Measure a Bode plot of your open loop gain. You may need to attenuate (and/or capacitively couple) your test input to do so.
3. Configure your op-amp for unity gain feedback. Is it stable? Does this match your Bode plot. If it is not unity gain stable, then configure it for non-inverting gain and increase the attenuation of the feedback factor until it become stable.
4. Measure a step responses for your closed-loop op-amp both with small input amplitude (so you get a linear response) and large input amplitude (so you observe slewing). What is your settling time constant, slew rate and steady state error? Do these agree with analytical predictions?
5. Find the maximum capacitive load of your op-amp. Does your maximum capacitive load make sense when you compare it to your Bode plot and to the design of your output stage?

**Required Data:** Gain stage design, Gain stage proof of functionality (eg: input/output scope trace), scope traces showing open loop stability/instability, Bode plot of open loop gain, proof of stability and functionality in feedback (specifying whether it's unity gain or with some other feedback factor), large and small input step responses from closed loop amplifier, measured time constant, slew rate and steady state error, maximum capacitive load and proof of stability or instability under that load, analytical transfer functions and analytical comparisons for every extracted number.