1. The amplifier pictured above is called a folded cascode amplifier. One aside that you don’t need for the problem: the current sources in this amplifier are usually implemented as current mirrors, and we’ll be studying how to incorporate them into amplifiers soon.

(a) Draw a small signal model for it and compare the small signal model to the cascode amplifier we studied in class (which is referred to as a telescopic cascode amplifier).

(b) Calculate the voltage swing of this folded cascode. Both npn and pnp transistors have a turn-on voltage of $V_{be, on}$ and a saturation voltage of $V_{ce, sat}$. Assume the current at the emitter of the NPN is selected to maximize output swing.

2. Digital gates, like the inverter above, operate their transistors in a mix of operating regions. When the input voltage is transitioning from low to high, the NMOS device starts in cutoff, enters saturation as the input voltage rises above $V_t$, and finally ends in linear operation as the output voltage falls below the input voltage.

(a) What regions of operation does the PMOS device pass through during a low to high transition at the input and at what combinations of $V_{in}$ and $V_{out}$ does it switch between those regions? You may assume that the edge rate at the input is similar to the edge rate at the output; neither $V_{in}$ nor $V_{out}$ looks like an ideal step compared to the other quantity.

(b) What capacitance is seen at the input (i.e.: what is the sum of all capacitors with one terminal attached to the in node) during each combination of NMOS/PMOS device states? Assume both devices have length $L$ and capacitance density $C_{ox}$. 

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**Figure 1:** A folded Cascode amplifier.

**Figure 2:** An inverter.