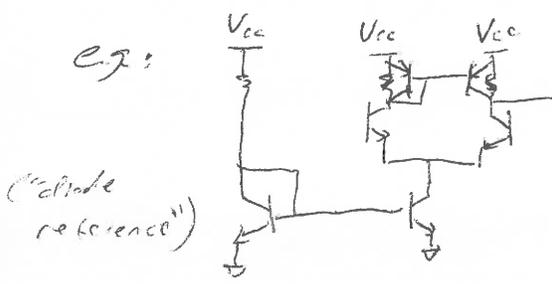


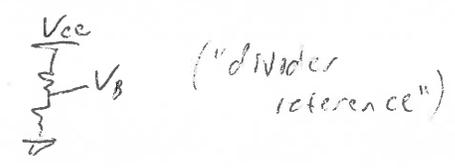
<p>Diff amp review</p> <ul style="list-style-type: none"> - Degeneration - Extends input range - Equalizer - 160 gm @ 2/2 	<p>Sensitivity & Current mirrors</p> <ul style="list-style-type: none"> - Mirror current varies w/ supply - Define sensitivity - Widlar Reference 	<p>Supply Invariant Bias currents</p> <ul style="list-style-type: none"> - Principle: make a current from what you care about - V_{be} reference - self-biasing & startup 	<p>Bandgap References</p> <ul style="list-style-type: none"> - Why ~ regulators - CTAT & PTAT & Curcon - Quick implementation - $V_{out} = 1.26 V$
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We've been looking @ amplifiers biased & loaded by current mirrors



- Current source biasing enables high gain & high swing active loads
- Enables high CMRR diff amp

Before we biased w/ voltage dividers



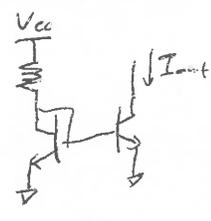
- ISSUE: ~~supply~~ bias point very sensitive to supply voltage
- ↳ voltage input range on op-amps often spans 10s of V_{cc}

Want to quantify how bad this is, do so w/ a measure called sensitivity

$$S_{\text{of } Y \text{ to } X} \equiv S_X \equiv \lim_{\Delta X \rightarrow 0} \frac{\Delta Y/Y}{\Delta X/X} = \frac{X}{Y} \frac{\partial Y}{\partial X}$$

↖ fractional change of Y w/ % X

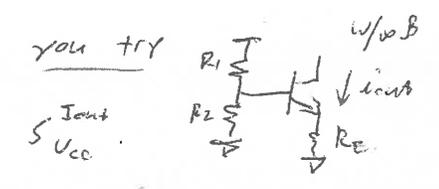
eg: diode reference in simple mirror



$$S_{\frac{I_{out}}{V_{cc}}} = \frac{V_{cc}}{I_{out}} \frac{\partial}{\partial V_{cc}} \left[\left(\frac{\beta}{\beta+2} \right) \cdot \left(\frac{V_{cc} - V_{be,on}}{R} \right) \right]$$

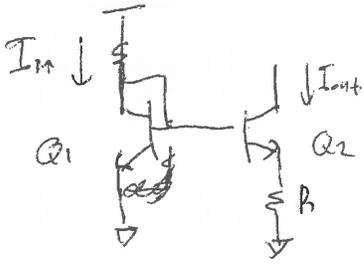
$$= \frac{\beta}{\beta+2} \cdot \frac{V_{cc}}{R} \cdot \frac{1}{\left(\frac{\beta}{\beta+2} \right) \left(\frac{V_{cc} - V_{be,on}}{R} \right)}$$

$$\approx \frac{1}{\left(1 - \frac{V_{be,on}}{V_{cc}} \right)} \approx 1 \quad \text{very sensitive!}$$



$$S_{\frac{I_{out}}{V_{cc}}} = \frac{R_2}{R_1 + R_2} \cdot \frac{V_{cc}}{R_E} \cdot \frac{1}{\left(1 - \left(1 + \frac{R_1}{R_2} \right) \frac{V_{be,on}}{V_{cc}} \right)} \approx 1$$

Can make a mirror less sensitive to I_{in} using different V_{be}
 - eg Widlar reference current source



Interested in $I_{out}(I_{in})$

$$- V_{be1} = V_{be2} + I_{out} R \cdot \frac{\beta}{\beta+1}$$

$$- I_{s1} e^{V_{be1}/\phi_T} = i_{b1} \rightarrow V_{be1} = \phi_T \ln \frac{i_{b1}}{I_{s1}}$$

$$- \phi_T \ln \frac{I_{in}}{I_{out}} \approx I_{out} R$$

• Note ϕ_T assume 0.7V here

• Need on $1/\beta$ for V_{be} (bug last lecture)

- Temperature sensitive, so lab simulations solve exactly

- But relatively insensitive to I_{in} ~ logarithmically compressed

- Called current source for that reason & not current mirror

Sensitivity ~ $\phi_T \frac{\partial}{\partial V_{cc}} \ln \frac{I_{in}}{I_{out}} = R \frac{\partial I_{out}}{\partial V_{cc}}$

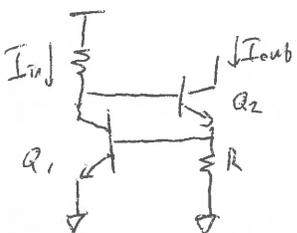
$$\phi_T \left(\frac{1}{I_{out}} \frac{\partial I_{in}}{\partial V_{cc}} - \frac{I_{in}}{I_{out}} \frac{\partial I_{out}}{\partial V_{cc}} \right) = R \frac{\partial I_{out}}{\partial V_{cc}}$$

$$\frac{\partial I_{out}}{\partial V_{cc}} = \left(\frac{1}{1 + \frac{I_{out} R}{\phi_T}} \right) \cdot \frac{I_{out}}{I_{in}} \cdot \frac{\partial I_{in}}{\partial V_{cc}}$$

$$S_{V_{cc}}^{I_{out}} = \frac{V_{cc}}{I_{out}} \cdot \frac{\partial I_{out}}{\partial V_{cc}} = \left(\frac{1}{1 + \frac{I_{out} R}{\phi_T}} \right) \cdot S_{V_{cc}}^{I_{in}} \approx \left(\frac{1}{1 + \frac{I_{out} R}{\phi_T}} \right)$$

1k
 w/ 1mA I_{out} & $R=10k$
 (with V_{cc} !)
 1/40 better!

You try V_{be} reference



$$I_{out} = V_{be1}/R$$

$$= \frac{\phi_T}{R} \ln \frac{I_{in}}{I_{s1}}$$

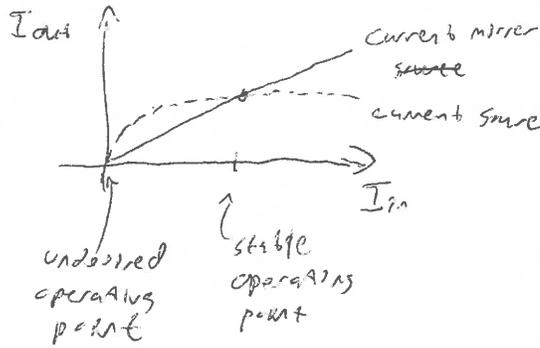
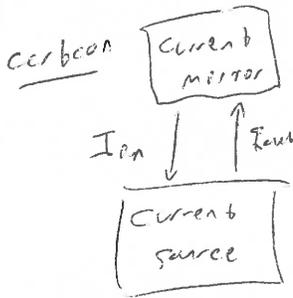
$$\frac{\partial I_{out}}{\partial V_{cc}} = \frac{\phi_T}{R} \cdot \frac{I_{s1}}{I_{in}} \cdot \frac{\partial V_{be1}}{\partial V_{cc}} = \frac{1}{R I_{s1}} \cdot \frac{\partial I_{in}}{\partial V_{cc}}$$

$$S_{V_{cc}}^{I_{out}} = \frac{\phi_T}{R} \cdot \frac{I_{s1}}{I_{in}} \cdot \frac{\partial I_{in}}{\partial V_{cc}} = \frac{V_{cc}}{I_{out}} = \frac{\phi_T}{V_{be1,ref}} \cdot S_{V_{cc}}^{I_{in}}$$

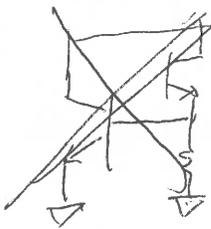
- Note: pretty good vs V_{cc}
 $S = \frac{26mV}{700mV} = 3.7\%$

b/c $I_{out} R = V_{be,ref}$
 & $\frac{V_{cc}}{I_{in}} \frac{\partial I_{in}}{\partial V_{cc}} = S_{V_{cc}}^{I_{in}}$

Further improve supply in sensitivity w/ self-biasing (no dependence on $V_{cc} - R$ at all)



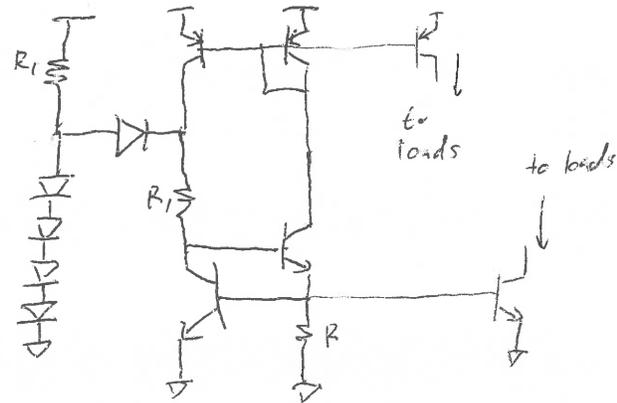
- Need a startup circuit to kick to correct op. pt.



- 4 diode drops vs. 3 guarantees current injection @ startup

until $V_{R1} = V_{be,on}$

- bias Rx rev. biases diode $R1 \cdot I_{in} > 2V_{be,on}$



Look for corners

Temperature Insensitivity

- measured w/ Temperature coefficient

$$TC^{I_{out}} = \frac{1}{I_{out}} \frac{\partial I_{out}}{\partial T}$$

- fractional change in output per degree C (not sensitivity bc don't care about fractional temp)

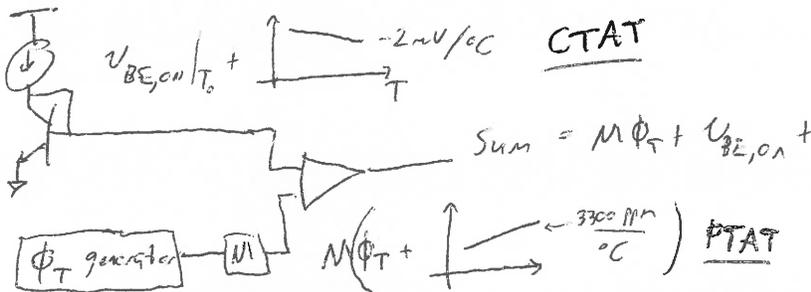
- Shows up a lot in resistors (~ 1000 ppm/°C) $(\frac{1}{R} \frac{\partial R}{\partial T})$

- Various tricks to adjust temperature in self-biased circuits

- $V_{be} \propto T$ & $R_T \propto T$, so tend to cancel in V_{be} current references. V_{be} is $\propto T$

- But sometimes want supply & temp invariant voltages (eg: regulator reference)

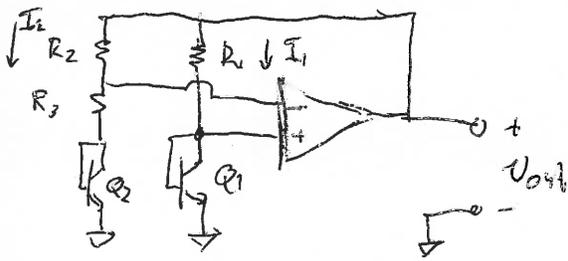
- so we'll look @ bandgap reference - an iconic reference



- Cancel out temp dependence!

$(kT/q) \sim \text{slope} = \frac{k}{q}$; $V_{be,on} = \frac{\Phi_T \ln(I/I_s)}{q}$ related to I_s

Band gap reference does this in a very literal way



- OP-amp forces $V_{R1} = V_{R2}$

- so $\frac{I_1}{I_2} = \frac{R_2}{R_1}$

- ϕ_T generates ΔV_{be} can get it from ΔV_{be}

$$V_{R3} = \underbrace{V_{be1} - V_{be2}}_{\Delta V_{be}} = \phi_T \ln \frac{I_1}{I_{S1}} - \phi_T \ln \frac{I_2}{I_{S2}} = \phi_T \ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}}$$

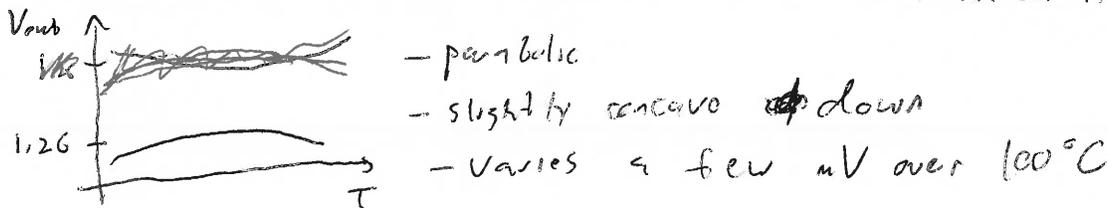
• same current in R_2 & R_3 , so $V_{R2} = \frac{R_2}{R_3} V_{R3}$

Finally, do KVL, $V_{out} = V_{be2} + V_{R2} + V_{R3}$

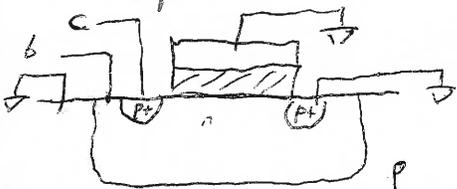
$$= V_{be2} + \left(1 + \frac{R_2}{R_3}\right) \phi_T \ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}}$$

$$= V_{be2} + M \phi_T \quad \text{where } M = \left(1 + \frac{R_2}{R_3}\right) \ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}}$$

- Generally have an output $V_{BG} = 1.26V$ ~ tenuous relationship w/ band gap of Silicon in eV



- Implement in CMOS using polysilic substrate BST



PMOS device