We've been looking at amplifiers biased and loaded by current mirrors.

**Example**:

![Current Source Biasing](image)

Current source biasing enables high gain and high supply active loads.

Before we biased w/ voltage dividers, we had:

\[ \frac{V_{cc}}{3} - V_b \] ("divider reference")

**Issues**:

- Gains point very sensitive to supply voltage.

- Voltage input range can change often spans 10s of V.

To quantify how bad this is, do so w/ a measure called sensitivity:

\[ S = \lim_{A \to 0} \frac{\Delta Y}{Y} \approx \frac{dy}{y} \]

**Example**:

**Divider Reference in Simple Mirror**

\[ S = \frac{V_{cc}}{3} \left( \frac{V_{cc}}{V_{cc} - V_{th, en}} \right) \]

\[ \Delta I_{in} \approx \frac{R_2}{R_1 + R_2} \frac{V_{cc} - V_{th, en}}{V_{cc}} \]

\[ V_{cc} \approx \frac{R_1}{R_2 + R_1} \frac{V_{cc} - V_{th, en}}{V_{cc}} \]

\[ S = \frac{1}{1 + \frac{V_{th, en}}{V_{cc}}} \approx 1 \] very sensitive!
can make a sensor less sensitive to $I_{in}$ using different $V_{be}$
- eg wider reference current source

- Interested in $I_{out} (I_{in})$

- $V_{be1} = V_{be2} + I_{out} R - \frac{I_{in}}{\phi_T}$
- $I_{sat} e^{V_{be1}/qT} = I_{sat} \Rightarrow V_{be1} = \phi_T \ln \frac{I_{in}}{I_{sat}}$

- $\phi_T \ln \frac{I_{in}}{I_{out}} \approx I_{out} R$

- Feedback, so let transistors solve exactly
- But relatively insensitive to $I_{in}$ - logarithmically compressed
- Called current source for that reason - not current mirror

- Sensitivity $\approx \phi_T \frac{\partial}{\partial V_{cc}} \ln \frac{I_{in}}{I_{out}} = R \frac{\partial I_{out}}{\partial V_{cc}}$

- $\phi_T \left( \frac{i}{I_{out}} \frac{\partial I_{in}}{\partial V_{cc}} - \frac{I_{in}}{I_{out}} \frac{\partial I_{out}}{\partial V_{cc}} \right) \approx R \frac{\partial I_{out}}{\partial V_{cc}}$

- $\frac{\partial I_{out}}{\partial V_{cc}} = \left( \frac{i}{1 + \frac{I_{in}}{\phi_T}} \right) \frac{I_{out}}{I_{in}} \frac{\partial I_{in}}{\partial V_{cc}}$

- $S_{V_{out}} = \frac{V_{out}}{I_{out}} \frac{\partial I_{out}}{\partial V_{cc}} = \left( \frac{1}{1 + \frac{I_{in} R}{\phi_T}} \right) \frac{\partial I_{in}}{I_{in}} \frac{V_{cc}}{V_{out}} \approx \left( \frac{1}{1 + \frac{I_{in} R}{\phi_T}} \right) \frac{V_{cc}}{V_{out}}$

- $\frac{1}{I_{in}} \frac{V_{out}}{V_{be}}$ reference

- $I_{out} = V_{be} / R$

- $\frac{\partial I_{out}}{\partial V_{cc}} = \frac{\phi_T}{R} \frac{I_{in}}{I_{sat}} \frac{\partial I_{in}}{\partial V_{cc}}$

- $\frac{\partial I_{out}}{V_{cc}} = \frac{\phi_T}{I_{sat}} \frac{I_{in}}{I_{out}} \frac{\partial I_{in}}{\partial V_{cc}}$

- Note: Pretty good vs $V_{be}$

- $S_{V_{out}} = \frac{2.6 \text{mV}}{300 \text{mV}} = 7.7 \times 10^{-3}$
Further improve supply sensitivity w/ self-biasing (no dependence on $Vcc-R$ et al)

- Need a startup circuit to kick to correct op pt.

- 4 diode drops vs. 3 generators current injection @ startup

  $\mathit{U_{R1}} = \mathit{U_{B1,0}}$

- big Rx rev. bias is $V_{R1} \mathit{I_{1}} = 2 \mathit{U_{B1,0}}$

- Look for corners

- Temperature Insensitivity

  - measured w/ temperature coefficient $TC = \frac{1}{I_{bias}} \frac{2 I_{bias}}{d}$

  - fractional change in output per degree C (not sensitivity so don't care about fractional temp)

  - shows up a lot in resistors ($\approx 1000 \text{ ppm/oc}$)

= Various tricks to adjust temperature in self-biased circuits

- Use $v_{BE} \propto T \propto 1/T$, so tend to cancel in current references $U_{BE}$

- But sometimes want supply or temp invariant voltages ($V$-regulator reference)

- so we'll look @ bandgap reference - an iconic reference

  - $V_{BE,0}(T) + \mathit{2 mV}/\mathit{oc}$ CTAT

  - Sum = $M \Phi_T + V_{BE,0} + \frac{T}{T_e}$

  - Cancel out temp dependence!

  $k_T = \frac{k}{2} \approx \text{slope} = \frac{1}{T}$ - $V_{BE,0}$ related to $I_T$
Band gap reference does this in a very literal way:

\[
-o p-a m p f o r c e s \quad U_{R1} = U_{R2}
\]

\[
- \quad so \quad \frac{I_1}{I_2} = \frac{R_2}{R_1}
\]

\[
- \quad \Phi_T \quad g e n e r a t i o n \quad C a n \quad s e t \quad i t \quad f r o m \quad \Delta V_{be}
\]

\[
\begin{align*}
U_{R3} &= U_{be1} - U_{be2} = \Phi_T \ln \frac{I_1}{I_{S1}} - \Phi_T \ln \frac{I_2}{I_{S2}} = \Phi_T \ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \n
\end{align*}
\]

\[
- s o m e \quad c u r r e n t \quad i n \quad R_2 \quad \Rightarrow \quad U_{R2} = \frac{R_2}{R_1} U_{R2}
\]

Finally, do KVL:

\[
V_{out} = V_{be2} + U_{R2} + U_{R3}
\]

\[
= V_{be2} + (1 + \frac{R_2}{R_3}) \Phi_T \ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}}
\]

\[
= V_{be2} + M \Phi_T \quad \text{where} \quad M = (1 + \frac{R_2}{R_3}) \ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}}
\]

- Generally have an output \( VBG = 1.26 \text{V} \) - tension relationship w/ band gap of silicon in eV

- Implement in CMOS using parasitic substrate BST PMOS device

- Varies a few mV over 100°C