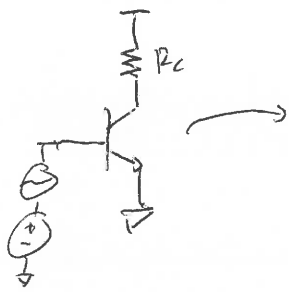
Lec 19 - Current Mirror

MOS Bias Points & V_{ov}	Current Mirror Biasing (large signal)	Current Mirror Gain (small signal)	Current Mirror bandwidth (dynamics)	Higher impedance & higher swing
	- Basics ~kVL, error - Load lines - CMFB issues	- Small sig model for CE - Impedance of diode		- Cascoded mirrors - Wilson mirrors? - High swing MOS mirror?
		4.2.{1-3,5}	7.3.5	

~~Current Mirrors~~

- We've been using resistive loads for our amps & I've promised a change



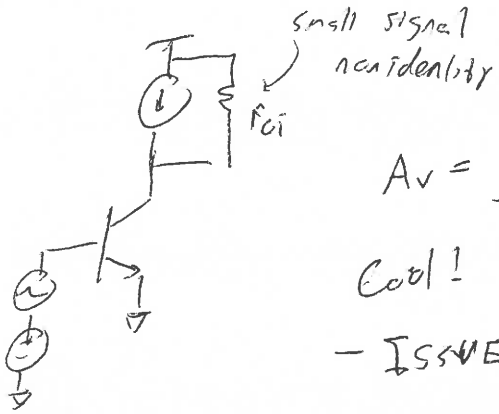
- $A_v = g_m (R_C \| r_o)$ ← Feels like R_C limits gain
  $A_{v,max} = g_m r_o$

- But making R_C really big crashes V_o
  $V_o = V_{cc} - I_C R_C$ ← need big I_C @ fixed R_C

- Merging equations reveals $A_v = \Delta V / \phi_{th}$

- Our swing/DC operating point is coupled to our gain, limits performance

- Fix this by biasing w/ current source

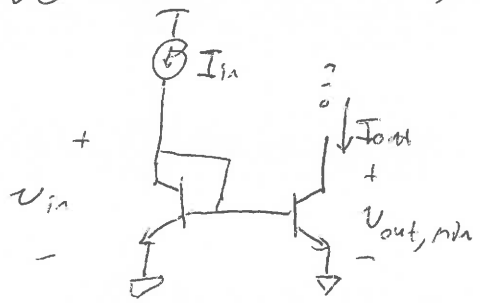


$A_v = g_m (r_o \| r_{oi})$ & unrelated to DC value of V_{out} (both in FAR)

Cool!

- ISSUE 1: How to make
- ISSUE 2: What's large signal V_o

We make it using current mirrors (seen on PSET)



"simple mirror"

– Take a closer look @ analysis today

– Basic idea $i_E = T(v_{be})$ on left

$i_C = T^{-1}(v_{be})$ on right

$= T(T^{-1}(i_C))$

– Figures of merit v_{in} – want minimized

$v_{out,min}$ – minimize to max output swing

ε – I_{out}/I_{in} ~ can have error

R_{out} – small signal output impedance (→ gain)

– Must evaluate different mirrors @ same I_C b/c affects r_o, v_{in}

In simple mirror draw KVL loop through v_{be} drops

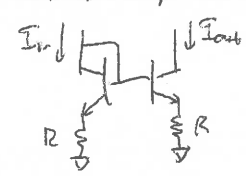
$v_{be1} = v_{be2}$ ← All mirrors have KVL @ heart

← surprisingly useful: translinear ckt, etc.

- $I_{b1} = I_{s1}(e^{v_{be1}/\phi_{th}} - 1)$ & $I_{b2} = I_{s2}(e^{v_{be2}/\phi_{th}} - 1)$

- Current gain if $I_{s1} \neq I_{s2}$, o/w same

You try
– KVL loop here

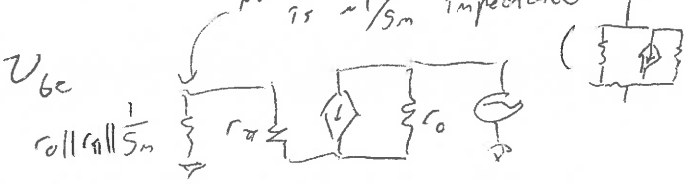


$$\left.\begin{aligned} I_{in} &= I_{b1} + I_{c1} = (\beta+1) I_{b1} \\ I_{out} &= \beta I_{b1} \end{aligned}\right\} \quad \varepsilon = \frac{\beta}{\beta+2}$$ ~ small error b/c of base current

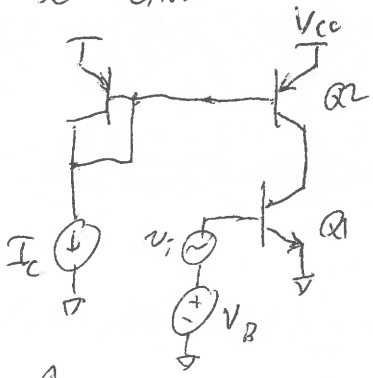
- $v_{out,min} = v_{ce,sat}$ & $v_{in} = v_{be}$

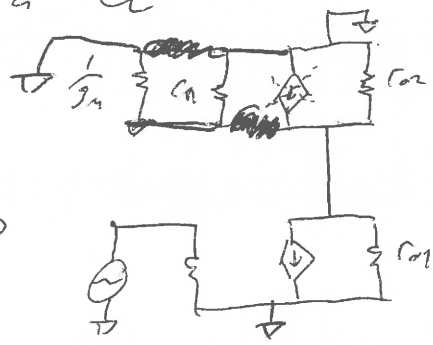
- $R_{out} = r_o$

Note diode connected device is ~ $1/g_m$ impedance



Use this as a load on a CE





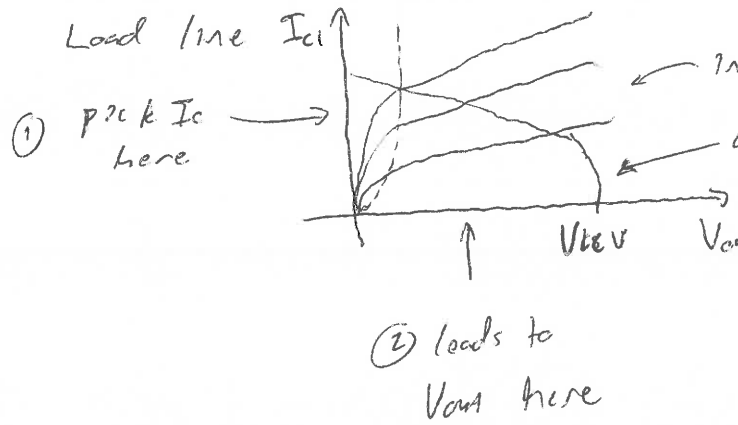
- $A_v = g_m \cdot (r_{o1} \| r_{o2})$
  - ~1000 for BJT
  - ~high!
- V_{sw} potentially $V_{CC} - 2V_{CE,sat}$ (or centered V_{out})

- sets our bias current, nicely
- Need to pick V_B so in FAR
- Still don't know DC V_{out} (1 min) so don't have upper bound on V_B

You try

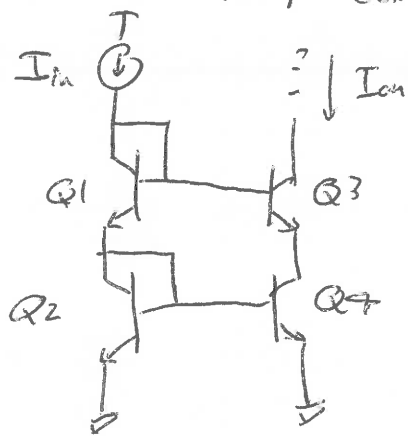
A_v of I_{src} loaded cascode

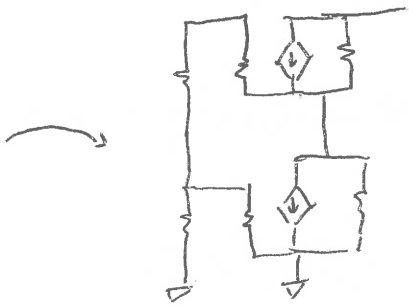
- Find V_{out} using load line analysis (qualitative understanding) or simulator (exact number)
  - ~ large signal problem w/ many exponentials not tractable, little insight



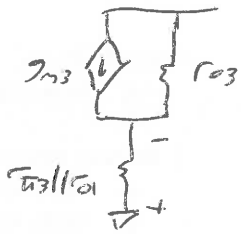
- Actually simulate & make this graph when designing active loads

- Simple mirror implies there are non-simple mirrors...
  - One very common mirror is the cascoded mirror





Assume $1/g_m$ small



Same as cascode or right/left pattern

$R_{out} \approx r_{\pi3} + r_{o3} + g_{m3} r_{\pi3} r_{o3}$

$\approx \beta r_{o3}$

- surprisingly, high by 2x b/c mirror Q2/Q4 forces $I_{b3} = I_{E3}$

$v_{in} = 2 \cdot v_{be,on}$

$v_{out,min} = 2 \cdot v_{CE,sat}$

- Improved R_{out} is good, but get worse ε

$I_{E1} = I_{c2} + \frac{2 I_{c2}}{\beta}$ ← Note KVL used to get $I_{B2} = I_{B4}$

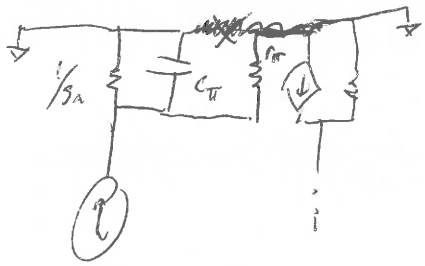
$I_{IN} = I_{E1} + I_{c3}/\beta$ ← Assumes $V_{CE4} \approx V_{CE1}$ by following diode drops around loop

~ Note $I_{c3} = \frac{\beta}{\beta+1} I_{c2}$

$I_{IN} = I_{c2}\left(1 + \frac{2}{\beta} + \frac{1}{\beta+1}\right)$

$I_{out} = \frac{\beta I_{c2}}{\beta+1}$ } ~ $\varepsilon = \frac{\beta}{\beta+1} \frac{1}{1 + \frac{2}{\beta} + \frac{1}{\beta+1}}$

- Dynamics
  - C_μ shorted b/c of diode connection
  - C_π sees diode ~ so looks into $1/g_m \| r_\pi$



pole @ $\approx \frac{g_m}{C_\pi}$

zero @ $\frac{2 g_m}{C_\pi}$

- Very approximate, OCTC caveats
- key point is that it's usually very fast, not the issue