Channel Length Modulation

- Region at end
  - Clr example

- Training you guys to go get semiconductor jobs or other electrical eng. position

- Requires fluency in BJT models (you guys OK) & a few MOSFET models

- Also, you'll probably mostly use FETs in your career

Channel Length Modulation

\[ I_{D, sat} = \frac{M_{n} C_{ox}}{L} \left( V_{GS} - V_{T} \right)^{2} \left( 1 + V_{DS} \right) \]

- \( q \cdot \mu \cdot n \)

- What's this? causes \( \frac{d}{dV_{DS}} \) vs \( V_{DS} \)

- Small \( \lambda \) channel pinches off \( \approx \) channel length

- \( \lambda \) is very small \( \lambda \) channel length compared to pinch off \( \approx \) channel length

- Shows up in BJT \( 6f \) vs \( 6f \frac{1}{Q_{base}} \times \frac{1}{N_{A}C_{ox}} \times \frac{1}{V_{DS}} \), \( V_{BASE} \) is set by BC depletion region. 
Backgate Effect

- We've asserted \( Q_C = \text{Cov} \cdot W_L \cdot (V_{GS} - V_T) \) or likened it to a plate cap
- Kind of weird...why this \( V_T \) tax before accumulating channel charge
- \( \Rightarrow \) pay \( V_T \) to create the channel...field lines terminate on bulk
- \( \Rightarrow \) Assumes no bulk voltage...need to examine \( V_T \)

\[
V_T = \phi_m + 2\phi_e + \frac{Q_b}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} \\
\text{possible charge stuck in gate}
\]

\[
= \phi_m + 2\phi_e + \frac{Q_b}{C_{ox}} + \frac{Q_{ss}}{C_{ox}} + \frac{Q_{bc} - Q_b}{C_{ox}}
\]

\[
\Rightarrow \quad V_T \quad \text{w/ } 0 = V_{BS}
\]

\[
= V_{TS} + \left( \sqrt{2\phi_e - V_{BS}} - \sqrt{2\phi_e} \right) \\
\text{mostly we have } V_{SB} \text{, switch near } V_s \uparrow \text{ w/ } V_{BS} \text{ @ } 0 \Rightarrow V_T \uparrow \rightarrow I_D \downarrow
\]

Can cause some large signal surprises...but manifests like crazy in small signal

\[
\text{\( g_m = \frac{\partial I_D}{\partial V_{BS}} \) = } \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \cdot \frac{\partial V_T}{\partial V_{BS}} = \frac{1}{2} \frac{\partial V_{GS} - V_T}{2 \sqrt{2\phi_e - V_{BS}}}
\]

\[
= 9 \cdot \frac{1}{2 \sqrt{2\phi_e - V_{BS}}} \frac{V_T}{3} = \text{called } \chi, \quad \text{ratio of } \frac{C_{ox}}{C_{j6}} \text{, small } 3/8 \text{ depletion under channel big}
\]

\[
\text{You say: } \quad \text{Exercise draw small signal cascade model if}
\]

\[
\text{upper device has extended base?}
\]
Expression for \( g_m \), kind of clunky, re-factor to find \( V_{GS} - V_T = V_{ov} \)

\[
I_D = \frac{1}{2} M_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad \text{and} \quad V_{ov} = V_{GS} - V_T = \sqrt{\frac{2I_D}{M_n C_{ox} \frac{W}{L}}} \quad \text{gate overdrive}
\]

\[
g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{M_n C_{ox} W}{L} (V_{GS} - V_T)
\]

\[
= \sqrt{2M_n C_{ox} \frac{W}{L} I_D} \quad \Rightarrow \quad g_m V_{ov} = 2I_D
\]

\[ \text{Example}\]

\[ \text{What should } V_B \text{ be for a given } I_D \text{ to have gain } A_V? \]

\[
A_V = -g_m R_0 = -2I_D R_0 \quad \frac{V_B - V_T}{V_B}
\]

\[ V_B = \frac{2I_D R_0}{A_V} + V_T \]

Speaks to basic biasing patterns in MOSFETs
- Gate always at least \( V_T \) above src. = reliably \( V_T + V_{ov} \)
- Drain set to stay in sat., so \( V_D < V_T \rightarrow V_D > V_T \)
- Use Irre to bias \( V_{GS} < V_T \)

\[ \text{Example: mos cascode}\]

\[
A_V = g_m \left( \frac{r_{oi} + r_{o2} + g_{m2} r_{oi} r_{o2}}{} \right)
\]

\[ V_{bi} = V_{ov1} + V_T \quad \text{pick to achieve desired } g_m \]

\[ V_{bi} = V_{ov2} + V_T \quad \text{usually just set to very saturated sat.} \]

\[ V_{ov} \text{ set by } V_{bi} + I_D \text{ ~not easy to set like BJT cascade} \]

\[ \text{No} \]
Modern transistors have a bunch of weird behaviors

**Velocity saturation**

- E field steeper if channel shorter, eventually e-hit speed limit
- collision don't allow net speed beyond $E_{\text{critical}}$

$$V_{ds} = \frac{m_n E_c}{1 + \frac{E}{E_c}} \quad \Rightarrow \quad I_D = \frac{m_n C_{ox}}{2 \left(1 + \frac{V_{ds}}{E_c}\right)} \frac{W}{L} \left(2(V_{gs} - V_T) - V_{ds}^2\right)$$

$$I_D = \frac{m_n C_{ox}}{2 \left(1 + \frac{V_{gs} - V_T}{E_c}\right)} \frac{W}{L} \left(V_{gs} - V_T - V_{ds}\right)^2$$

- Usually just look at extracted I-V curves and adjust $V_{in} \rightarrow V^*$

**Leakage Current**

- Below $V_T$ MOSFET is a literal NPN BJT

$$I_D = I_s e^{\frac{V_{gs} - V_T}{V_T}} \left[1 - e^{-\frac{V_{ds}}{V_T}}\right]$$

$$L \approx \frac{C_{ox}}{C_{ox} + C_JB} = \frac{1}{1 + \chi}$$

- $\chi$ reflects electrostatic control of channel of gate, lower, lower
- Get current even if $V_{gs} = 0$ as long as some $V_{ds}$
- Big power issue

**Short channel effects**

- $V_T$-like doping
- Gate field terminates an $O/S$
- $O/S$ field can influence channel