Review
- Zero & pole causing caps
- Common small signal patterns
- P2 plots - dynamics in step & frequency
- SAC couple

- Last time we discussed a nice mnemonic for identifying QTC caps

- So QTC caps lower gain when shorted
- SCTC caps lower gain when opened

- Must apply mnemonic to small signal model
- Not big signal

- Device caps cause poles - extrinsic caps cause zeros

- Doing cascade has reminded us that we see the same small signal patterns over & over

- Cascade Rint
- CE with degeneration Rint

- mos physics we missed
- CNM calculation done right
- Backgate effect - large signal
- Backgate small signal
- Mode origin
- Long vs. short channel

- Overdrive & biasing by Vt
- Region of operation review
- The mos cascade as an example
- Has design process & biasing

- Rin = R1R3R5 + R5
- You try
- Rin = R0(R4+R5) + R0
- CB input
- EF output

- Good, careful small signal driving
Big challenge of dynamics is going from P2 plots to Bode/resp step

\[ H(s) = \frac{P}{s+P} \]
\[ H(s) = \frac{s+2}{z} \cdot \frac{P}{s+P} \]
\[ H(p) = \frac{P}{2} \cdot \frac{\sqrt{s^2+2^2}}{s^2+1^2} \]
\[ H(p) = \tan^{-1} \left( \frac{p}{2} \right) - \tan^{-1} \left( \frac{p}{P} \right) \]

Note IVT \( \Rightarrow \frac{Z}{P} \) \( \Rightarrow \frac{Z}{2} \) where \( \frac{Z}{P} \) \( \Rightarrow \frac{Z}{2} \)

- General geometric construction extends from this

\[ |H(p)| = \frac{|\frac{Z}{P} - \frac{Z}{2}|}{|\frac{P}{2} - \frac{Z}{2}|} \]
\[ \angle H(p) = \tan^{-1} \left( \frac{\frac{Z}{2}}{\frac{P}{2}} \right) \]

- Leads to RHP zero causing negative phase and positive gain, bad for stability

- Step response is comprised of particular & homogeneous soln

\[ x + kx = y \rightarrow \text{ homogeneous soln \ y side is zero} \]
\[ (s+k)x = sy \]
\[ \frac{x}{s+k} = \frac{s}{s+k} \rightarrow \text{ related to particular soln} \]
\[ \frac{x}{y} = \frac{s}{s+k} \rightarrow \text{ that means poles determine homogeneous soln} \]

So why we can find RC settling trying only RHP seen from cap

**After step input**

1. Immediately activate zeros - related to particular input or constant step

\[ \frac{s}{s+Z} \rightarrow \text{ zero} \]

(IVT again)

2. All poles settle out, \( x(t) = \sum e^{p_k t} c_k \) from ILT

- If all coupled or coupling ramp slow, can look @ close in poles near step
- All poles settling means that we can get time scale separation

\[ x(t) = C_1 e^{-\alpha t} t + C_2 e^{-\beta t} \]

- 2 pole underdamped system w/ dominant pole

- Imagined settling to zero (down step resp.)

- This part dominated by \( p_1 \)
- Mostly see \( p_1 \)

- Happens same in + response

- The zeros-w-poles widely separated
  - amplifiers mostly look like 1st order systems
  - why we approx that way
  - trying to demo this in lab 5, but saw close-in zero

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**MOS Dynamics**

**MOSFET**

- Channel explicitly controlled by capacitance (field lines over oxide dielectric)

\[ \lambda = \frac{Q_{channel}}{E_M} \]

\[ \lambda = \frac{C_{ox} W L (V_g - V_t)}{V_{th}} \]

\[ \lambda = \frac{C_{ox} W L (V_g - V_t)}{V_{th}} \]

- Channel charge distribution varies

\[ n = \sqrt{\frac{N_c e L}{I_D}} \]

\[ s = \sqrt{\frac{N_c e L}{I_D}} \]

- Channel charge distribution varies
- No channel charge
- Small cap to bulk
- None to drain/srce

- $C_{ox\text{ WL cap}}$
- $\frac{1}{2}$ to drain + $\frac{1}{2}$ to srce.

- Charge distribution weird, so cap less
- $C_{ox} = \frac{2}{3} C_{ox\text{ WL}}$
- All to source

*Cap comes from some other components too*

- Really want overlap (why?) $\rightarrow C_{ov}$
- Also comes from field lines terminating from gate side
- Adds to $C_{gd}$

*Still have diodes $\rightarrow$ still have junction caps*

- Very smoothly w/ bias, kind of rounded & non-linear

Let simulator tell you what is $\partial V_{gs}$ $\rightarrow C_{gs}$, $C_{gd}$

**Cmp matrix**

\[
\begin{bmatrix}
C_{gs} & C_{gd} & C_{gs} \\
C_{gd} & C_{dd} & C_{gd} \\
C_{gs} & C_{gd} & C_{ss}
\end{bmatrix}
\]