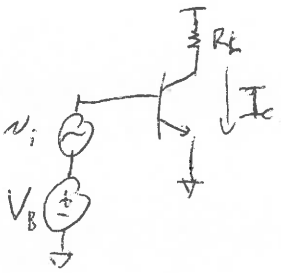
Workload Discussion	CE Amp. Review	Design Params	Emitter Degeneration	Amp Design Example
• see slides for notes	→ 2 port params - Reviewed key design params R_{in}, R_{out}, A_v - Came from a general 2 port amp model - Made small sig CE to find params	f_{low}, i_b, V_{sw}, A_I - Table for them - A_I example (there do) - V_{sw} talk → example	- Want to split A_v & V_o design - Mid-band tricks ok... - But big benefits to emitter degen - Tricky analysis, it's feedback	- Find easy "orthogonal" constraints 1st eg: R_o & V_{sw} - Move backwards to A_v & R_{in} - Big caps for f_{low} last.
(1)	(2)	(3)	(5)	(4)

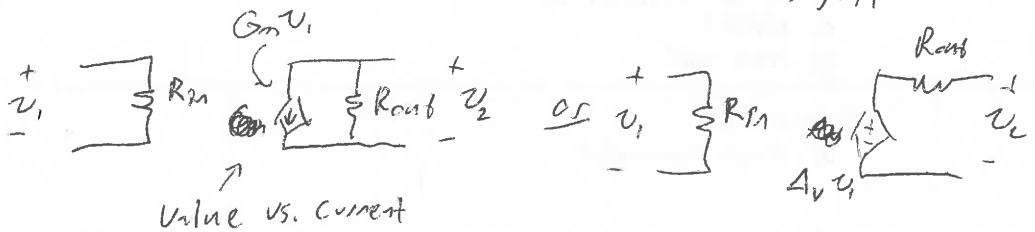
- Last time looked at simply biased CE amplifier



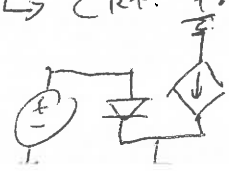
- Specified 3 parameters we cared about

	Name	Colloquial	2 port
R_{in}	Input resistance	Thevenin resistance seen @ input	$\left(\left(\frac{d i_b}{d v_t}\right)^{-1} \text{@ input}\right)$
R_{out}	Output Resistance	Thevenin resistance seen @ output	$\left(\frac{d i_c}{d v_t}\Big\|_{\text{IN Short}}\right)^{-1}$ @ output
A_v	Voltage Gain (small signal)	How much bigger does my signal get?	$\frac{d v_o}{d v_i}\Big\|_{\text{out OPEN}}$

- derivative definitions come from a ~~ideal~~ General small signal amp. model



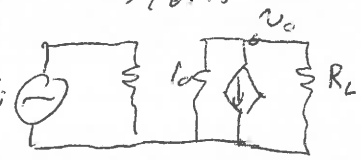
- We make small signal model to find R_{in}, R_{out} & A_v of our amp
  - ↳ Need to ~~find~~ solve large signal model to know small sig
  - ↳ Ckt. to control large signal called biasing/bias network, sort called bias point



Given $V_B \to I_c$

$V_c = V_{cc} - I_c R_c$

+



$R_{in} = r_\pi$

$R_{out} = R_L \| r_o$

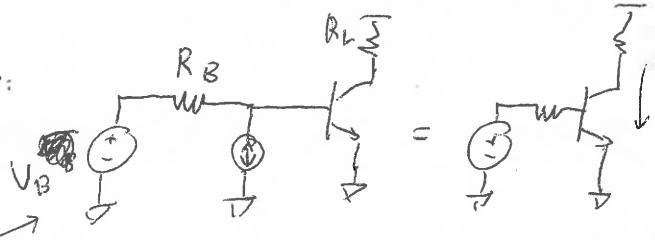
$A_v = -g_m(r_o \| R_L)$

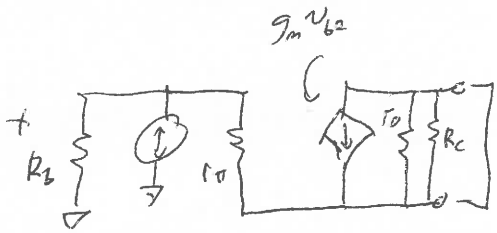
Other design params we care about: I_L, f_{low}, A_I, V_{sw}

↳ V_{sw} most important, do others 1st quick

I_L	Input Leakage/ bias current	Large signal current going into input port	mostly calculate, sense resistor
f_{low}	Low frequency −3dB corner	Frequency @ which mid band assumption fails & start seeing cap high pass	Find pole associated w/ each mid-band cap
A_I	small signal current gain	How much more current does amp spit out than was sent in?	$\left.\frac{di_o}{di_{in}}\right\|_{\text{OUT SHORT}}$

eg:





They Do:

Why large signal in parallel?

① Draw large & small signal ckt.

② Find I_C

③ Find A_I (recall out short)

Find I_C

$I_C = \frac{V_B - 0.7}{R_B}\beta$

- Let R_b be big
- $v_{be} = i_{in} r_\pi$
- $i_o = g_m r_\pi i_{in}$

↳ $A_I = \beta$ (unsurprising!)

V_{sw}	output voltage swing	– How much can V_o change w/o breaking small signal model? – What range of voltages can V_o assume	• Tricky ~~[illegible]~~ usually → rely on $V_{CE,sat}$ for downswing – upswing by load resistor if loaded – by reflecting to input if unloaded – OR by V_{CC} as rough cut

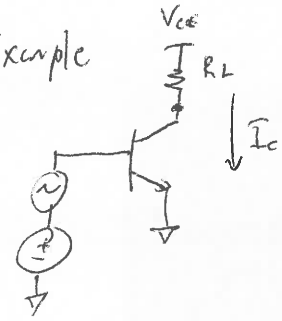
Max swing bias

1. $V_{CC}/2$
2. $V_{CC}/R_{DC}+R_{AC}$

– block –

~ Bridges large & small signal model, so it's tricky

Output swing Example



$V_{CC} = 5V$ $V_{CE,sat} = 0.1V$

$R_L = 1\,k\Omega$

$I_C = 2.5\,mA$

- Find top allowed voltage, bottom allowed voltage & V_{SW}

① Find V_o $V_o = V_{CC} - I_C R_L = 2.5V$

② Minimum voltage (set by $V_{CE,SAT}$) $\rightarrow$ $V_{min} = V_{CE,SAT} = 0.1V$

③ max voltage ③.1 $V_{max} = V_{CC} = 5V$, so $V_{SW} = 4.9V$

③.2 $A_v = g_m R_L = \frac{2.5\,mA}{25\,mV} 1k\Omega = 100$

- massive distortion w/ FFT. Harmonic peaks.

$26\,mV \cdot 100 = 2.6V$ ~ so $\pm 2.5V$ ok approx here

Let's design an amplifier

↳ so far we've moved from circuits → amp specs.

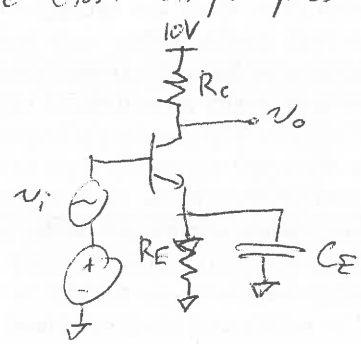
↳ now job is to move from amp specs to circuits

<u>example:</u> $R_{out} < 2\,k\Omega$

$R_{in} > 1\,k\Omega$

$A_v =$

$V_{SW} > 4V$



$\beta = 100$

$V_B = 3.2V$

$V_{CE,sat} = 0.3V$

① start w/ Easy constraints

min power by setting $I_C = 2.5mA$

$g_m = 100mS$

- In this case, $R_{in} = r_\pi \longrightarrow r_\pi = \frac{\beta}{g_m} = \frac{\beta \phi_t}{I_C} = \frac{100 \cdot 25mV}{I_C} > 1k\Omega \rightarrow I_C > 2.5mA$

- usually, easy constraints are found @ output: V_{SW} or R_{out}

② Propagate

$R_C = 1.6k$

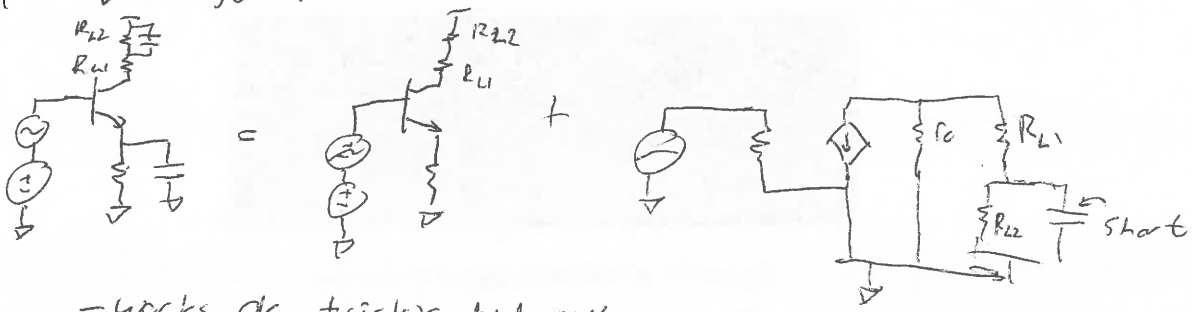
- know $V_E = 2.5V$, so need $R_E = 1k$

- [illegible] inverter $V_o < 8V$ & down swing says $V_o > 4.8V$, $\frac{1}{2}$ way is 6.4V

Have an odd issue ~

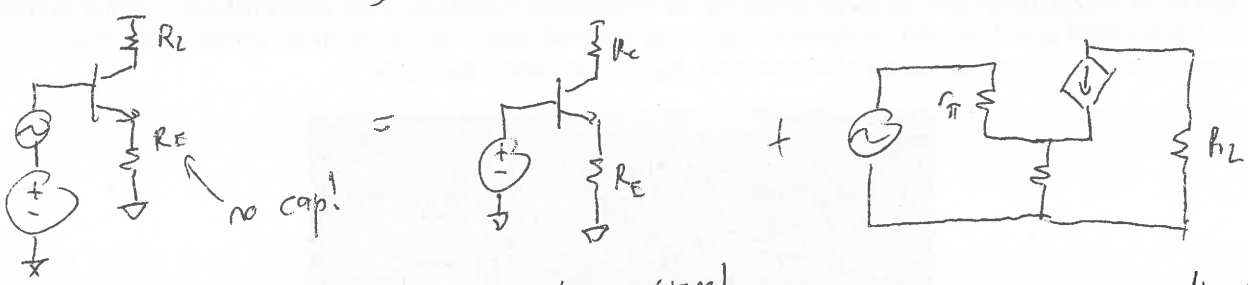
- specifying R_{in} & V_{SW} fully specifies R_{out} & A_v
- $1.6k\Omega \cdot 100mS = A_v = 160$ & $R_{out} \approx 1.6k\Omega$ $\left(\frac{50V}{2.5mA} = 20k\Omega \right)$ Fo...
- we'd like to build amps where we can set V_{SW} indept. A_v

Trick #1 - Leverage the midband



- works dc, tricky high pass

Trick #2 - Emitter degeneration



same large signal that we're used to

- crazy new small signal
- ignoring r_o for now, you'll add it back in on your HW

Find R_{in}, R_{out}, A_v

Me R_{in}

- Note $v_{in} \neq v_{be}$
- leads to feedback (could do fun LCL stuff)

$v_{be} = i_i \cdot r_\pi$

$v_E = (g_m r_\pi i_i + i_i) R_E$

$v_i = v_E + v_{be} = i_i (r_\pi + R_E + \beta R_E)$

really big!

You Try A_v

$v_{be} = r_\pi \, v_i / R_{in}$

$v_o = -g_m \left(r_\pi \, v_i / R_{in} \right) \cdot R_L$

$= \dfrac{-g_m r_\pi R_L}{r_\pi + R_E + \beta R_E} v_i$

$A_v = \dfrac{-\beta R_L}{r_\pi + (\beta+1) R_E} \approx \dfrac{-R_L}{R_E}$

- can have $g_m r_\pi$ [illegible]
- Free V_o [illegible]