Review Small Signal Derivation?	Roadmap	Amplifier params	CE large signal	CE small signal
Add Load Line	- Input, output & bias - Show CE, CB, EF - In modulates BE junction ~~- 2 port Review~~	- 2 port review - R_{in}, R_o, A_v - A_{i_g}, V_{swing}, ~~$A_{v,max}$~~ - i_{b_g}, ~~$i_{b_{CE}}$~~ - S_{low} - PSRR, CMRR, Noise	⑤	④

(optional) small signal model review in FAR

$$i_c = \beta i_b$$

$$i_e = i_c + i_b$$

$$i_b = I_{ES}\left(e^{v/\phi_{th}} - 1\right)$$ ← only a function of v_{BE}

a conductance, $r_\pi = \frac{\phi_{th}}{I_B} = \frac{\beta}{g_m}$

$$\frac{\partial i_b}{\partial v_{CE}} = \frac{I_B}{\phi_{th}}$$

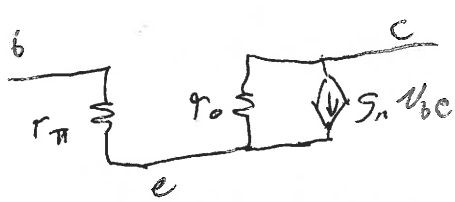
$$i_c = \beta I_{ES}\left(e^{v/\phi_{th}} - 1\right)\underbrace{\left(1 + \frac{v_{CE}}{V_A}\right)}$$ ← $\frac{\partial i_c}{\partial v_{BE}} = \frac{I_c}{\phi_{th}} \equiv g_m$

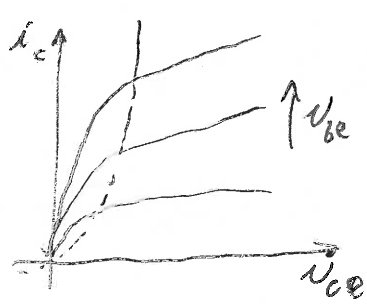
we've been ignoring in calcs, but showing on large signal plots

$$\frac{\partial i_c}{\partial v_{CE}} = \frac{I_c}{V_A}$$ ← a conductance

↳ $r_o = \frac{V_A}{I_c}$

- All same for NPN & PNP b/c of wacky sign conventions making large signal plots same (upside down large signal models only issue)



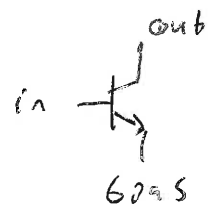


GET HYPE, WE'RE DOING AMPLIFIERS!

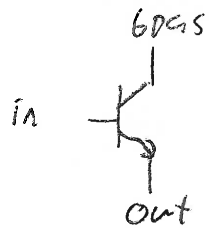
↳ sort of why we're here!

Roadmap

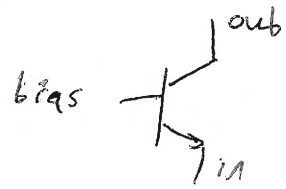
- 3 terminals & 3 key functions (in, out & bias)



Common-emitter



Common-collector
or
emitter follower

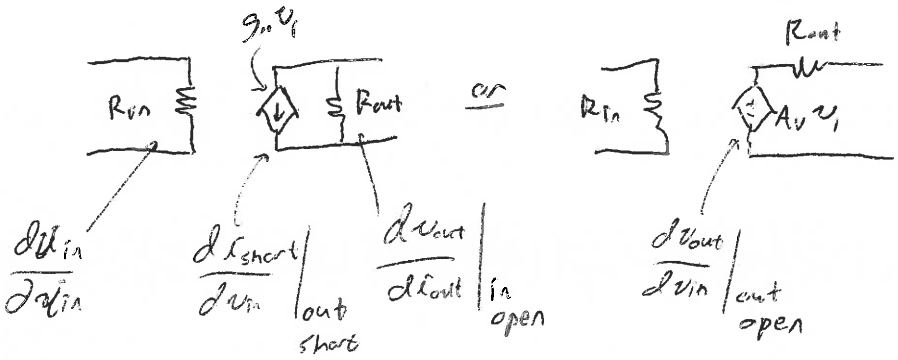


Common-base

Always use v_{in} to modulate v_{be} junction

Amplifier Design Parameters

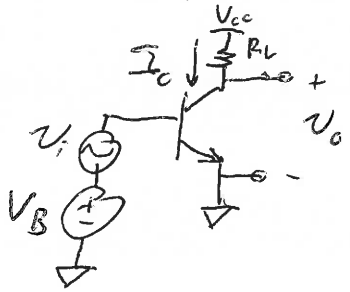
- each configuration does different things well, want a quantitative description of those things
- most common parameters are R_{in}, R_{out} & A_v & V_{sw}
  - ↳ technically Z_{in} & Z_{out} ...
  - ↳ small signal qty. & R_{in} & R_{out} linear



- Recall our 2 port amplifier model
- Can rep. as Thevenin/Norton

- Circuit picture of these derivatives is small signal test sources
- 2 port model lets us separate analysis from loading

- save V_{sw} (& oddities: A_i, i_b & simple thing f_{low}) until after we apply this

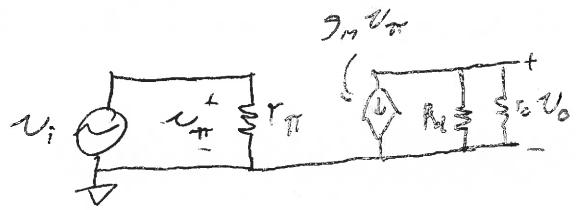


- Let V_B be picked such that we have I_c flowing into BJT

(Naive) CE Amplifier!

- You guys find R_{in}, R_{out} & A_v (symbolically)
- Find values if $I_c = 1mA$, $V_A = 50V$, $\beta = 100$, $R_L = 1k$

small signal model



$R_{in} = r_\pi$

$R_{out} = r_o \| R_L$ ← r_o usually big, so ignore it; ← max possible $R_{out} = r_o$

$A_v = -g_m (r_o \| R_L)$ ← max gain is $g_m r_o$; ← negative b/c nudging v_{be} up causes v_o to nudge down w/ more current

- v_i controls v_{be} directly

- w/ BJs → $g_m = \frac{I_c}{\phi_{th}} \approx 40mS$ w/ $25mV$ ϕ_{th}

$r_o = 50k\Omega$ $\left(\frac{50V}{1mA}\right)$

$R_{out} \approx 1k$ & $A_v \approx -40$

- Let $V_{cc} = 5V$, how big can v_i be before trouble?
  - ↳ have issues if v_o too big or too small
  - ↳ too big cuts off I_c ~ note I_c also $= \frac{V_{CE} - V_o}{R_L}$ ← easy way to check I_c!
    - ~ means cutoff transistor
    - ~ $v_{in,min} = 0.7V$
    - — propagate $V_B - V_{in,min}$ to output
  - ↳ too small saturates BJT
    - ~ $V_o > V_{CE,SAT}$
  - ↳ voltage swing, V_{sw}, is max V_{out} − min V_{out}

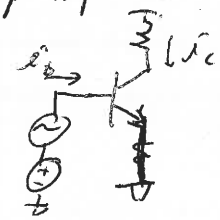
- Other amplifier specs.
  - ↳ short circuit current gain, A_i

$$\frac{i_{short}}{i_{in}}$$

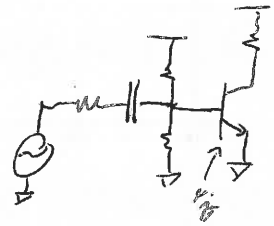
Ther Find for CE?

$$A_i = g_m r_\pi$$

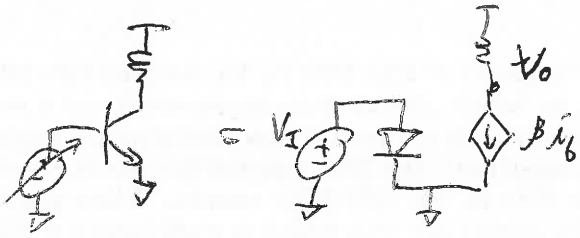
  - ↳ Input bias current, i_{in}
    - Large signal, DC, parameter
    - How much current does the amp input steal?
    - For us: I_c/β in CE amp

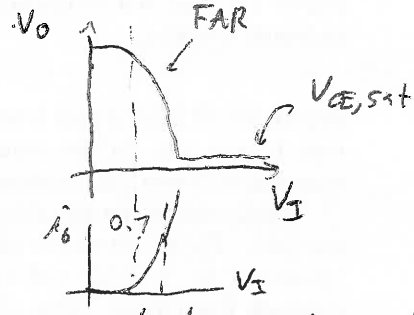


  - ↳ Low frequency corner, f_{low}
    - Where does mid-band approx break?



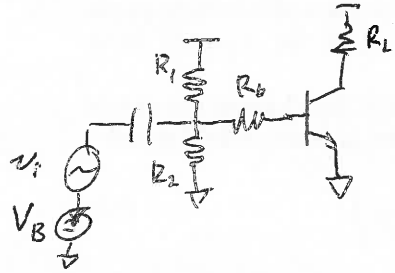
- Large Signal Behavior

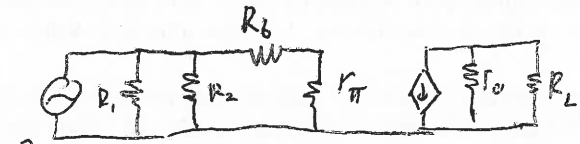




  - Looks like logic gate X^{fer} curve, some early logic gates made this way

- Let's try practical CE amplifier w/ series bias





source impedance would make this tougher

$R_{in} = R_b + r_\pi \parallel R1 \parallel R2$

$R_{out} = r_o \parallel R_L$

$$A_v = \frac{r_\pi}{R_b + r_\pi} g_m (r_o \parallel R_L)$$

A_i, i_{in}, f_{low}, large signal, practical w/ series R_b