Digital Design and Computer Architecture (E85)

J. Spjut & M. Spencer

Problem Set 10

1. The pipelined ARM processor is running the following programs. Which registers are being written and which are being read on the fifth cycle? Recall that the pipelined processor has a hazard unit.

a.

```
ADD R1, R2, #5
SUB R0, R5, R6
LDR R3, [R1, #15]
STR R7, [R0, #72]
ORR R6, R8, R9
```

b.

```
ADD R0, R4, R5
SUB R1, R6, R7
AND R2, R0, R1
ORR R3, R8, R9
SUBS R4, R2, R3
```

2. Show an execution diagram similar to figure 0.53 in the chapter 7 text showing the forwarding and stalls needed to execute the following instructions on the pipelined ARM processor.

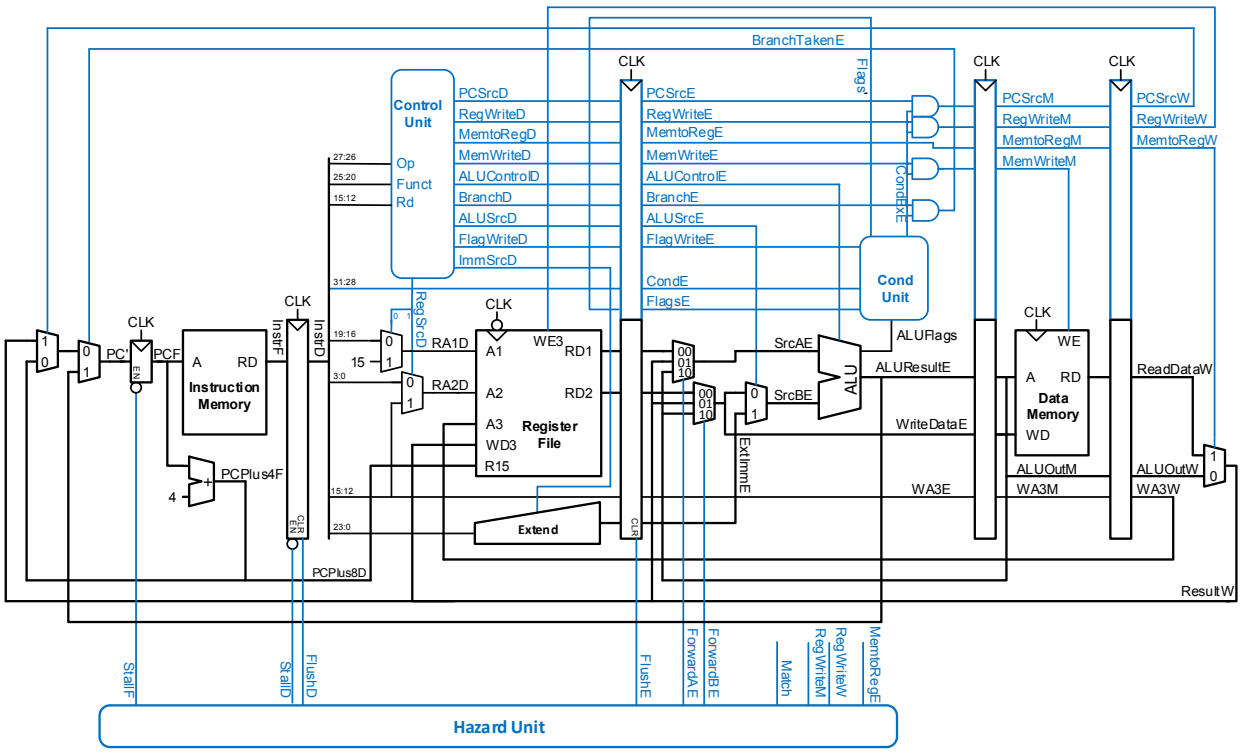
```
ADDS R4, R0, R1
LDR R5, [R2, #60]
SUB R6, R4, R3
AND R7, R5, R4
```

3) Textbook Problems

Do problems 8.11, 8.20.

4) Time

Please indicate how many hours you spent on this problem set. This will not affect your grade (unless completely omitted), but will be helpful for calibrating the workload for next semester's class.


BranchTakenE
Control Unit
Op
Funct
Rd
PCSrcD
RegWriteD
MemtoRegD
MemWriteD
ALUControlD
BranchD
ALUSrcD
FlagWriteD
ImmSrcD
PCSrcE
RegWriteE
MemtoRegE
MemWriteE
ALUControlE
BranchE
ALUSrcE
FlagWriteE
CondE
FlagsE
Flags'
CondExE
Cond Unit
PCSrcM
RegWriteM
MemtoRegM
MemWriteM
PCSrcW
RegWriteW
MemtoRegW
CLK
PC'
PCF
Instruction Memory
InstrF
InstrD
RegSrcD
RA1D
RA2D
Register File
WE3
RD1
RD2
A1
A2
A3
WD3
R15
Extend
ExtImmE
SrcAE
SrcBE
ALU
ALUFlags
ALUResultE
WriteDataE
WA3E
Data Memory
WE
WD
ReadDataW
ALUOutM
ALUOutW
WA3M
WA3W
ResultW
PCPlus4F
PCPlus8D
StallF
StallD
FlushD
FlushE
ForwardAE
ForwardBE
Match
RegWriteM
RegWriteW
MemtoRegE
Hazard Unit