Digital Design and Computer Architecture (E85)

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Problem Set 9

1) Problems

1. Modify the multi-cycle ARM processor to add the functionality required to implement $R_{rshiftr}$-Type instructions. Label all added signals and describe the circuits in each block added to the data-path. Also show any changes required for the controller FSM.

2. Find the new cycle-time for a multi-cycle and calculate the execution time for 100 billion instructions for the ARM processor based on the timings in Table 0.5 in chapter 7.3 if a new ALU design reduces the ALU delay by 20ps. Use the same instruction mix as example 7.5 in the text.

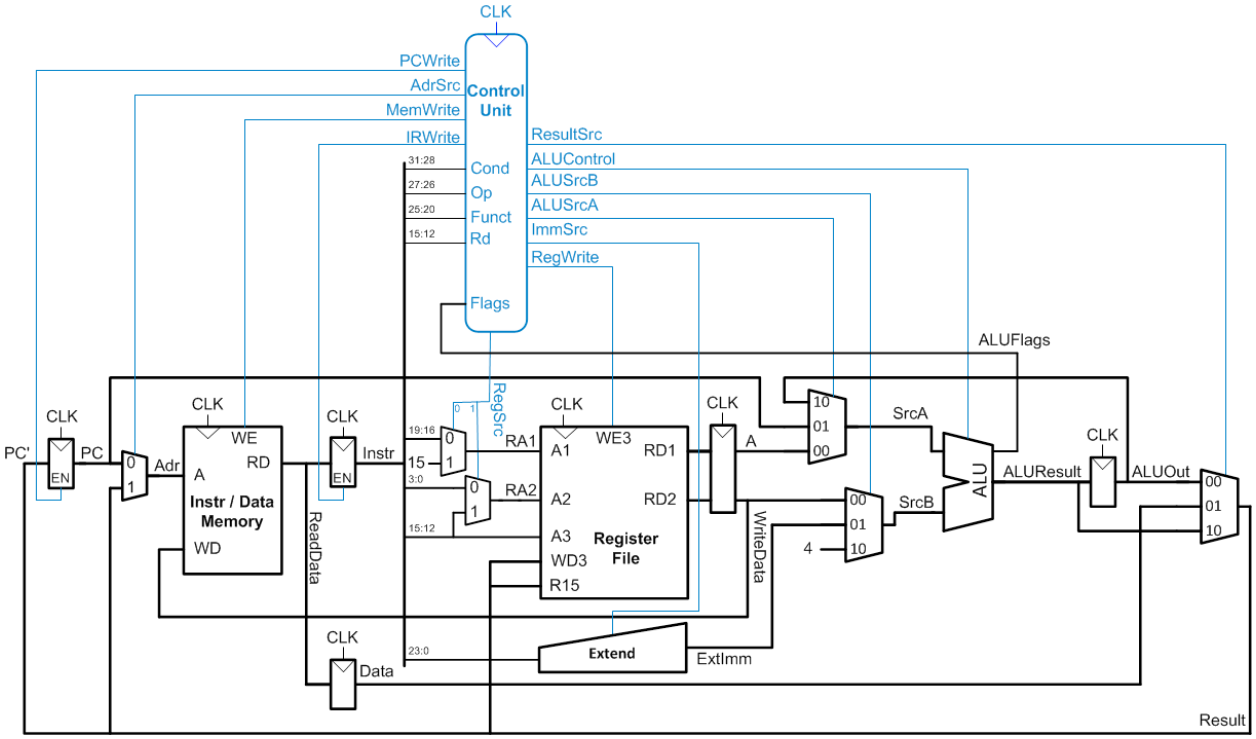
3. If a friend were able to design a register file that consumed 40% less power but doubled its delay. Would you use that component? Assume the delays of the original register file and all other components are the same as in table 7.5. Explain your decision.

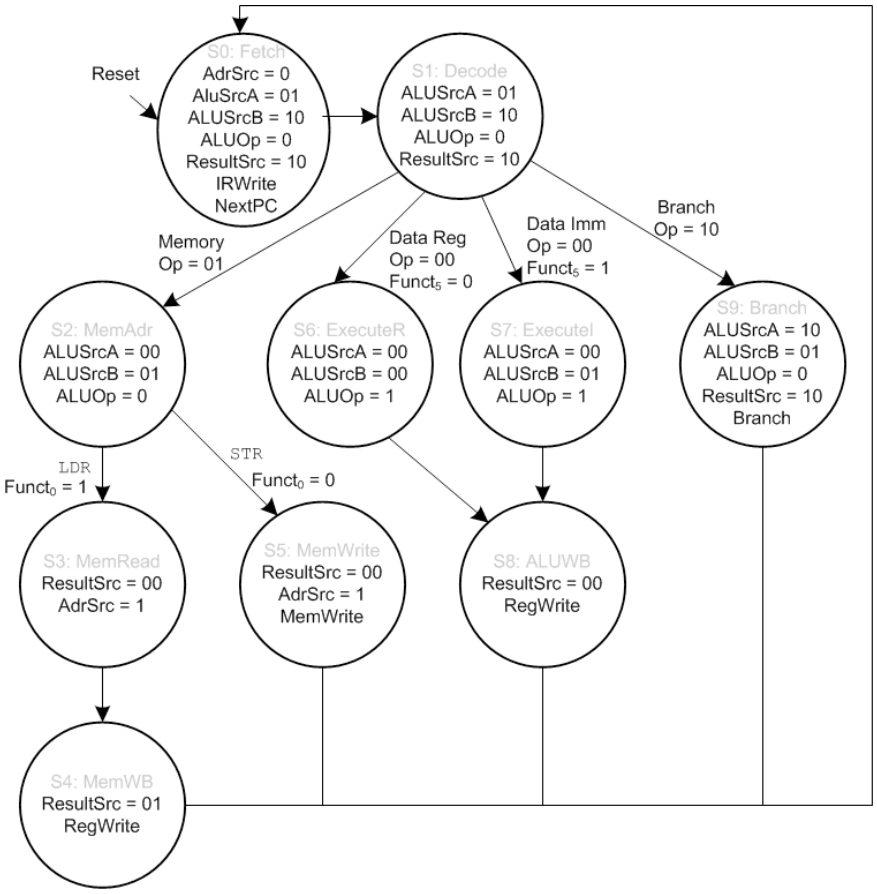
4. How many cycles are required to run the following program on the multi-cycle ARM processor? What is the CPI of this program?

```
     MOV R0, #5
while:
     CMP R0, #0
     BEQ done
     SUB R0, R0, #1
     B while
done:
```

2) Time

Please indicate how many hours you spent on this problem set. This will not affect your grade (unless entirely omitted), but will be helpful for calibrating the workload for next semester's class.





State	Datapath μOp
Fetch	Instr ←Mem[PC]; PC ← PC+4
Decode	ALUOut ← PC+4
MemAdr	ALUOut ← Rn + Imm
MemRead	Data ← Mem[ALUOut]
MemWB	Rd ← Data
MemWrite	Mem[ALUOut] ← Rd
ExecuteR	ALUOut ← Rn op Rm
ExecuteI	ALUOut ← Rn op Imm
ALUWB	Rd ← ALUOut
Branch	PC ← ALUOut + offset