Digital Electronics and Computer Engineering (E85)
Spring 2013
Syllabus

Teaching Staff

Professors:	Josef Spjut Parsons 2374	josef_spjut@hmc.edu Hours: T,W 2:30-4:30pm
	Ruye Wang Parsons 2372	ruye_wang@hmc.edu Hours:
Lab Tutors:	Dong-Hyeon Park Joshua Vasquez Austin Chen Nicole Yu Dylan Stow	
Lab Graders:	Sasha Paudel Katherine Yang	
Homework Graders:	Douglas Hu Lauren Nishizaki Matt Espy	

Schedule:

Lecture:		MWF 10:00-10:50
Lab Hours:	Nicole	Tu 9-11
	Dylan	W 7-9
	Dong-hyeon	Th 6-8
	Joshua	Th 7-9
	Austin	Th 9-11
TBII Tutor Hours:		Sat 3-5, Sun 7-9

Textbook:

Harris & Harris, *Digital Design and Computer Architecture*, 2nd Ed., Morgan Kaufmann, 2012.

Electronic Communication

Class Web Page:	http://fourier.eng.hmc.edu/e85
Class Email List:	eng-85-l@hmc.edu

Be sure you are on the class mailing list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-85-l

Alternatively, if you have an electronic version of the syllabus, you can click this paragraph to have your mail client autocomplete the email for you.

You also will need a Harvey Mudd College computer to complete your labs. If you are not a HMC student, email me your full name and school affiliation and I will request an account for you. You will complete most of your labs in the E85 lab, Parsons B183. See Professor Spjut for the door code. Hardware portions of the labs must be completed in the E85 lab, but other computers including

the ones in the ECF may be used for some parts of the labs. If you have issues with the software or computer systems in the lab, contact the system administrator, Willie Drake. He can often be found in his office inside the ECF, and after-hours contact information is typically posted on his door.

Course Objectives:

- To apply the principles of abstraction, modularity, hierarchy, and regularity in digital design
- To develop debugging skills by designing, building, and testing digital circuits using commercially available CAD (computer aided design) tools
- To design, build, and test your own microprocessor
- To understand what's under the hood of a computer

Grading:
Labs: 30%
Problem Sets: 25%
Midterm 1: 20%
Midterm 2: 25%

There will be weekly labs and problem sets, a and two midterm exams. The first midterm will be taken in-class and the second will be a take-home exam. The first midterm is worth 20% of your grade and is closed-book, closed-notes. The second midterm is open-book, open-notes (your own notes, including course handouts) and is comprehensive, but biased towards the second half of the class. It is worth 25% of your grade.

The only way to really master the material in this class is to design a microprocessor. The labs in this class build upon each other and culminate in designing your own 32-bit MIPS microprocessor in Labs 10 and 11. You **must** complete these labs and demonstrate a working microprocessor to pass this class.

No late homework or labs will be accepted. However, you are allowed to drop one lab and one homework score. Homework is due **at the beginning** of class. You will lose 50% of the points on late homework turned in by the end of class. Labs are due electronically on Sakai by 12 noon on the due date. Even if you do not complete your microprocessor (labs 10 & 11) on time, you must still submit them before finals week to pass the class.

Your lowest lab and homework score will be dropped before the average is calculated. You are welcome to discuss labs and problem sets with other students or with the professor or lab assistants or tutors after you have made an effort by yourself. However, you must turn in your own work, not work identical to that of another person. Be sure to credit at the top of your assignment anyone with whom you discussed ideas. **It is an honor code violation to simply copy someone else's work.** Reading assignments are to be completed before class.

A suggestion for text preparation comes from reddit user **onanym**, "I usually write a cheat sheet, then memorize it so it's all in my head. That way, they can't possibly prove I'm cheating.
Genius." As a response, reddit user **leontes** added, "I used to [do] that, but I found I couldn't remember the details perfectly. So instead... I integrated the information on the cheat sheet into my prior existing knowledge, Coding it perfectly within my preexisting framework.
Not only could they not know I was regurgitating the cheat sheet, but since I had remembered it in terms of [stuff] I already knew, I was able to synthesize complex consequences from the source material so it seemed like original, derivated understanding! They never caught on!" From `http://www.reddit.com/r/AskReddit/comments/11nbmz/im_a_political_science_professor_i_gave_my/c6nzn34`

Tentative Schedule: The schedule below is a tentative plan that may change during the semester. The deadlines, however, are fixed unless otherwise notified; do not assume that they will change just because the lecture schedule changes. Any changes to deadlines will be announced in class and sent to the class mailing list.

Monday	Wednesday	Friday
Jan 21st Martin Luther King Jr. Day	23rd **1** Binary, logic gates, logic levels 1.1-1.5,A.1-A.2,A.5-A.7	25th **2** transistors; truth tables 1.6, 1.7,1.9
28th **3** Boolean expressions; Boolean algebra 2.1-2.3 **PS1 Due**	30th **4** K-maps; Xs and Zs; multiplexers and decoders; priority circuit 2.4-2.8	Feb 1st **5** timing; hazards; sequential circuits: SR latches 2.9-2.10,3.1-3.2.1 **Lab1 Due**
4th **6** Last Day to Add Classes D latches, flip-flops, clocking 3.2.2-3.3.3 **PS2 Due**	6th **7** finite state machines (FSMs) 3.4	8th **8** dynamic discipline 3.5.1-3.5.3 **Lab2 Due**
11th **9** metastability, parallelism 3.5.4-3.5.6,3.6, 3.7 **PS3 Due**	13th **10** System Verilog 1 4.1-4.3	15th **11** System Verilog 2 4.4-4.9 **Lab3 Due**
18th **12** System Verilog 3 **PS4 Due**	20th **13** arithmetic: adders, subtractors, comparators 5.1-5.2.5	22nd **14** ALUs 5.2.6-5.2.8 **Lab4 Due**
25th **15** number systems: fixed & floating 5.3 **PS5 Due**	27th **16** sequential building blocks: counter, shift register, memory arrays: RAMs, ROMs 5.4, 5.5	Mar 1st **17** logic arrays: PLAs, FPGAs 5.6, 5.7 **Lab5 Due**
4th **18** Problems/Review	6th **19** Problems/Review	8th **20** End E85A **Midterm #1**
11th **21** C-programming 1 c.1-c.4	13th **22** C-programming 2 c.5-c.8	15th **23** C-programming 3 c.9-c.11 **Lab6 Due**
18th Spring Break	20th Spring Break	22nd Spring Break

Monday	Wednesday	Friday
25th **24** MIPs instruction set and registers 6.1-6.3	27th **25** branches & procedure calls 6.4 **Lab7 Due**	29th Cesar Chavez Day
Apr 1st **26** addressing modes 6.5 **PS6 Due**	3rd **27** linking & launching applications 6.6-6.7.1	5th **28** single-cycle processor data path 7.1-7.3.1 **Lab8 Due**
8th **29** single-cycle processor control 7.3.2-7.3.4 **PS7 Due**	10th **30** multi-cycle processor 1 7.4.1	12th **31** Last Day to Drop Classes multi-cycle processor 2 7.4.2-7.4.4 **Lab9 Due**
15th **32** pipelining 1 7.5.1 **PS8 Due**	17th **33** pipelining hazards and stalls 7.5.2-7.5.5	19th **34** exceptions and advanced microarchitecture 7.7-7.8 **Lab10 Due**
22nd **35** memory system, performance 8.1, 8.2 **PS9 Due**	24th **36** caches 8.3	26th **37** caches and virtual memory 8.4 **Lab11 Due**
29th **38** Review **PS10 Due** **Midterm #2 Distributed**	May 1st **39** memory-mapped, embedded and PC I/O 8.5-8.7	3rd **40** Last Day of Classes No Lecture **Midterm #2 Due by Noon**