# Digital Design and Computer Architecture (E85)

J. Spjut & R. Wang Spring 2013

**Problem Set 9** **Due: Monday, 4/22/2013**

## 1) Textbook Problems

Do problems 7.29, 7.31, 7.34.

I've included a diagram of the pipelined MIPS processor's hardware and the main controller truth table for your convenience on the last page.

## 2) Pipelined Processor – Hazard Unit Hardware

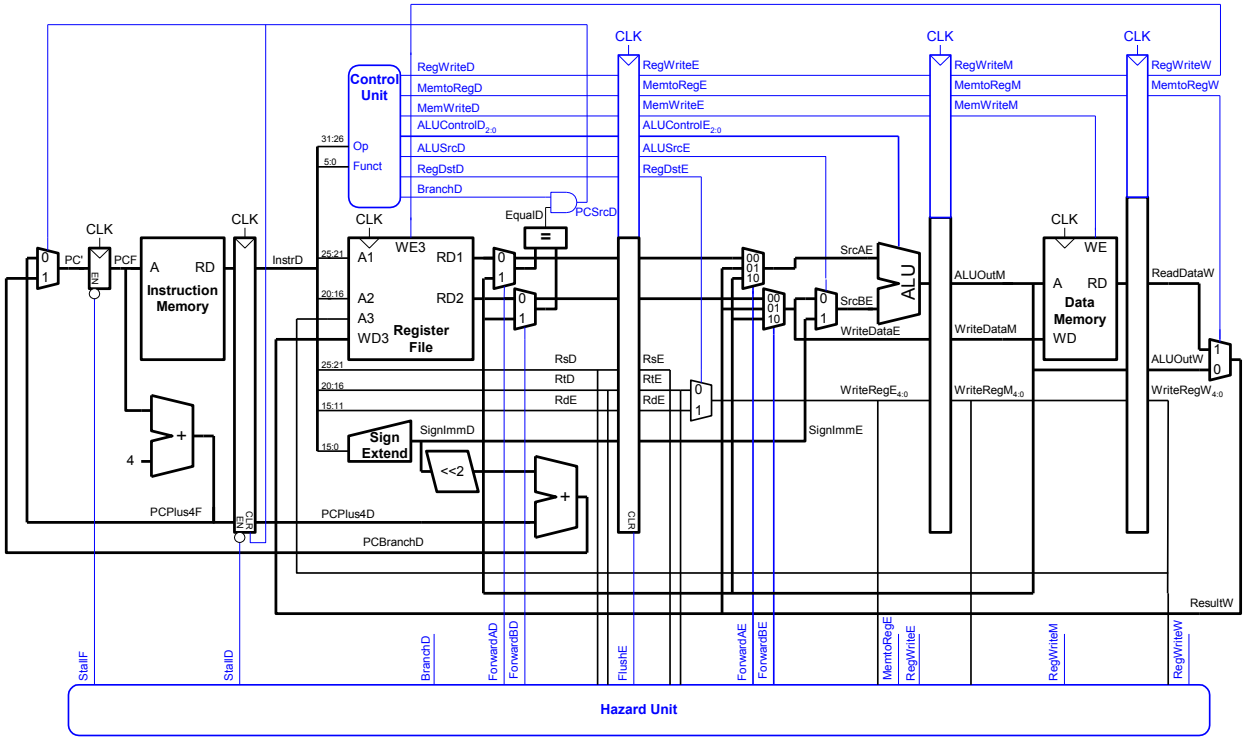
Design the hardware for the following signals of the pipelined processor's Hazard Unit. Remember that you can use any of the digital building blocks we have discussed in class.

$ForwardAE_{1:0}$

*lwstall*

## 3) Time

Please indicate how many hours you spent on this problem set. This will not affect your grade (unless entirely omitted), but will be helpful for calibrating the workload for next semester's class.




| Instruction | $Op_{5:0}$ | RegWrite | RegDst | $AluSrc_{1:0}$ | Branch | MemWrite | MemtoReg | $ALUOp_{1:0}$ |
|---|---|---|---|---|---|---|---|---|
| R-type | 000000 | 1 | 1 | 0 | 0 | 0 | 0 | 10 |
| lw | 100011 | 1 | 0 | 1 | 0 | 0 | 1 | 00 |
| sw | 101011 | 0 | X | 1 | 0 | 1 | X | 00 |
| beq | 000100 | 0 | X | 0 | 1 | 0 | X | 01 |
| **addi** | **001000** | | | | | | | |