Parallel Computer Architecture Design (E190o)
Spring 2013
Syllabus

Teaching Staff

Professor:	Josef Spjut	josef_spjut@hmc.edu
	Parsons 2374	Hours: T,W 2:30-4:30pm
Grader:	Andrew Carter	

Schedule:

Lecture:	MW 1:15-2:30
Lab Tutor Hours:	ECF W 7-9

Textbook:

Hennessy & Patterson, *Computer Architecture: A Quantitative Approach*, 5th Ed., Morgan Kaufmann, 2012.

Electronic Communication

Class Web Page:	http://www3.hmc.edu/~jspjut/class/e190o
Class Email List:	eng-190o-l@hmc.edu

Be sure you are on the class mailing list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-190o-l

Alternatively, if you have an electronic version of the syllabus, you can click this paragraph to have your mail client autocomplete the email for you.

You also will need a Harvey Mudd College computer to complete your labs. If you are not a HMC student, email me your full name and school affiliation and I will request an account for you. Your lab work will use tera, a linux server (tera.eng.hmc.edu). The ECF may be used for the labs, but any computer with a secure shell should suffice. If you have issues with the software or computer systems in the ECF, contact the system administrator, Willie Drake. If you have any issues with tera, then contact Prof. Spjut or Andrew Carter.

Course Objectives:

- To learn about modern advances in computer architecture
- To develop debugging skills by designing, building, and testing digital circuits using commercially available CAD (computer aided design) tools
- To design, build, and test your own parallel microprocessor
- To learn to work on a design team, dividing tasks and conquering problems
- To understand the broad impact of computer architecture on the world, and the influences from other disciplines on computer architecture.

Grading:
Homework: 20%
Labs: 30%
Project: 30%
Midterm 1: 10%
Midtern 2: 10%

There will be weekly labs and problem sets for the first half of the class, with a team project for the second half of the class. In addition there will be 2 in-class midterm exams. Both exams will be open book and open notes, however you are encouraged to prepare so you will not need either. The exams will be designed in such a way that they should not require the book or notes, and so that the book and notes will not help you very much anyway. They are each worth 10% of your grade.
A suggestion for text preparation comes from reddit user **onanym**, "I usually write a cheat sheet, then memorize it so it's all in my head. That way, they can't possibly prove I'm cheating.
Genius." As a response, reddit user **leontes** added, "I used to [do] that, but I found I couldn't remember the details perfectly. So instead... I integrated the information on the cheat sheet into my prior existing knowledge, Coding it perfectly within my preexisting framework.
Not only could they not know I was regurgitating the cheat sheet, but since I had remembered it in terms of [stuff] I already knew, I was able to synthesize complex consequences from the source material so it seemed like original, derivated understanding! They never caught on!" From `http://www.reddit.com/r/AskReddit/comments/11nbmz/im_a_political_science_professor_i_gave_my/c6nzn34`

The labs in the class will walk you through the design of a number of parallel architectural features based on an architecture called DLX. The DLX architecture is quite similar to the MIPS architecture you designed in E85. In addition, we will provide assembly tools for you to write and debug applications on your processor. The labs are to be completed by partnerships of 2 students working together. You are allowed to divide the work as you see fit, but both members should at least be aware of each decision made in the design.

No late homework or labs will be accepted. Labs will be turned in on tera according to the procedure found in Lab 0. We will be using the source code management software called git to allow for ease of group work. Lab 0 has suggested resources for learning how to use git. Various design an progress documents should be turned in as part of the project. You are welcome to discuss labs and problem sets with other students or with the professor and lab assistants after you have made an effort by yourself. However, you must turn in your own work, not work identical to that of another team. Be sure to credit at the top of your assignment anyone with whom you discussed ideas. **It is an honor code violation to simply copy someone else's work.**

Tentative Schedule: The schedule below is a tentative plan that may change during the semester. The deadlines, however, are fixed unless otherwise notified; do not assume that they will change just because the lecture schedule changes. Any changes to deadlines will be announced in class and sent to the class mailing list.

Monday	Wednesday	Friday
Jan 21st Martin Luther King Jr. Day	23rd **1** Quantitative Design and Analysis Chapter 1	25th
28th **2** Digital Logic and Verilog Review	30th **3** DLX Architecture Overview	Feb 1st **Lab 0.0 Due**
4th **4** Last Day to Add Classes Memory Hierarchy Chapter 2 **Homework 000 Due**	6th **5** Instruction-Level Parallelism Chapter 3	8th **Lab 1.0 Due**
11th **6** ILP cont.	13th **7** Data-Level Parallelism Chapter 4	15th
18th **8** GPUs **Homework 001:1-3 Due**	20th **9** Memory Hierarchy cont. Chapter 2	22nd **Lab 1.1 Due**
25th **10** OOO Processing **Homework 001:4-5 Due**	27th **11** Thread-Level Parallelism Chapter 5	Mar 1st **Lab 2.0 Due**
4th **12** Project Kickoff	6th **13** TLP cont.	8th **Lab 2.1 Due**
11th **14** **Midterm #1**	13th **15** Problems Day **Project Proposal Due**	15th **Lab 2.2 Due**
18th Spring Break	20th Spring Break	22nd Spring Break
25th **16** Proposal Presentations	27th **17** Proposal Presentations **Project Interface Design Due**	29th Cesar Chavez Day
Apr 1st **18** TBA **Homework 010 Due**	3rd **19** **Project Testing Plan Due**	5th
8th **20**	10th **21** **Project Status Report Due**	12th Last Day to Drop Classes

Monday	Wednesday	Friday
15th **22** TBA **Homework 011 Due**	17th **23** **Project Due**	19th
22nd **24** Project Presentations **Homework 100 Due**	24th **25** Project Presentations	26th
29th **26** Project Presentations	May 1st **27** **Midterm #2**	3rd Last Day of Classes