# Digital Design and Computer Architecture (E85)

J. Spjut Fall 2014

## Midterm

*" There are 10 kinds of people in the world – those who understand binary and those who don't."*

This is a closed-book closed-notes exam. You are permitted a calculator and one 8.5x11" sheet of paper with notes. You may have notes on both sides of the single 8.5x11" sheet.

You are allowed at most **1 hour and 30 minutes** to take the exam. The exam should be returned to Prof. J. Spjut's office no later than 3 pm on Friday October 17th.

Along side each question, the number of points is written in brackets. The entire exam is worth 100 points. Plan your time accordingly. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Write neatly; illegible answers will be marked wrong. **Show your work** for partial credit.

**Name: _____**

Name:_____

## Do Not Write Below This Point

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Name:_____

1. [24] For the Boolean equation

$$Y = (A \oplus B)C + \overline{A}B\overline{C} + \overline{A}(B \oplus C)$$

(a) Show the truth table for Y as a function of inputs A, B, and C.

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

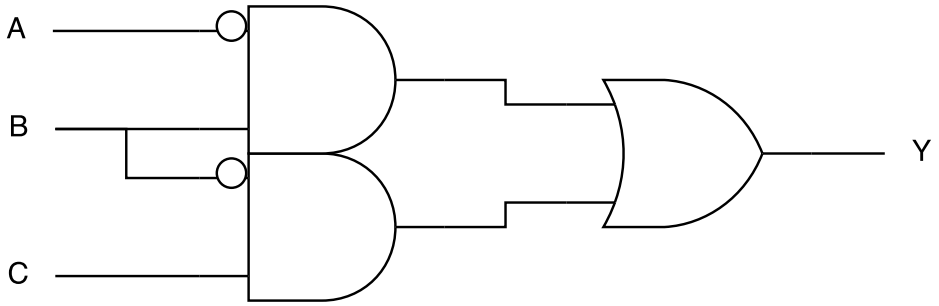
(b) Simply the Boolean equation for Y as a function of inputs A, B, and C.

| | | AB | | | |
|---|---|---|---|---|---|
| | | 00 | 01 | 11 | 10 |
| C | 0 | 0 | 1 | 0 | 0 |
| | 1 | 1 | 1 | 0 | 1 |

Y = !AB + !BC (+ AC)

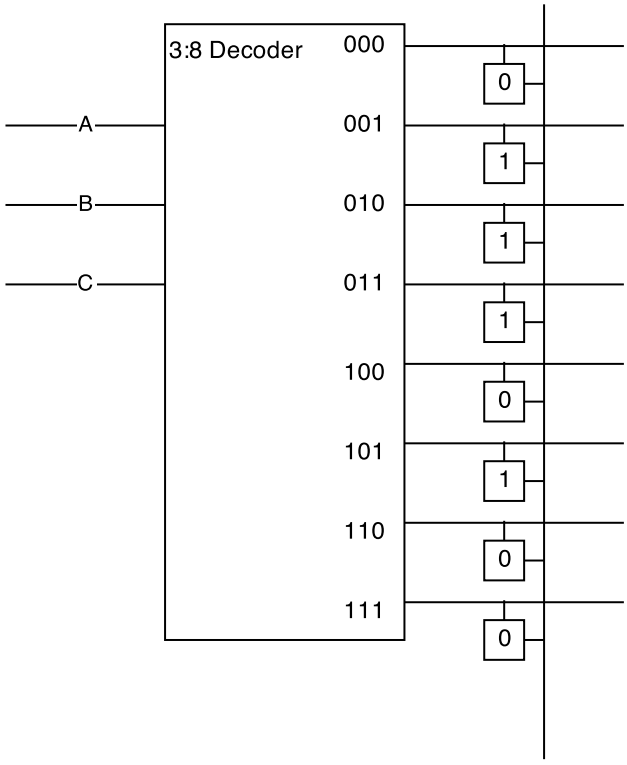
1 (cont.)

(c) Show the gate schematic for inputs A, B, and C and out Y. Use the minimum numbers of AND and OR gates.




(d) Show a lookup table (LUT) implementation of Y as a function of inputs A, B, and C.

ABC



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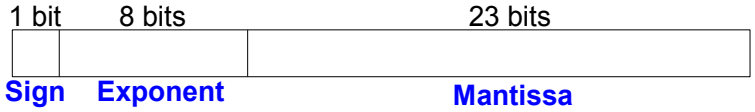
2) [20] Perform floating point addition C= A + B in 32-bit IEEE 754 floating point format




where A = 0x40580000

B = 0x3FD00000

Write the answer C in hexadecimal format. Note that A and B are floating point numbers.

| | S Exponent Fraction |
|---|---|
| A | 0**100 0000 0**101 1000 00… |
| B | 0**011 1111 1**101 0000 00… |

A = **1**.1011 x $2^{128-127}$ = 1.1011 x $2^{1}$

B = **1**.101 x $2^{127-127}$ = 0.1101 x $2^{1}$

```
     1 111 <-carry
     1.1011
+    0.1101
-----------
    10.1000 x 2^1
```

Normalize => 1.01000 x $2^{2}$

S Exponent Fraction

**C** = 0 100 0000 1 010 0000 00…

4 0 A 0 00…

**C=_____0x40A00000_____**

Name:_____

3. [28] In a PCB board design, the output of flip-flop A is buffered and the output signal q is driven 3 cm to the input of flip-flop B. The clk signal and q are carefully laid out next to each other, both traveling with the same speed of $8.0 \times 10^7$ m/sec. The flip-flop and buffer timing parameters are given in Tables 1 and 2 respectively.

Table 1 Flip-Flop Timing Parameters

| | |
|---|---|
| Tpcq | 50 ps |
| Tccq | 10 ps |
| Tsetup | 50 ps |
| Thold | 20 ps |

Table 2 Buffer Timing Parameters

| | |
|---|---|
| Tpq | 150 ps |
| Tcq | 100 ps |

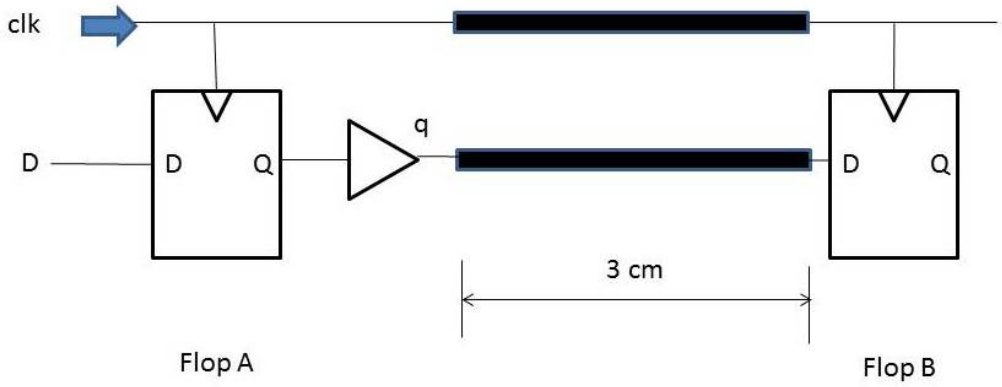



Figure 1

(a) If clk and q travel in the same direction as shown in Figure 1, what is the maximum frequency that the clk can operate?

$T_{skew} = T_{delay} = (3.0 \times 10^{-2})/(8.0 \times 10^7) = 3.75 \times 10^{-10} = 375$ ps

$T_c = T_{pcq} + T_{pq} + T_{delay} + T_{setup} - T_{skew}$

$T_c = 50 + 150 + 375 + 50 - 375 = 250$ ps $= 0.25$ ns

$f_{max} = 1/T_c = 4$ GHz

(b) Is there a hold time problem? Justify your answer.

$T_{ccq} + T_{cq} + T_{delay} > T_{hold} + T_{skew}$

$10 + 100 + 375 > 20 + 375$

$110 > 20 \Rightarrow$ true, therefore no hold time problem

3. (cont.)

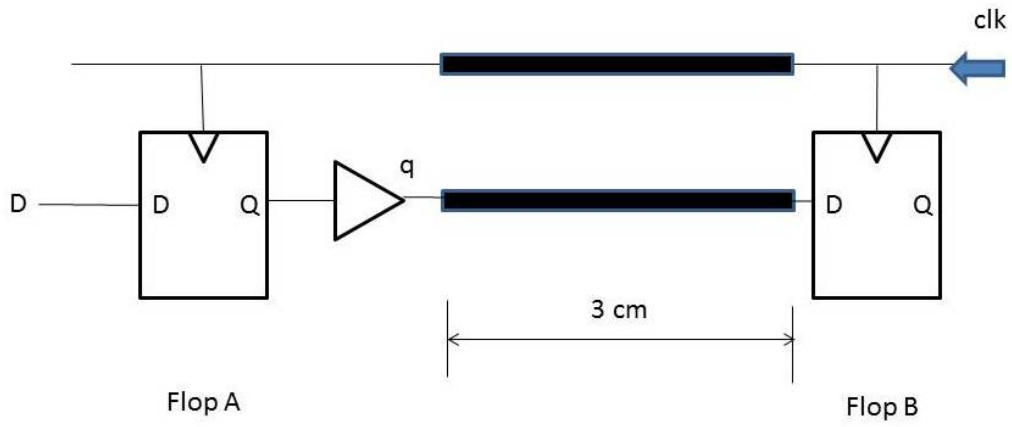



Figure 2

(c) If clk and q travel in the opposite direction as shown in Figure 2, what is the maximum frequency at which the clk can operate?

$T_{skew} = T_{delay} = (3.0 \times 10^{-2})/(8.0 \times 10^{7}) = 3.75 \times 10^{-10} = 375$ ps

$T_c = T_{pcq} + T_{pq} + T_{delay} + T_{setup} + T_{skew}$

$T_c = 50 + 150 + 375 + 50 + 375 = 1000$ ps $= 1$ ns

$f_{max} = 1/T_c = 1$ GHz

(d) Is there a hold time problem? Justify your answer.

$T_{ccq} + T_{cq} + T_{delay} > T_{hold} + T_{skew}$

$10 + 100 + 375 > 20 - 375$

$485 > -355$ => true, therefore no hold time problem

Name:_____

4.[18] A NRZ1 generator for a input data sequence of 1's and 0's is defined as follows:

- For each 0 in the input data sequence, the bit output is the same as the previous bit output.
- For each 1 in the in the input data sequence, the bit output is the complement of the previous output.

For example:

Data input sequence 0 1 1 1 0 0 1 0

Data output sequence 0 1 0 1 1 1 0 0

Assume output is reset to 0 and the input sequence starts at 0.

Design a FSM that generates the output sequence Dout from the input data sequence Din as shown in Figure 4.

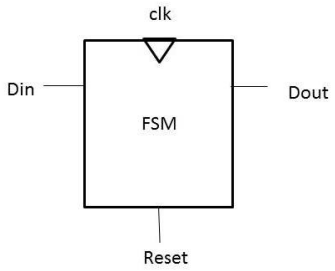
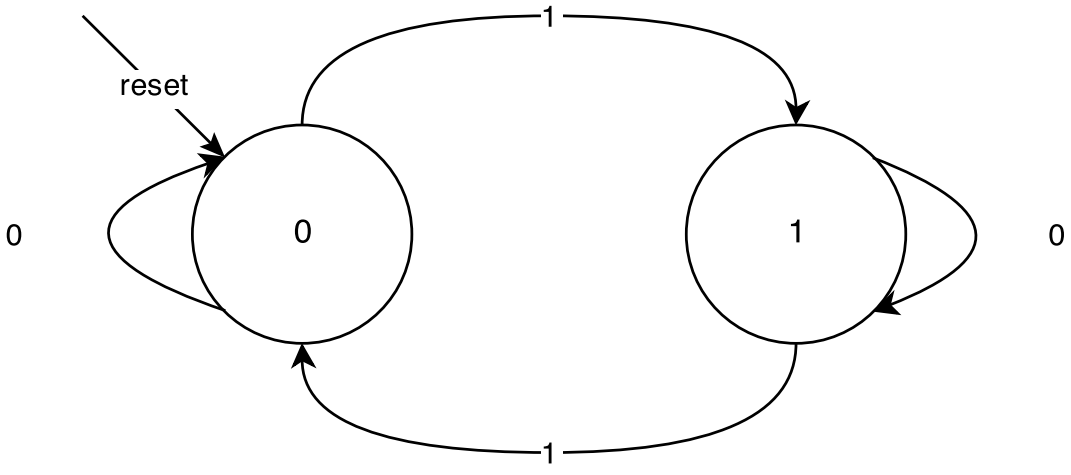


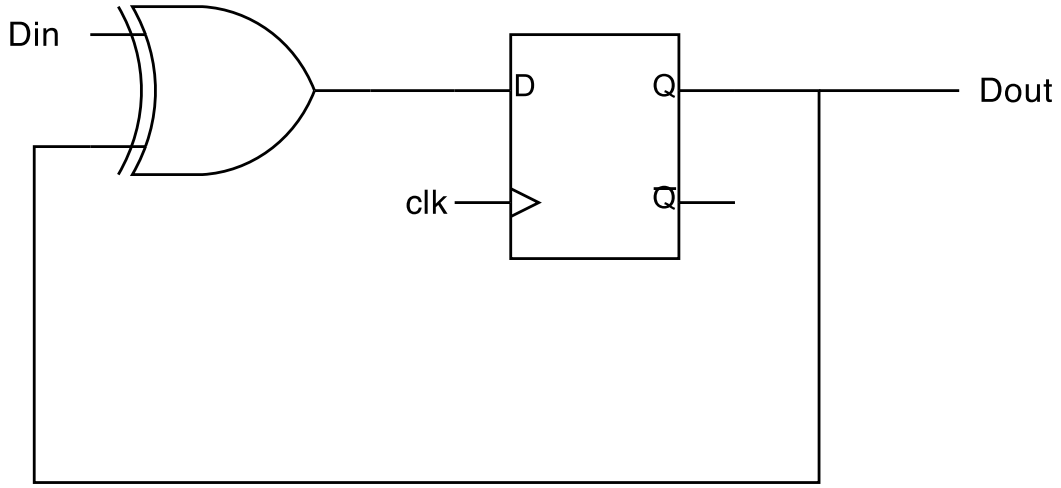

Figure 4

(a) Show state transition diagram.




4. (cont.)

(b) Show a gate schematic for the FSM design.




Next State Truth Table

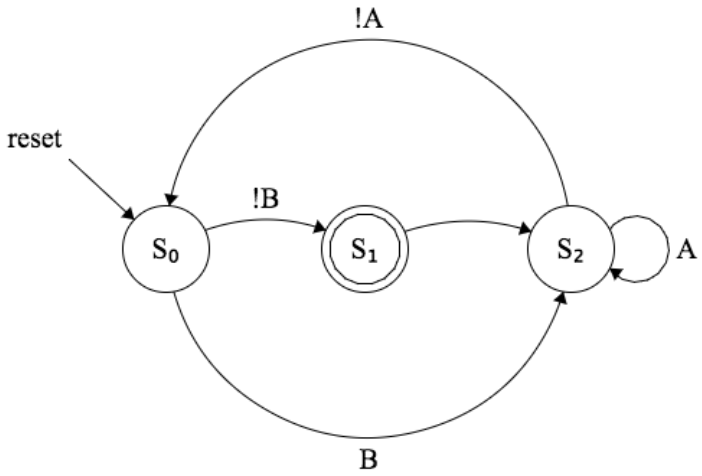
| State | Din | Next State |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Output Truth Table

| State | Dout |
|---|---|
| 0 | 0 |
| 1 | 1 |

Name:_____

5. [10] Create a SystemVerilog implementation of the following FSM. The output (Y) is high in state $S_1$ and low otherwise.




```
module pkb_fsm( input logic A, B, reset, clk,
                output logic Y);
// Put Code Here
     typedef enum logic[1:0] {S0, S1, S2} statetype;
     statetype state, nextstate;

     // state register
     always_ff @(posedge clk)
          if (reset) state <= S0;
          else state <= nextstate;

     // next state logic
     always_comb
          case(state)
               S0: nextstate = B ? S2 : S1;
               S1: nextstate = S2;
               S2: nextstate = A ? S2 : S0;
               Default: nextstate = S0;
          endcase

     // output logic
     assign Y = state == S1;
endmodule
```