Microprocessor-Based Systems (E155)
Fall 2013
Syllabus

Teaching Staff

Professor:	Josef Spjut	josef_spjut@hmc.edu	
	Parsons 2362	Office Hours by Appointment	
Lab Tutors:	Dong-hyeon Park	Joshua Vasquez	Shreyasha Paudel

Schedule:

Lecture:	MW 1:15-2:30
Lab Tutor Hours:	uPs Lab, Saturdays 1-3, Sundays 2-4, 8-10

Textbook:

Harris & Harris, *Digital Design and Computer Architecture*, 2nd Ed., Morgan Kaufmann, 2012. Has some good sections on embedded interfaces in chapter 8.

You will also need to put $80 Claremont cash on your card, see Sydney in the Engineering office to get a receipt and give the receipt to Sam to get your parts kit.

Electronic Communication

Class Web Page:	http://www3.hmc.edu/~jspjut/class/e155
Class Email List:	eng-155-l@hmc.edu

Be sure you are on the class mailing list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-155-l

Alternatively, if you have an electronic version of the syllabus, you can click this paragraph to have your mail client autocomplete the email for you.

You also will need a Harvey Mudd College computer to complete your labs. If you are not a HMC student, email me your full name and school affiliation and I will request an account for you. Your lab work will primarily be performed in the MicroPs lab where 10 stations are available. The ECF may be used for some parts of the labs, but the hardware and power supplies should remain in the MicroPs lab. If you have issues with the software or computer systems, contact the system administrator, Willie Drake. He can often be found in his office inside the ECF, and after-hours contact information is typically posted on his door.

Course Objectives:

- To get hands on experience with digital system design
- To develop debugging skills by designing, building, and testing digital circuits using commercially available CAD (computer aided design) tools
- To design, build, and test your own digital embedded system project on a design team

Grading:
Labs: 50%
Final Project: 45%
Activities: 5%
Labs are graded on a 9-point scale. 3 points are given for the system meeting its specified requirements. Up to 3 more points are given for the cleanliness of implementation (simple, elegant, well-commented code, clean wiring) on the scale of 1 = marginal, 2 = good, 3 = exceptional. Another 3 points are given for answering a "fault tolerance question," with 3 points for a correct answer to the first question, 2 for a second try, and so forth.

As the labs typically involve iterating on your design and modifications from a functional prototype towards adding more features as you develop them, it is extremely useful to maintain your source files using some form of version control. Doug Hu has developed an excellent tutorial on the git software version control system that you can find on Charlie at `charlie.ac.hmc.edu/Clinic/Engineering/Tutorials/Tutorial-Files-2013/GitVersionControl`. You are strongly encouraged to use git or some other form of version control for you labs as it will prevent many headaches from broken updates, and will make it natural to develop as a team when it comes time to work on the project.

Lab checkoffs are to be completed during your scheduled time on Monday or Tuesday of the week the lab assignment is due. As many people have scheduling conflicts with the planned lab times, the checkoffs will be scheduled using the following spreadsheet. If you are late for your appointed time, you may be given a 0 for the lab.

No late labs will be accepted. Late labs are not accepted, but your lowest lab score will be dropped before the average is calculated so if you are sick or have an emergency one week you can drop that lab. However, all labs must still be completed by the project proposal deadline, even if you drop the score. Labs are done individually. You are welcome to discuss them with other students or the instructor after you have made an effort by yourself. Please list the names of other students you have worked with. However, you should turn in your own work, not work identical to that of another person. **It is an honor code violation to simply copy someone else's work.** Solutions to past years labs have been handed out. Obviously, it is also an honor code violation to refer to these solutions while doing your lab. The final project will be done in groups of two.

Tentative Schedule: The schedule below is a tentative plan that may change during the semester. The deadlines, however, are fixed unless otherwise notified; do not assume that they will change just because the lecture schedule changes. Any changes to deadlines will be announced in class and sent to the class mailing list.

Monday	Wednesday	Friday
Sep 2nd Labor Day	4th **1** Class Intro	6th
9th **2** Logic Design	11th **3** Logic Design	13th
16th **4** **Lab 1 Due** Last Day to Add Classes FPGA **Lab 1 - FPGA Board**	18th **5** FPGA Datasheet	20th

Monday	Wednesday	Friday
23rd **6** **Lab 2 Due** Synchronous Logic Design **Lab 2 - Muxed Display**	25th **7** FSM Design	27th
30th **8** **Lab 3 Due** PIC Assembly **Lab 3 - Keypad**	Oct 2nd **9** PIC Programming	4th
7th **10** **Lab 4 Due** PIC Hardware **Lab 4 - Assembly**	9th **11** PIC Interfacing	11th
14th **12** **Lab 5 Due** C Programming **Lab 5 - Audio**	16th **13** C Examples	18th
21st Fall Break	23rd **14** Project Kickoff	25th
28th **15** **Lab 6 Due** VGA Graphics **Lab 6 - Wireless**	30th **16** USB,PCI	Nov 1st
4th **17** **Lab 7 Due** DAC **Lab 7 - VGA & USB**	6th **18** Motors, speakers	8th
11th **19** Network	13th **20** SATA	15th
18th **21** FLASH memory	20th **22** DDR3	22nd
25th **23** Presentations	27th **24** Presentations	29th Thanksgiving
Dec 2nd **25** Presentations	4th **26** Presentations	6th
9th **27** Interview Questions	11th **28** Project Demos	13th Last Day of Classes
16th Finals Week	18th Finals Week	20th Finals Week