TestosterICs: A Low-Cost Functional Chip Tester

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Abstract

Students in VLSI design courses find the opportunity to fabricate their chip designs very exciting and motivational. However, testing the chips after fabrication can be a hassle for both students and faculty. In collaboration with Sun Microsystems Laboratories, we have developed a functional chip tester that applies test vectors at low speed to check logical operation. The tester supports packages with up to 256 pins and operates over a range of 1.2-6.5 volts. It reads test vectors directly from IRSIM files and can be programmed through a Java API. The tester can also be used to drive scan chains and other control signals in conjunction with a high-speed signal generator and oscilloscope to test chips at speed. We have released the chip tester plans in open-source form and manufactured 20 units for other universities.

1. Introduction

For many undergraduates, the opportunity to design, fabricate, and test their own VLSI chips marks the point where they come to feel like "real engineers." The Semiconductor Industry Association and National Science Foundation have provided grants for many years to support chip fabrication in VLSI design classes through the MOSIS service [1]. However, the grants come with the expectation that the chips will be tested. This presents a logistical challenge for many faculty. By the time the chips are received, the course is usually over and grades are assigned. Students need test equipment that is easy to learn and use. A number of commonly used test methods include:

- Breadboard with LEDs and switches
- PC-based digital I/O card
- Logic analyzer and pattern generator
- Commercial IC tester

None of these methods are entirely satisfactory. Breadboards work for very simple combinational logic, but quickly become tedious for more interesting systems. Digital I/O cards allow faster application of test vectors but typically are not fast enough for performance testing, have clumsy user interfaces for chip testing, and operate at fixed voltage levels. High speed logic analyzer / pattern generator combinations cost around $40,000, and commercial IC testers cost an order of magnitude more. Moreover, professional test equipment has a steep learning curve.

The Asynchronous Research Group at Sun Microsystems Laboratories encountered similar problems with chip testing. The group builds asynchronous circuits with multi-GHz throughput that scales with operating voltage and temperature. The chips are configured through scan chains, and then observed on a few high-speed output pins. Although Sun has high-end IC testers, product teams get priority access to the tester time. The group formerly used a MacTester [2] system combined with level conversion boards. Sun Labs sponsored two engineering clinic projects at Harvey Mudd College to build TestosterICs, a better chip tester that supports variable voltage operation, handles more pins, and is easier to use.

2. TestosterICs

Figure 1 shows a photograph of the TestosterICs system. It consists of three parts: the Brain Box, the Device Under Test (DUT) card, and the Pin Electronics Adapters. The Brain Box communicates with a host PC or UNIX workstation via a serial port. The host machine sends test vectors to the Brain Box, which in turn drives them to the device under test and sends the resulting device state back to the computer. The DUT card contains a socket for the device under test; the card in the photograph holds a 16x16 Pin Grid Array (PGA) socket. The four Pin Electronics Adapters drive and sample the pins on the DUT at the desired voltage levels.

We have developed three models of pin electronics adapters: 5V, 3.3V, and variable voltage. The first two contain Xilinx Spartan and SpartanXL FPGAs configured as shift registers to drive and sample the pins. The FPGAs can

sink up to 12 mA of output current per pin at CMOS voltage levels and have proven resistant to ESD and other abuse in the lab. The third uses a custom chip designed by a group of HMC freshmen [3] that contains shift registers, comparators, and level converters to support operation from 1.5 to 6.5 volts. Each adapter controls up to 64 pins on the DUT.

We have developed two DUT cards for 40-pin DIP and 16x16-pin PGAs. The cards consist of the DUT socket, a 15-pin connector to the brain box, connectors for one or more pin electronics adapters, an external power supply (used only with the variable voltage adapters), and header pins for easy access to each DUT pin. The header pins may be jumpered to V_{DD} or GND to provide sturdy power supplies or may be connected to an oscilloscope to observe high-speed waveforms. The user may develop custom DUT cards to provide SMA connectors for very high-speed outputs, to attach to thermal cycling equipment, or to support specialized packages. Figure 2 shows the 40-pin DUT card holding a chip fabricated through MOSIS.

The included TesterGen software tools read IRSIM test vector files and control the Brain Box. The speed is limited by serial port bandwidth to about 240 vectors/s (or about 3000 vectors/s in a special high-speed mode in which each vector toggles only one pin). As students can use the same test vector files for pre-tapeout simulation in IRSIM and post-fabrication testing on TestosterICs, there is no time wasted learning new tools or rewriting tests. TestosterICs also has a Java API for more flexible control of the chip tester. The following code tests an inverter on a 7404 chip.

```
pindef vdd 40       # define pin numbers
pindef gnd 7        # for power, ground,
pindef a1 1         # inputs, and outputs
pindef y1 2         # (in 40 pin DIP socket)
h a1                # set input high
s                   # sim step (apply input)
assert y1 0         # report if output is not 0
l a1                # set input low
s
assert y1 1         # report if output is not 1
```

3. Testing Results

At Harvey Mudd College, seven teams of students have used the chip tester over the past two years. Before the chip tester, students wirewrapped test fixtures and took many weeks to test chips. Now, most teams complete their testing in under an hour. They begin by reading the manual, which provides a brief tutorial demonstrating how to test a 7404 inverter chip. They then locate their test vector file, define the pinout, and apply it to their own 40-pin DIP TinyChip.

4. Manufacturing

Sun Laboratories placed the results of the chip tester clinic projects in the public domain. We have improved upon the original design and now distribute TestosterICs using an open-source model so that other universities may use the tester and improve upon it. We have also started a small company to manufacture testers at a reasonable cost. At the time of writing, nine testers are in use (including at Sun, HMC, Notre Dame, Harvard, and Yale) and we need to sell about three more to break even. As David Diaz is interested in becoming an entrepreneur, this project has been a unique educational experience throughout his four years at HMC. For more information, see the One Hot Logic LLC web site [4].

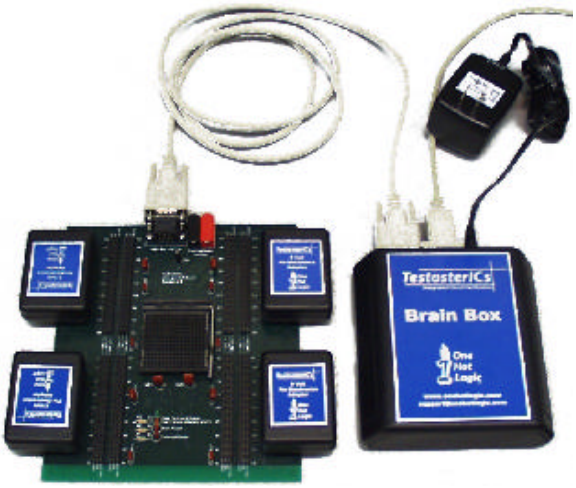

Figure 1: TestosterICs system

Figure 2: 40-pin DUT card

Acknowledgments

TestosterICs development has been supported by Sun Microsystems Laboratories. Numerous Harvey Mudd students have worked on the project.

References

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