Comparison of Noise Tolerant Precharge (NTP) to Conventional Feedback Keepers for Dynamic Logic

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ABSTRACT

Dynamic logic requires some sort of keeper to prevent the output node from floating and to provide acceptable noise immunity. A number of recent papers have advocated using a very weak complementary pMOS network in place of the conventional feedback keeper; such a technique is called Noise-Tolerant Precharge (NTP). This paper compares the delay and noise margin of NTP with conventional feedback keepers. Although NTP is more robust in that it can recover from a dynamic noise event, it is also 5-50% slower than conventional feedback keepers with the same static noise margin.

Categories and Subject Descriptors

B.7.1 [Integrated Circuits]: Types and Design Styles - VLSI

General Terms: Design, Performance, Reliability

Keywords: dynamic logic, keepers, static noise margin

1. INTRODUCTION

Dynamic logic is popular in high-speed applications. Keepers are required to counter leakage and deliver acceptable noise margins. Figure 1(a) shows a footed dynamic gate with a conventional feedback keeper. A number of authors have proposed replacing the keeper with a weak complementary pMOS network shown in Figure 1(b). The technique has been variously called Noise Tolerant Precharge (NTP) [1], [2] or Monotonic CMOS [3]. Skewed CMOS [4] is a closely related technique alternating one NTP stage for every two skewed static CMOS stages. The authors have claimed better performance for the same noise margin. Moreover, NTP can recover from dynamic noise events that are large enough to flip the output state. If these claims are accurate, domino designers should find NTP a compelling improvement over the conventional feedback keeper. This paper compares the delay and static noise margin of dynamic logic using the conventional feedback keeper to that using NTP. It finds that the feedback keeper is consistently faster for the same noise margin.

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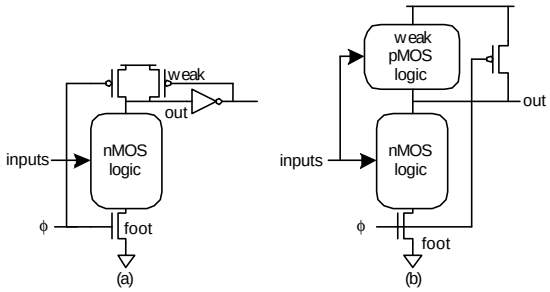

Figure 1: Dynamic gates with (a) conventional feedback keeper and (b) noise tolerant precharge

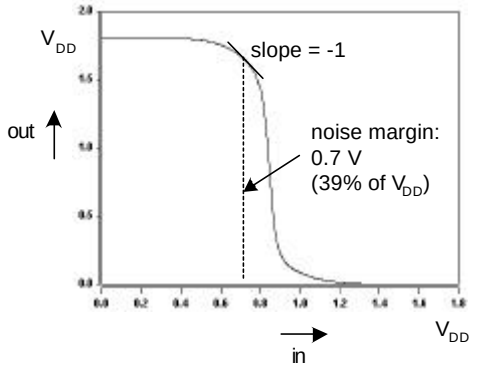

Figure 2: Inverter DC transfer characteristics

The propagation delay of a dynamic gate is defined from the last input rising through 50% to the dynamic output falling through 50%. The static noise margin is the leftmost of the two points on the DC transfer characteristic where the slope is –1. For example, Figure 2 shows that the static noise margin of a static CMOS inverter with 2/1 P/N ratio is about 39% of V_{DD} under the simulation conditions given in Section 2. A dynamic gate without a keeper has almost zero static noise margin because the output will discharge through subthreshold conduction. Even if subthreshold conduction is zero, the static noise margin would be V_t. A keeper significantly improves the static noise margin at a slight expense in delay.

The conventional feedback keeper uses an inverter and weak pMOS transistor to hold the output high. When the dynamic gate evaluates, the keeper fights the transition, increasing delay until the keeper turns off. The NTP technique uses a weak

complementary pMOS network. As the inputs rise, the pMOS transistors turn off immediately, reducing contention. However, a complex stack of pMOS transistors increases the input capacitance as well as the parasitic capacitance on the output node.

When an input glitch flips the output, the conventional keeper turns off so the output will never recover. NTP provides an extra advantage of pulling the output back high. The recovery takes too long to be of help at high frequency, but at least permits low-frequency debug. Therefore, if delay and noise margin were equal, NTP would be preferred.

Many other keeper techniques have been proposed in the literature, including a "leaker" that is always ON, input-controlled refresh [5], the inverter technique [6], pMOS pull-up technique [7], mirror technique [8], twin-transistor technique [9]. This study is restricted to conventional keepers and NTP.

Section 2 precisely describes the experimental method. Section 3 presents the results, showing that the feedback keeper is consistently faster. Section 4 discusses the discrepancies between this and prior work.

2. EXPERIMENTAL METHOD

We simulated the circuits in HSPICE using the TSMC 180 nm process at 1.8 V and 70 °C. The process has a FO4 inverter delay of 74 ps and an nMOS threshold voltage V_t of about 0.35 V. The simulation setup is shown in Figure 3 and examples of the devices under test are shown in Figure 4. Transistor widths are selected for a fanout-of-4 at each stage. The input capacitance of each dynamic input is equivalent to one 48λ (4.32 μm) wide transistor. This means that the nMOS input transistors are 48λ wide on conventional keeper gates. The pMOS precharge transistor has approximately half the strength of the evaluation stack. The keeper transistors have a width of 48*s*, where *s* is a scale factor that affects the delay and noise margin (typically on the order of 0.1-0.2). For NTP gates, the nMOS transistors are 48(1-*s*) wide so the total input capacitance is the same as that of the gates with conventional keepers. The HI-skew inverter after the dynamic stage has a 4:1 P/N ratio to favor its rising output. Delay and static noise margin are measured between *in* and *out*. On multiple-input gates, *in* is attached to the transistor closest to the rail, while all other inputs are tied to V_{DD} or GND as appropriate.

3. RESULTS

Figure 6(a-e) plots the delay vs. noise margin as *s* is swept from 0.06 to 0.3. Delay is measured in picoseconds and static noise margin is measured in percentage of V_{DD}. Each plot shows footed and footless dynamic gates with conventional keepers and NTP. Footless gates omit the clocked evaluation transistor. The figure considers NOT, NAND2, NAND4, NOR2, and NOR4 functions. Observe that in all cases the conventional keeper is faster for the same noise margin.

Figures 6(f-g) plot delay vs. number of inputs for footed and footless NAND and NOR gates. *s* is selected to give a noise margin of 0.45 V (25% of V_{DD}) in each case. *s* is typically 0.11-0.14 for feedback keepers to obtain this noise margin. For NAND gates, the conventional feedback keeper is 5-9% faster than NTP, which requires comparable values of *s*. For NOR gates, the conventional feedback keeper is 21-49% faster than NTP because

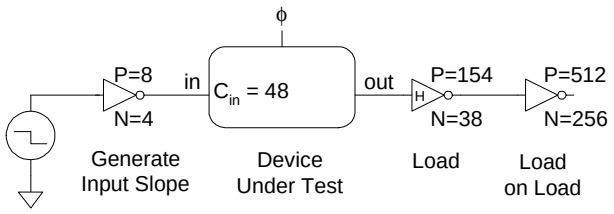

Figure 3: Simulation setup

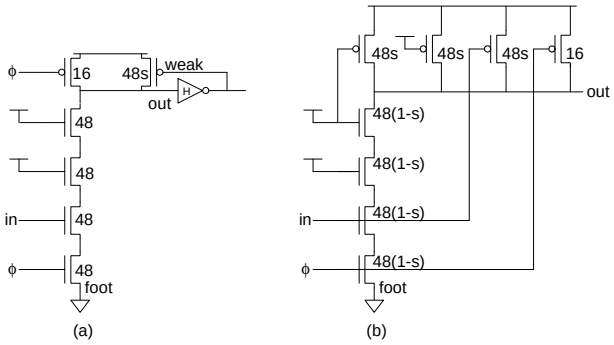

Figure 4: Footed NAND3: (a) conventional feedback keeper, (b) noise tolerant precharge

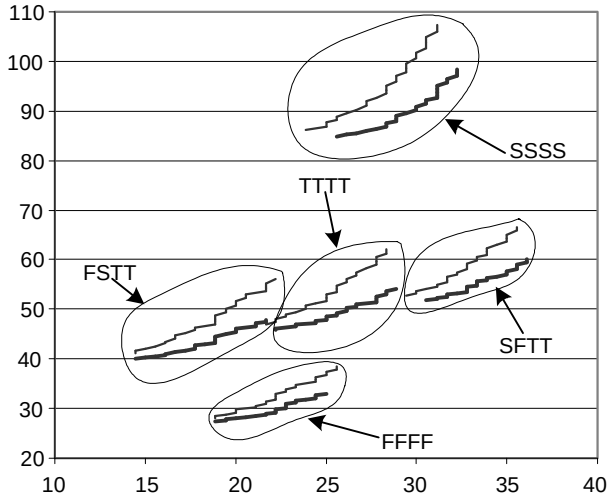

Figure 5: Delay vs. NM across process corners

the NOR gates require a large series stack of pMOS transistors (*s* = 0.24-0.44) that loads the inputs.

Figure 6(h) shows the delay vs. noise margin for footed NAND2 gates for TSMC 180 nm (1.8 V), 250 nm (2.5 V) and 350 nm (3.3 V) processes using models from MOSIS. The conventional keeper is consistently faster. The noise margin is better for the newer processes because the threshold voltage is a larger percent of the supply voltage.

Figure 5 is similar to 6(h) but compares across process corners (nMOS, pMOS, voltage, temperature). Heavy lines represent the conventional feedback keepers, which are consistently faster across all corners.

4. DISCUSSION

Murabayashi [2] found that NTP was 9-21% faster than a conventional feedback keeper for the same noise immunity. However, it was unclear if the gates had the same input capacitance. Moreover, the method of selecting transistor sizes to achieve equal noise immunity was not reported and neither were the actual noise margins.

Thorp [3] found that NTP was comparable in performance to feedback keeper circuits that performed logic in place of the HI-skew inverter. However, the NTP circuits were footless while the feedback keeper circuits were footed [Thorp, personal communication]. By implication, footed NTP should be slower than conventional footed domino.

Figures 6(a-e) show that at both ends (s = 0.06 and s = 0.3) the feedback keepers are faster and have at least as good noise margin as NTP. We can understand the results intuitively by thinking about the DC and step responses of both techniques.

The static noise margins are slightly larger than V_t. At this input voltage, the pMOS device in NTP sees reduced gate overdrive. However, the feedback keeper is isolated by the output inverter and sees nearly full gate overdrive. Therefore, for the same value of s, the feedback keeper delivers more restoring current and hence would be expected to have better noise margin. For NOR circuits, the series pMOS transistors further degrade NTP noise margins.

The delay is determined by the current available to discharge the output node. In NTP, this nMOS stack delivers a current proportional to (1-s). For a step input, the pMOS transistors turn off immediately and do not fight the pulldown. For feedback keeper circuits, the nMOS stack delivers a current proportional to (1). The pMOS keeper of width s fights the pulldown through most of the transition. If pMOS transistors have about half the mobility of nMOS, this leaves a net current of (1-s/2) to discharge the output. Thus we should expect that for the same value of s, the feedback keeper will also be faster.

In summary, NTP is attractive because it can recover from dynamic noise events that flip the output. Unfortunately, this robustness comes at the expense of performance. For NAND gates, it is slightly slower than the conventional feedback keeper with the same static noise margin. For NOR gates, it is much slower than the conventional feedback keeper because the series pMOS transistors must be rather large to achieve acceptable noise margin and thus significantly load the inputs. As a final caveat, NTP is subject to race conditions when delayed-reset domino techniques are used if the inputs precharge before the gate completes evaluation.

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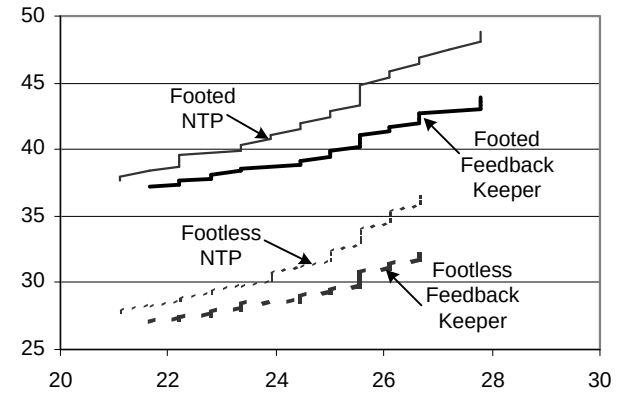
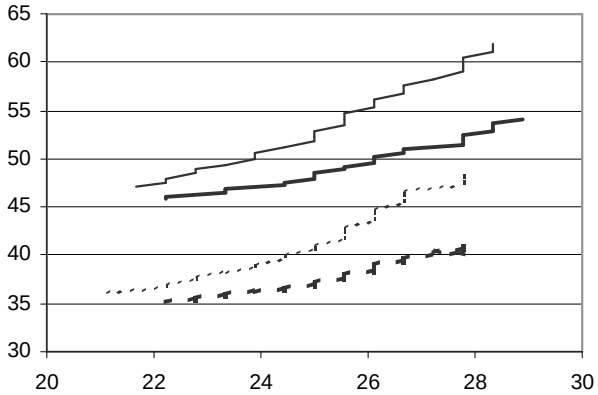
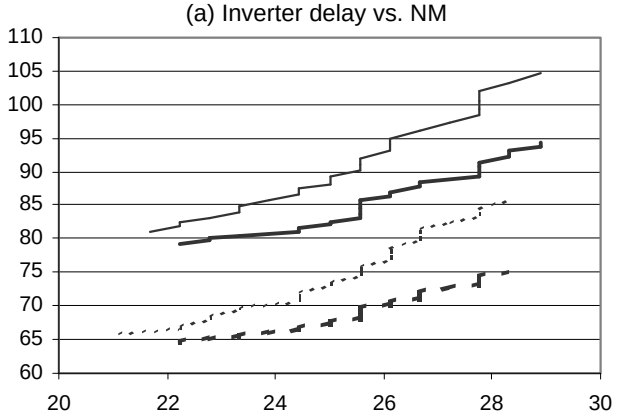


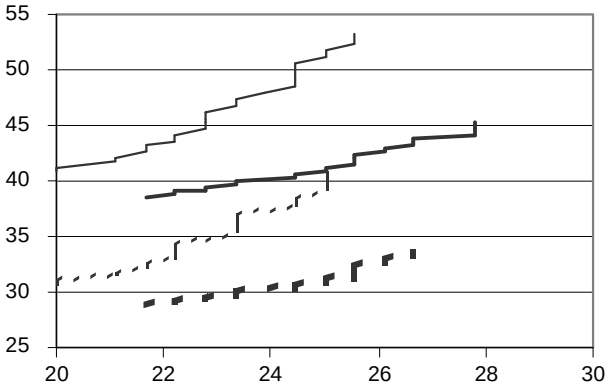
(a) Inverter delay vs. NM



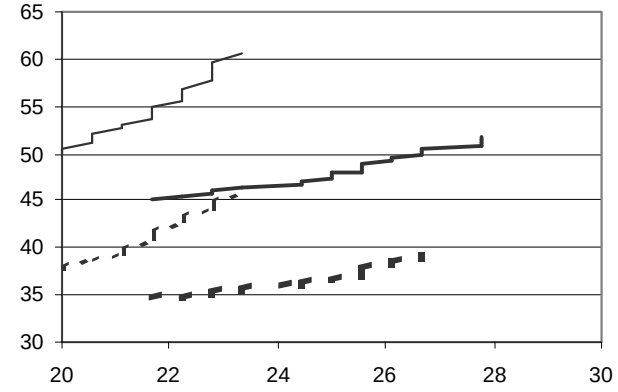
(b) NAND2 delay vs. NM



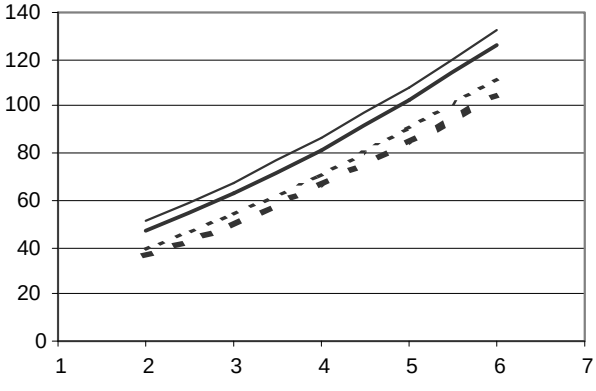
(c) NAND4 delay vs. NM



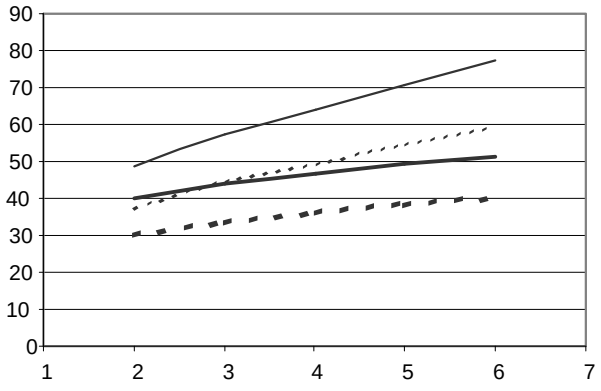
(d) NOR2 delay vs. NM



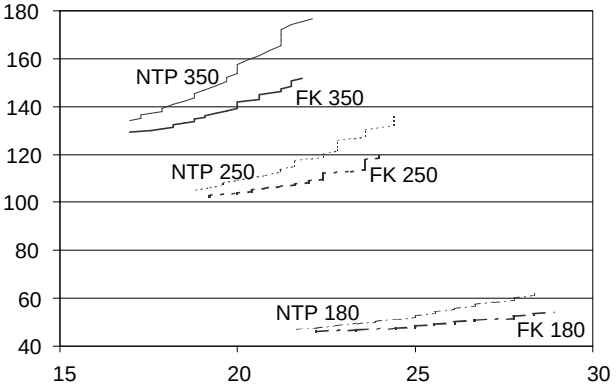
(e) NOR4 delay vs. NM



(f) NAND delay vs. number of inputs (NM=25%)



(g) NOR delay vs. number of inputs (NM=25%)



(h) NAND2 delay vs. NM across processes

Figure 6: Simulation results