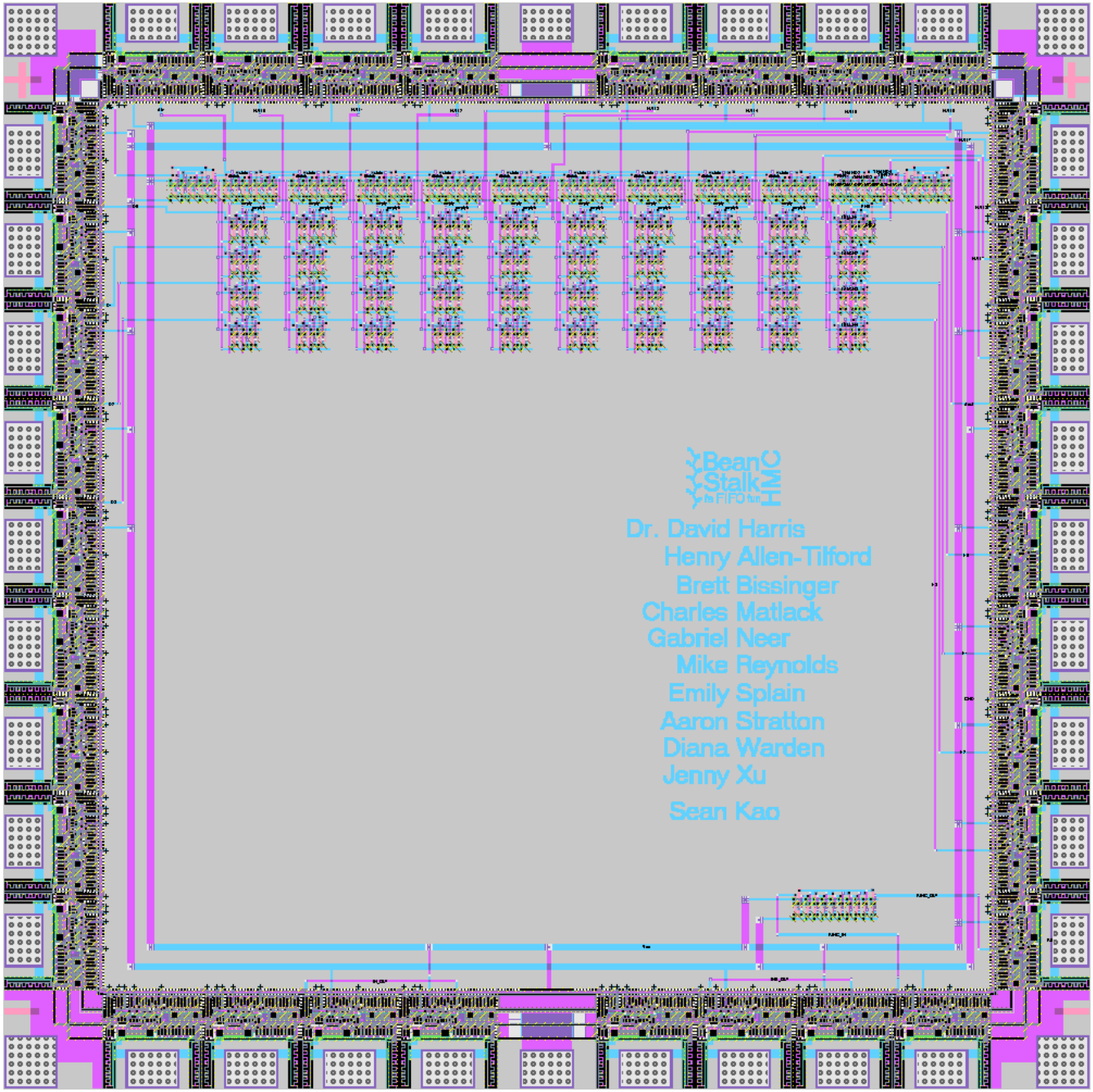
Beanstalk Chip Report

David Harris & Brett Bissinger

December 2, 2000



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Introduction

The Sun Microsystems 2000-2001 Harvey Mudd College Clinic Team is building an asynchronous FIFO demonstration board meant as a teaching tool to illustrate how asynchronous communication can provide a low latency, high throughput communication link between chips that is immune to phase or frequency errors between the transmitter and receiver. The clinic team is constructing one FIFO with a Xilinx Spartan FPGA. They requested the freshmen in the Fall 2000 FYS1 Digital Electronics and Chip Design seminar to construct a second FIFO using a custom integrated circuit.

This report documents the custom chip, named Beanstalk, alluding to ϕFIFOfum, or fiFIFOfun, depending on one's mood. Beanstalk was developed by eight freshmen in the seminar: Henry Allen-Tilford, Brett Bissinger, Charles Matlack, Gabriel Neer, Mike Reynolds, Emily Splain, Diana Warden, and Jenny Xu. Aaron Stratton was the sophomore lab assistant. Sean Kao, from the Sun clinic team, provided specifications and technical assistance.

Beanstalk is implemented on a MOSIS 2.2x2.2 mm TinyChip in the AMI 1.5 micron process ($\lambda = 0.8$) in a 40-pin package. It is the first chip to be taped out from Harvey Mudd College using the Electric CAD system. Thanks to Steve Rubin for speedy bug fixes and tool enhancements.

This chip report describes the ASP* pipeline organization and test structures on the chip. It then presents the verification methodology used for the chip. It presents the pinout diagram, a summary of the files used in the design, and the procedure used for tapeout. Finally, it contains schematics and layout of all the cells in the design.

Specifications

The Beanstalk chip implements a 10-stage ASP* FIFO with a 4-bit datapath. It accepts a 4-bit input and a request Rin. It pulses an acknowledgment Ain when Rin is toggled. The FIFO delivers a four-bit output each time the acknowledgement Aout is toggled. It also produces 10 full signals so the fullness of the FIFO may be gauged.

Inputs	Outputs
Rin	Ain
Aout	
D0, D1, D2, D3	E0, E1, E2, E3
	Full0, …, Full9

The ASP* FIFO uses a pulse-based protocol described in [1] as specified by the Sun Microsystems 2000-2001 Clinic Team.

The Beanstalk chip also includes test structures to verify the pads and basic gates because this is the first chip being produced using the MOSIS padframe and Electric. The test structures include an enablable ring oscillator, an input connected directly to an output pad, and an inverting input connected directly to an output pad. They have the following signals:

Inputs	Outputs
ringin (1 = ring oscillator enabled, 0 = disabled)	ringout (9 stage ring oscillator)
straightin	straightout (same as straightin)
straightinb	straightoutb (complement of straigtinb)

Verification

The chip was verified in a number of ways.

The chip was CIFFed out. The checksum code appears to match the code from MOSIS. It was read into Magic for further verification. Magic seemed to have a problem with the io pads where an n diffusion abutted a substrate contact. Magic seems to have incorrectly extracted this as a short to ground. The substrate contact had to be reshaped in Magic to avoid touching to correctly extract the io pad. This change was not propagated back to the master CIF.

Network Consistency Check was run flat and hierarchically on the fifo cell checking options to ignore power and ground, use port names, and check port order. It passed both. This caught a bug that the latch output had been taken from qb rather than q in the original layout. NCC also passed in both modes on the ringosc cell.

Electrical Rule Check was run on the fifo layout. It found the farthest distance from a contact to be about 30 and found 636 total transistors. It also passed on the ring oscillator layout. It hung while running on the top level chip.

Design Rule Check was run on the entire layout with the pads and logo deleted. It passed with two levels of metal in the moscmossub process with no stacked vias allowed. This required some minor edits from the version in early December because the two-level metal rules require a spacing of 4 rather than 3 between metal2 lines. DRC produced some warnings in Magic. These appear to be problems with wires off grid and thus we ignored them.

The schematics of the fifo and ring oscillator simulated correctly in Electric. The simulator hung on the fifo layout.

The ring oscillator and io pads simulated successfully with IRSIM from extracted CIF layout read by Magic. The io pads don't have vdd or gnd labled, so the approprate nodes w_n129_n115# and a_n126_n36# had to be explicitly forced high and low. Also, all three test structures simulated in their entirety in IRSIM from extracted CIF of the top-level chip. The fifo would not simulate in IRSIM, apparently due to initial condition problems.

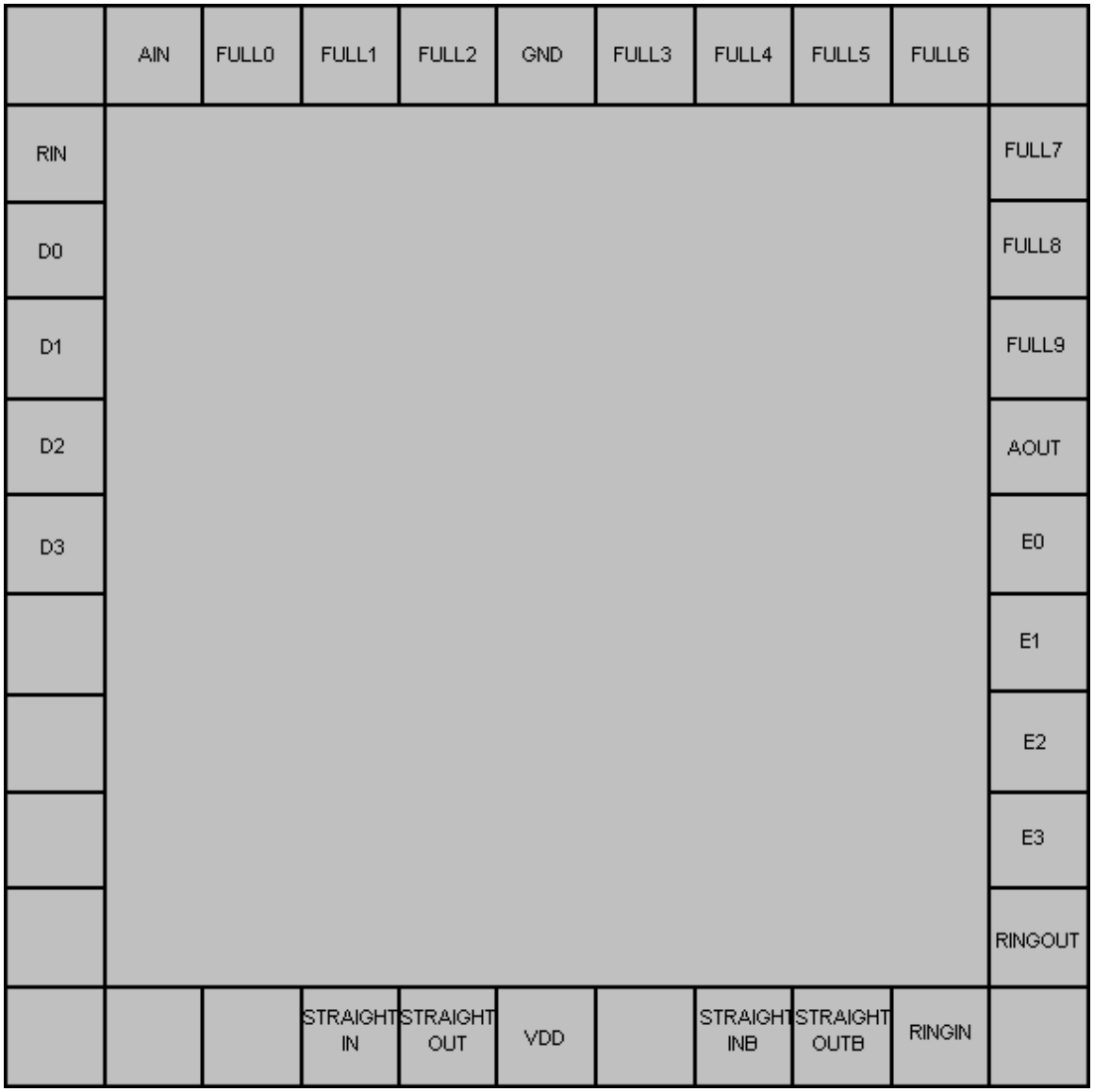
They fifo also would not simulate in WinSpice3 on NT netlisted directly from Electric on account of convergence problems.

Testing Results

The ring oscillators on all chips were operational.

None of the FIFOs were operational. This appears to be a timing problem.

Pinout Diagram



Also note that the upper two corner pads are VDD and the lower two corner pads are GND.

Summary of Files

NT

The master files needed to recreate the project are on Prof. Harris' machine at:

D:\Classes\chipseminar\Fall 2000\Electric\Beanstalk

They include the four master Electric libraries:

beanstalk.elib: the top-level design
mosispads.elib: the pads imported from MOSIS CIF for the 1.5 μm AMI TinyChip.
logo.elib: the chip logo
brettmike.elib: the fifo and ring oscillator designed by Brett Bissinger, Mike Reynolds, and co.

They also include the master CIF file:

beanstalk.cif

Unix on CHIPS

In the ~harris/class/fys/fall2000 directory on chips are versions of the design used for verification. They are slightly out of date; the fifo layout has been modified to clean up a metal2 DRC problem and swap q and qb on the latch. The directories on chips include:

cif: the slightly outdated beanstalk.cif

magic: imported CIF, extracted

sim: ext2sim files and the scmos parameter files for IRSIM

spice: ext2spice files, unsimulated

Tapeout Instructions

On NT:

ERC, verify that substrate and well contacts are close to all devices
Clear valid DRC dates and DRC top level (problems come from pads and logos)
Clear valid NCC and compare flat and hierarchically checking port order and name bug
ignoring power
CIF out with following layer map:
Metal: CMF, CMS
Contacts: CCC for active and polysilicon
(this leads to lambda = 80 CIF units)
check that file length is in the 100's of KB or more and last two lines are
```
C 116; (or something where 116 happened to be the top cell)
E
```

FTP to chips

On Chips:

magic
:cif istyle lambda=0.8(nwell)
:cif read ../cif/beanstalk
expect complaints about CWP layer and nonmanhattan paths in logo
:drc why
look for errors. expect to have some from ½ lambda snapping.
clean up via on flat surface errors; Electric doesn't check that well
:ext style lambda=0.8(scna_ami)
:extract

io p node substrate contact abutting. magic incorrectly extracts this as a short to gnd. must modify substrate contact to extract io pad ok.

ext2sim beanstalk.ext
to generate sim file for IRSIM. Also generate file for inverters
irsim scmos100.prm beanstalk.sim ***.cmd
don't have the lamdba = 0.8 tech file, so use lambda = 1.0 and lambda = 0.6
test chip

Submitting to MOSIS:
Use Web forms at: https://www.mosis.org/Webforms/menu-webforms.html

New Project:
Account #: 2685 (from 2000-2001 donation)
Accoutn Password: RCFTSTM
Design Name: beanstalk
Design Password: fifo
Net Address: David_Harris@hmc.edu
Run Type: shared
Phone: 909-607-3623
Tech Code: SCNE
Foundry: AMI
Design Size: 2203 x 2203
Lambda: 0.80
Pad Count: 40

Get back design number (61517 in this case)

Fabricate Form:
Design Number: 61517
Design Password: fifo
Layout Format: CIF
Compression: uncompressed
Checksum Type: CRC
Checksum:4188899861 Count: 179078 (these come from Electric when CIFfing out)
FTP Send Host: 134.173.32.20 (this is orion, and is the only way we seem to get through the firewall)
FTP Send Password: fifo
FTP Send Filename: beanstalk.cif

send file:
ftp to ftp.design.mosis.org from orion
user: 61517, password fifo
put beanstalk.cif
should see:

226- ASCII transfer completed. Checksum matches.
226 Project state: BEING CHECKED

should get email with the following project check warnings:

Missing layer: POLY2

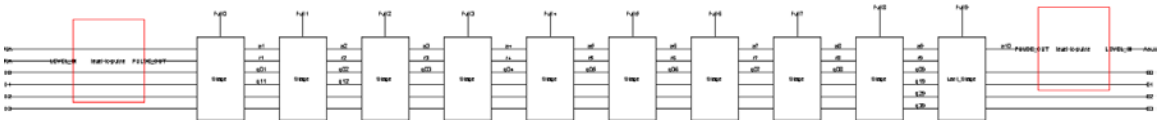
Design pad location is symmetric; bonding orientation assumed
same as submitted design file

References

[1] ASP* paper from Sun ***

Schematics

fifo:



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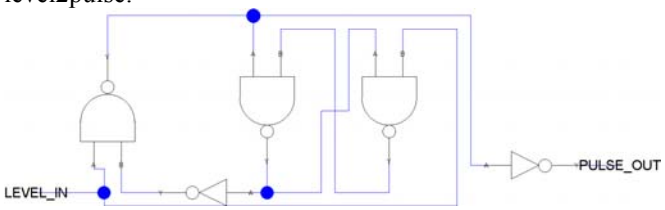

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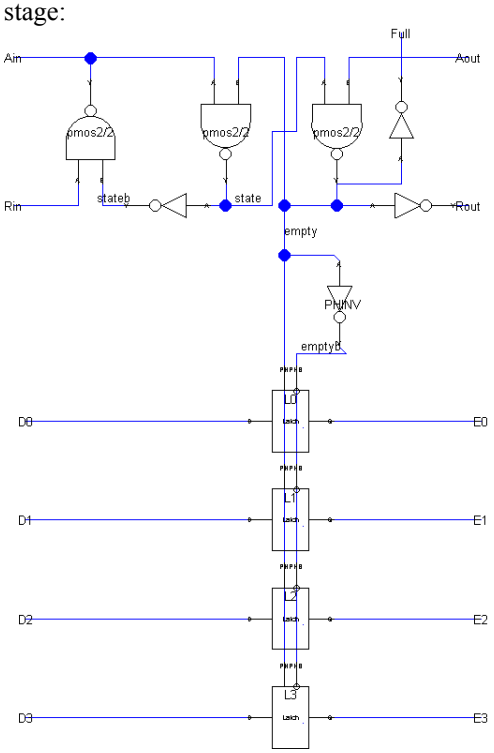

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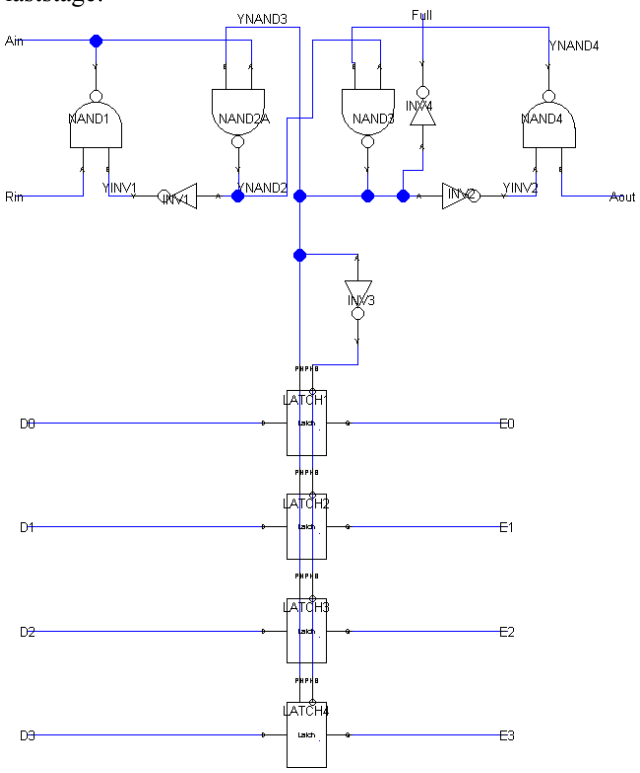
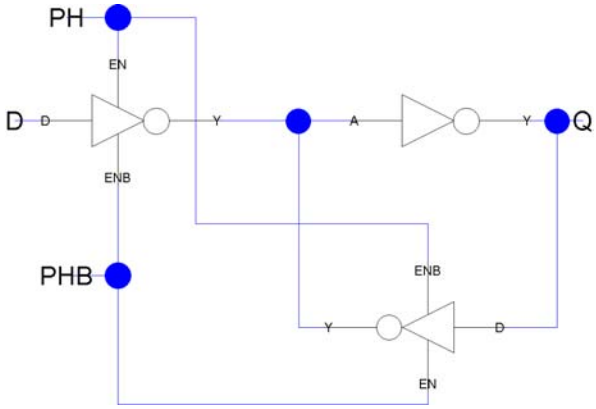
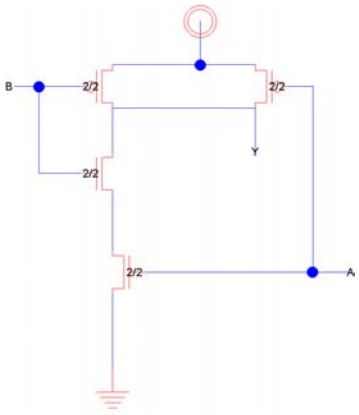


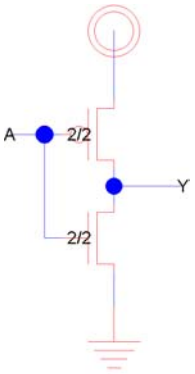
latch:



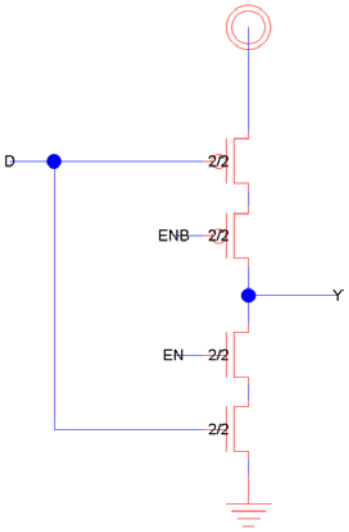
NAND2:



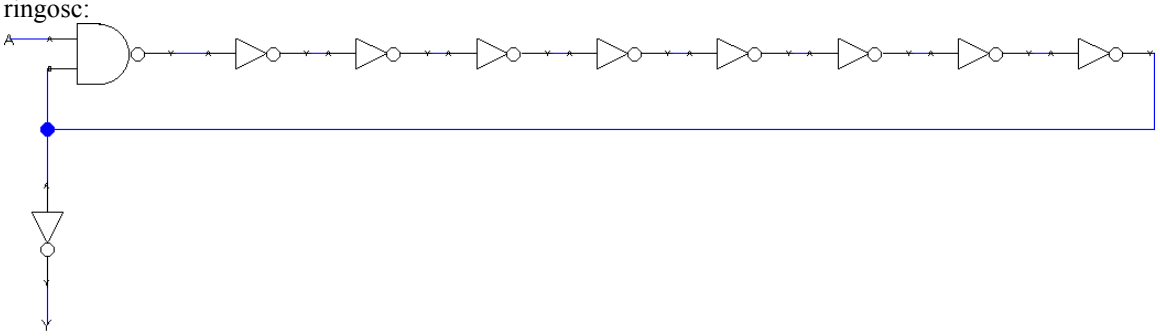
INV:



TRI:



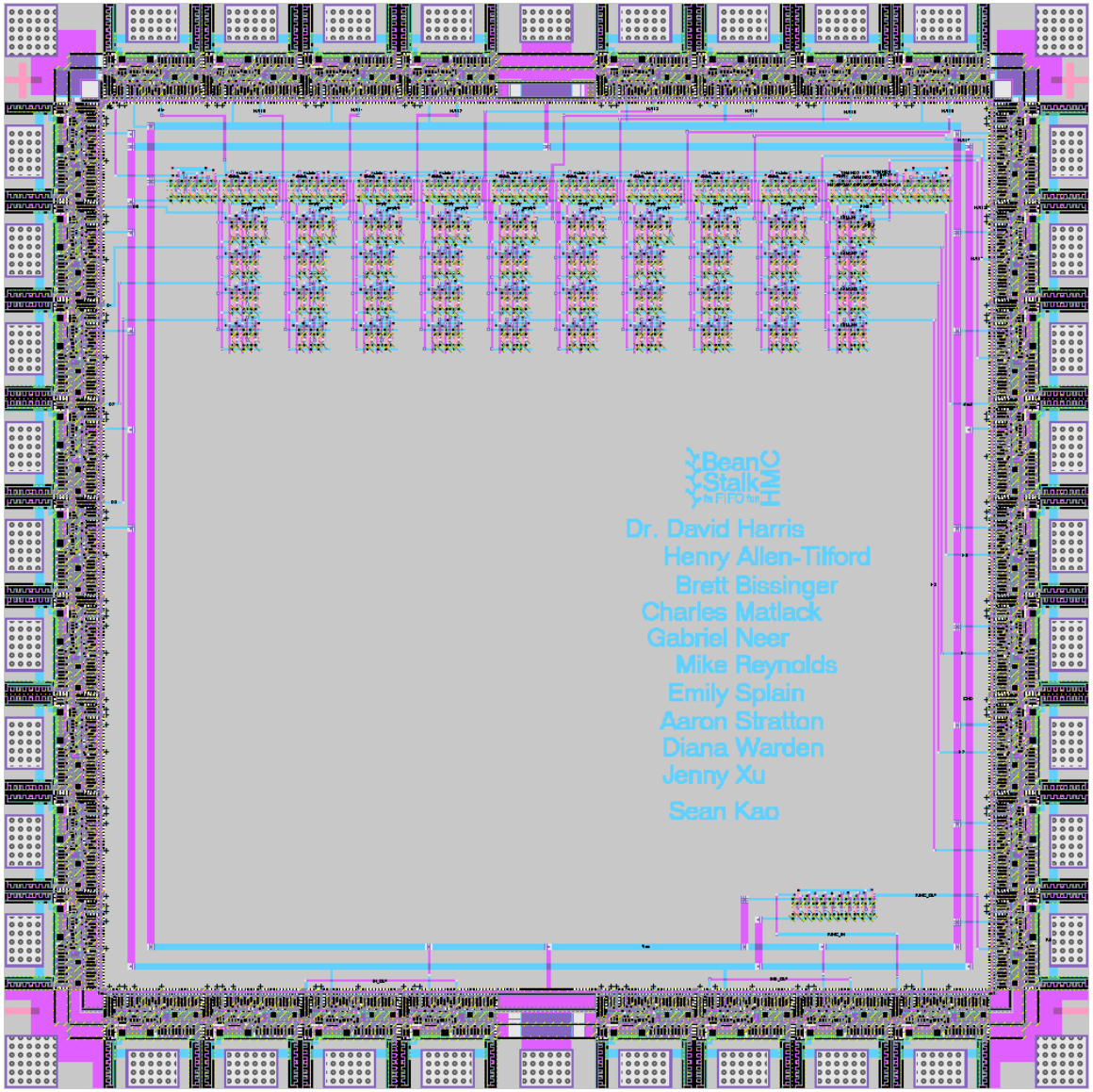
ringosc:



Layout

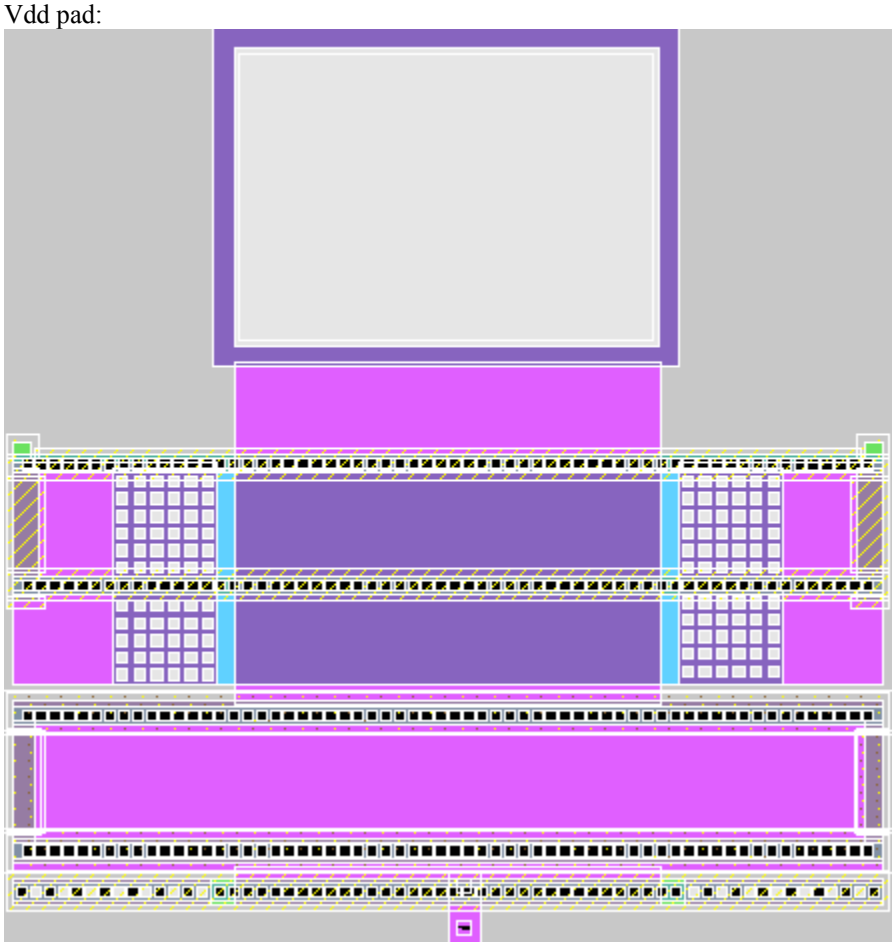
This file includes layout of all the facets:

beanstalk:

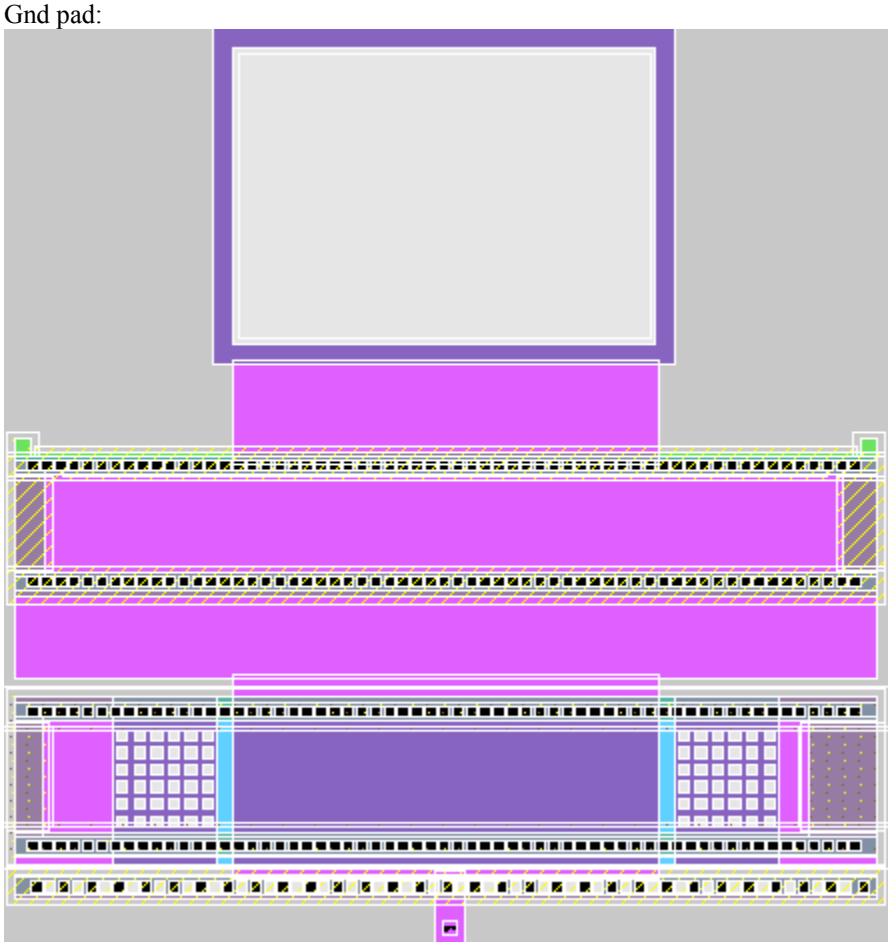


(I've fixed this one but the rest need to be recopied and pasted to get rid of lines. dh 12/24/00) ***

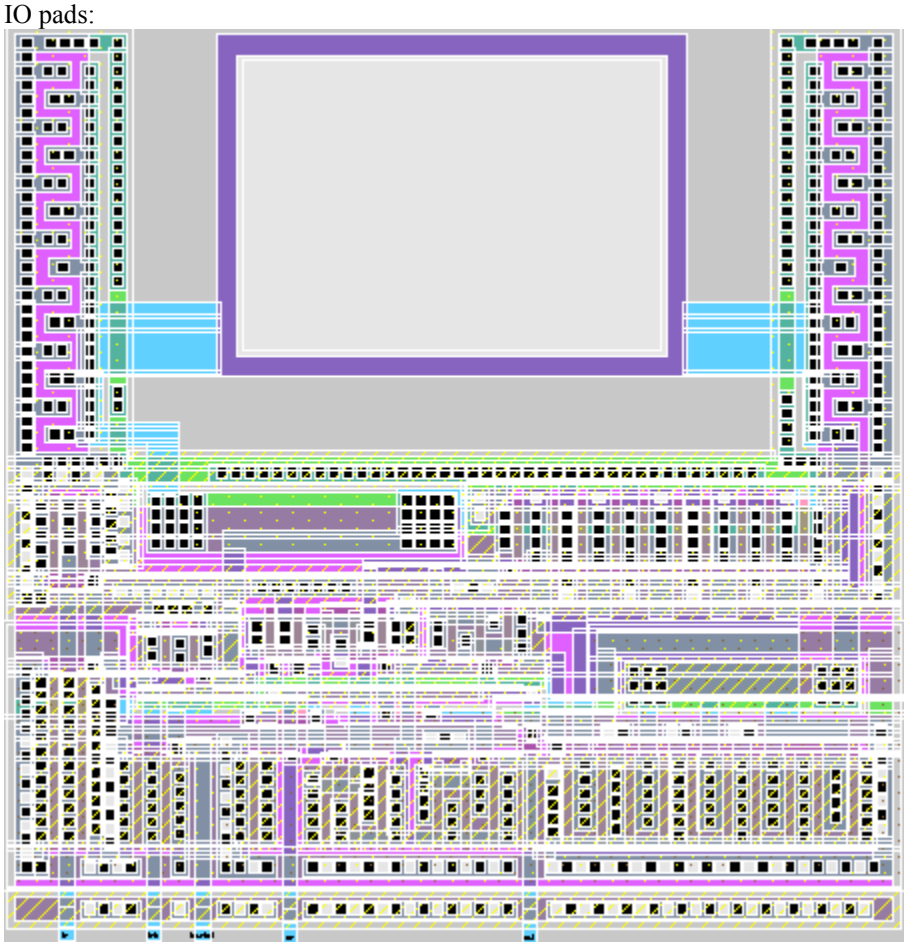
Vdd pad:



Gnd pad:



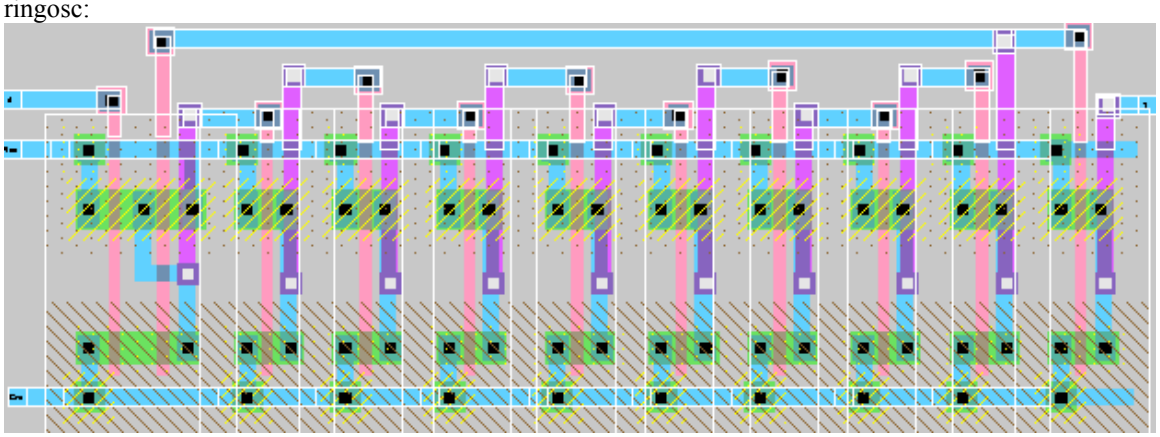
IO pads:



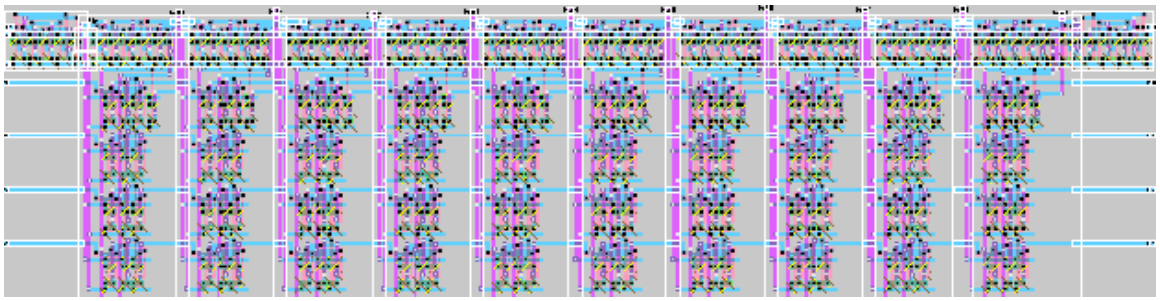
logo:


BeanStalk
to FIFOrm
Dr. David Harris
Henry Allen-Tilford
Brett Bissinger
Charles Matlack
Gabriel Neer
Mike Reynolds
Emily Splain
Aaron Stratton
Diana Warden
Jenny Xu
Sean Kao

ringosc:



fifo:



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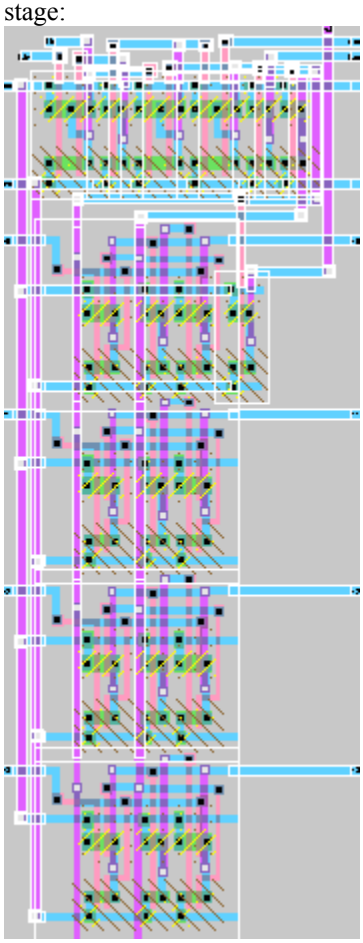

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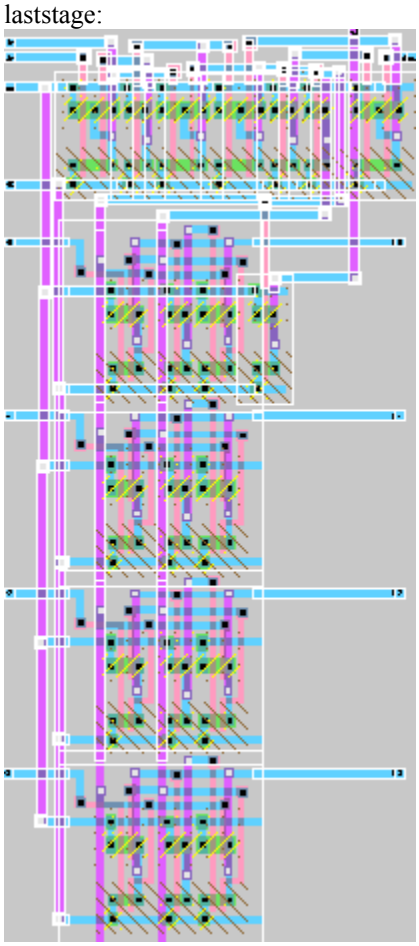
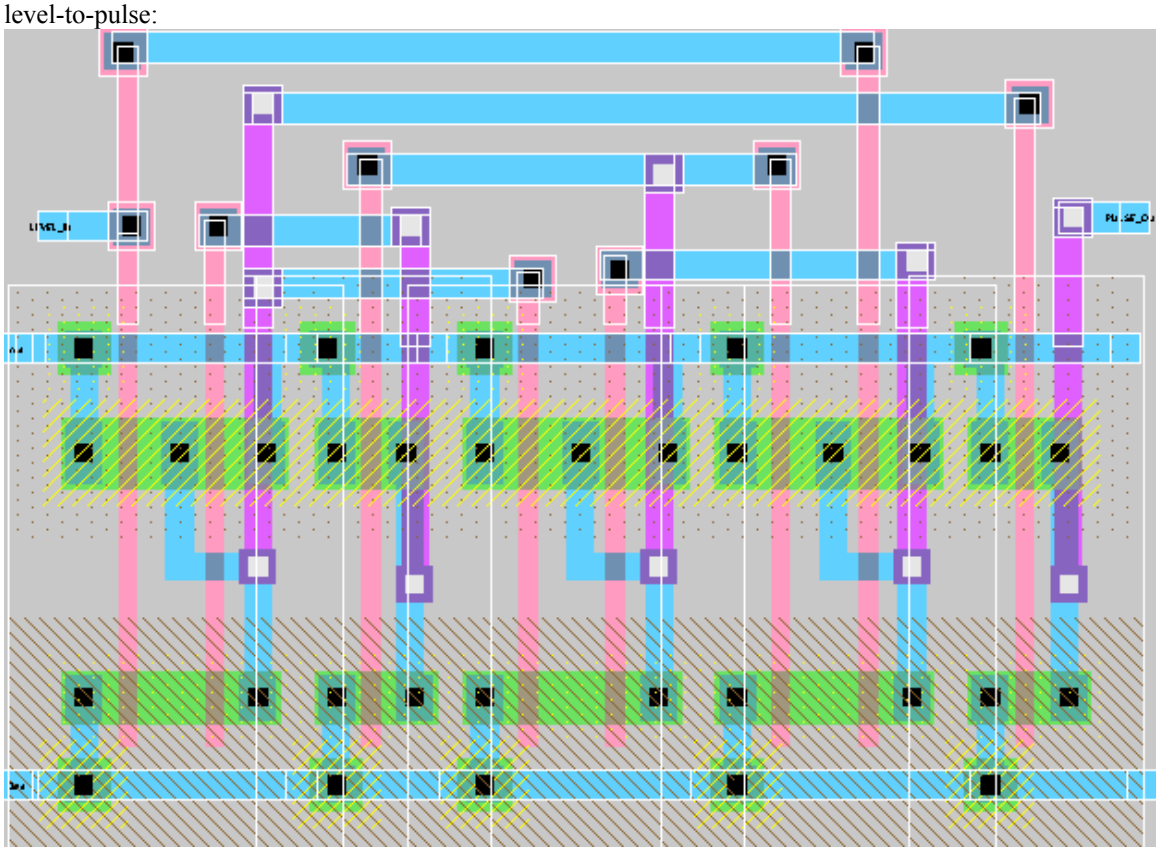
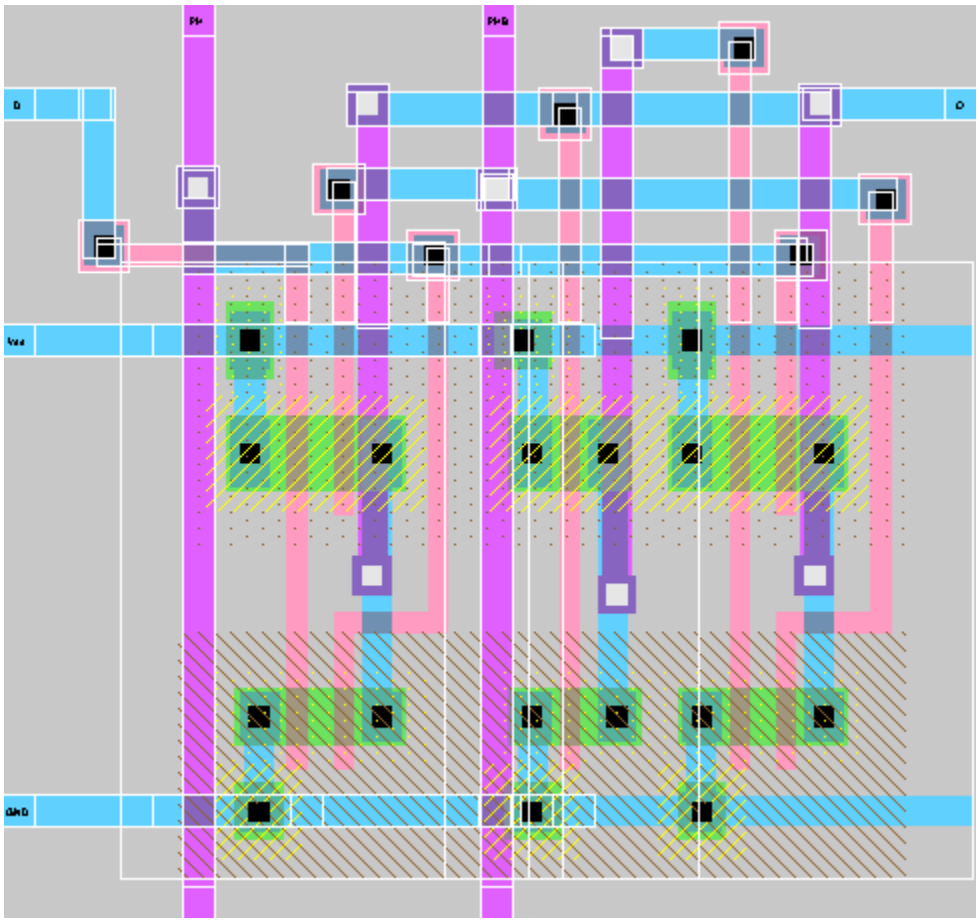


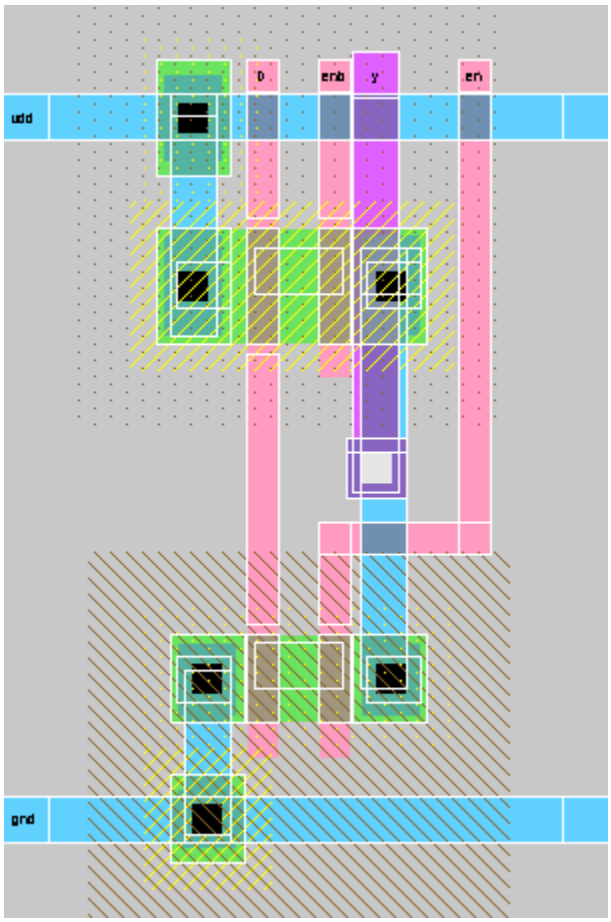
level-to-pulse:



latch:



tri:



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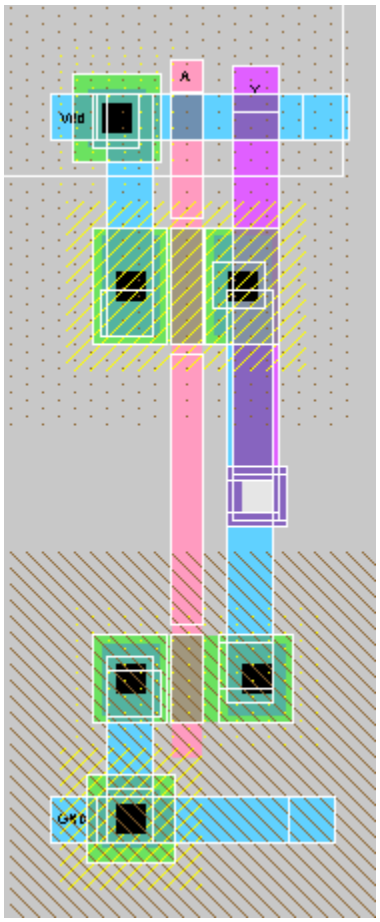

nand2: