A Freshman Advising Seminar on Digital Electronics and Chip Design

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Abstract

This paper describes a novel freshman advising seminar on digital electronics and chip design that has been taught at Harvey Mudd College for three semesters. The seminar seeks to combine the freshman advising process with a hands-on opportunity for freshmen to see what engineers "really do." In this seminar, the advisor, six to eight freshman advisees, and a student associate advisor / lab assistant meet one evening a week. In the first five weeks, students learn to solder together a utility board and breadboard a series of combinational and sequential digital electronics projects. Once they are comfortable with the design of digital circuits, they learn about building logic gates from Complementary Metal Oxide Semiconductor (CMOS) CMOS transistors and laying out CMOS transistors. They use the Electric CAD tool to design schematics, layout their circuits, simulate, and verify the chip as a team before sending it to the MOSIS service for fabrication. The chips have been used as components in industry sponsored research projects carried out by senior engineering students. Very Large Scale Integration (VLSI) design historically has been offered at the graduate or senior level, but has been simplified to the point that freshmen can develop working chips in the time available. This paper presents the structure of the seminar and assesses its benefits, including closer contact between advisor and advisees and the tremendous enthusiasm it generates among the freshmen. Based on success of the pilot project, a number of other freshman seminars have been developed and taught at Harvey Mudd College.

Introduction

Despite the best of intentions on the part of both faculty and students, freshman advising is often a bureaucratic process rather than a source of meaningful mentoring. Faculty and students are always busy and in the press of teaching and research and assignments, it is difficult to make time to meet beyond the obligatory signing of registration forms. Freshman advising seminars are a mechanism to regularly engage faculty and freshmen in an area of mutual interest; this regular meeting gives advisors a chance to get to know their advisees and offer support at a formative time in the student's career. This paper describes an experiment offering a freshman advising seminar on digital electronics and chip design at Harvey Mudd College during the fall semesters of 1999, 2000, and 2001.

The author has found that the topic is particularly well suited to a freshman advising seminar. Freshmen arrive curious about what major to pursue and wonder "what do engineers really do?"

Unfortunately, introductory classes in engineering often are a poor reflection of what engineers actually spend their time doing and very few offer technical depth. Chip design has traditionally been offered at the graduate or senior level. It is one of the marvels of modern technology that has revolutionized our world and appears completely unapproachable to the uninitiated. However, the subject has proven to be quite accessible to freshmen. Students with no prior experience and no special mathematical training learn to solder, design and breadboard digital circuits, understand how transistors work, draw schematics and layout logic gates, and work as a team to produce a complete integrated circuit for fabrication. At the end of the semester they take home a plot of the chip they designed and a good sense of what a practicing engineers might spend their time doing.

The freshman advising seminar grew out of a previous seminar offered by the author at MIT in 1992, 1993, and 1994 in collaboration with Dr. William Dally[1] and a further experiment by the author teaching chip design in 24 hours to high school students with the Stanford Educational Studies Program. This paper presents the structure of the advising seminar. It describes the projects that freshmen have completed and the CAD tool being used. Finally, it assesses the costs and benefits of the seminar.

Course Structure

The freshman advising seminar involves six to eight freshmen, chosen by lottery from approximately seventy applicants in the incoming class of one hundred eighty. The seminar generally also has a lab assistant who has taken the class before and who also serves as a peer advisor. The advisor and advisees first meet for a Saturday afternoon during freshmen orientation for an icebreaking activity. Such activities have included rock climbing and a beach trip.

The seminar meets one evening a week from 6:30 to 10:30 for thirteen weeks. It consists of one hour of lecture followed by up to three hours of laboratory time building circuits or designing chips. Freshmen receive one unit of pass/fail credit for the seminar on top of the seventeen units they ordinarily must take. Attendance is mandatory. At the beginning of lecture advising topics such as study habits, sleep management, study abroad, and test taking are discussed as appropriate. During lab the advisor has opportunity to talk one-on-one with freshmen. At the same time, first semester freshmen typically take Calculus, Mechanics, Chemistry (with lab), Structured Programming, and a humanities survey course.

The first five weeks are devoted to developing a mastery of digital electronics and an understanding of the uses of integrated circuits. The remainder is dedicated to learning to design CMOS gates at the schematic and layout levels and to a team project designing a chip. A week-by-week listing of the topics presented in 2001 is presented below. The syllabus, lecture notes, and lab manuals are available on the course web page[2].

September 5: Soldering & utility board
Principles of operation of a utility board with a power supply, LEDs, switches, and a 555 oscillator. Soldering. Students assemble their own utility board in the lab.

September 12: Logic gates
Boolean functions (NOT, AND, OR, XOR) and logic gates. Breadboarding. Students design and build a circuit to determine the direction of invasion of the Caltech Barbarians based on digital inputs from watchmen.

September 19: Boolean algebra
Boolean algebra and sum of products form. Students design and build a larger combinational logic function of multiple inputs and outputs.

September 26: Sequential circuits
Memory. RS latches, transparent latches, and D flip-flops. Students breadboard a D flip-flop from logic gates, then experiment with a 7474 flip-flop.

October 3: Finite state machines
Design process for a traffic light controller. Shift registers. Students breadboard a pocket hypnotizer.

October 10: CMOS circuits
Switch-level model of CMOS transistors. Conduction complement method of designing CMOS logic gates. Schematic entry and hierarchical design with the Electric CAD tool of inv, nand, nor, and, or, tristate, latch.

October 17: CMOS layout
Cross-section and principle of operation of a CMOS transistor. Layout design rules. Layout entry with Electric of inv, nand, and, nor, or, tristate, latch.

October 24: Fall Break. No seminar.

October 31: Structured layout
Datapath and control layout styles. Complete remaining layout of leaf cells.

November 7, 14, 21, December 5, 12: Project
Team implementation of a chip (see below). Usually a subset of the students work in the lab with the advisor on a Saturday in December to tapeout the chip.

In 2001, the lab assistant, Aaron Stratton, gave three supervised lectures. This was a learning experience for him as well as the freshmen. Most undergraduates at Harvey Mudd do not have the opportunity to teach.

Projects

The final third of each semester is dedicated to the class project. The project each year has been drawn from the Harvey Mudd Clinic program. Clinic teams generally consist of four juniors and seniors working on a year-long project sponsored by industry. Most clinic teams are not familiar with chip design and delegate work to the freshmen, which is exciting for the freshmen and gives the seniors experience managing technical development in an unfamiliar area. The author's criteria for choosing a project is that the chip should be an optional but useful addition to the clinic. As the chip may not work, it should not be essential to the success of the clinic project. Moreover, the chip is generally not available from manufacturing until March, so it should not be in the critical path. However, it should offer a meaningful benefit to the clinic team and client if it functions. The projects have been very motivating to the freshmen.

The three chips designed so far are a pin electronics adapter for a chip tester, an asynchronous first in first out (FIFO) buffer, and a Bit Error Rate Tester (BERT). The first two were designed for Sun Microsystems clinic teams and the third was for an Aerospace Corporation clinic team. Each of the chips has been fabricated through the MOSIS service[3] and plots are shown in Fig. 1.

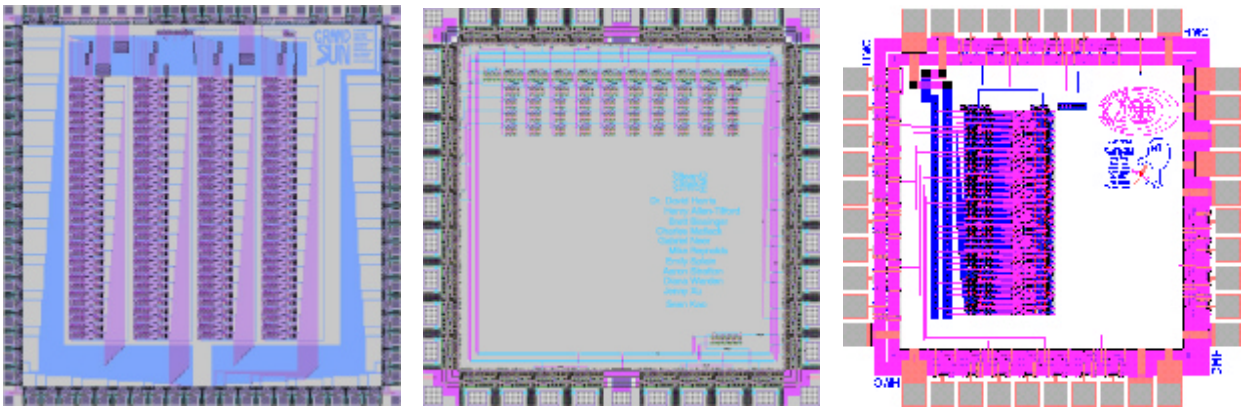

Figure 1: (a) Pin Electronics (b) Asynchronous FIFO (c) Bit Error Rate Tester

The first Sun Microsystems clinic team built a functional chip tester. A previous clinic team had tried constructing a tester controlling 256 pins of a device under test at variable voltage levels using off-the-shelf comparators and CMOS switches as level converters; this solution consumed a vast amount of board space. The current clinic team chose to use a custom chip designed by the freshmen and built pin electronics adapters using 5 and 3.3-v Xilinx FPGAs as a backup solution in the event that the custom chip did not function correctly. The freshmen chip functioned perfectly and is in use by Sun Microsystems Laboratories and Harvey Mudd College. The author and one of the freshmen from the seminar have proceeded to start a small company to build chip testers for other universities[4].

The second Sun Microsystems clinic team built an asynchronous FIFO as part of a demonstration board showing how to use short ripple FIFOs to interface synchronous systems running at different phases or frequencies. This was the first chip to use Electric and encountered many bugs in the software and simulator. The chip came back only partially functional and the clinic team used a Xilinx FPGA to implement the FIFO.

The Aerospace Corporation clinic team designed a 622 Mb/s BERT. The clinic team first developed a low-speed proof of concept. The method of building a full-speed product was initially unclear and the clinic team commissioned a chip from the freshmen to operate at intermediate speed as a further proof of concept. In the meantime, the clinic team has explored using a Virtex II FPGA. The chip was simulated and verified with Electric and was tested to be fully operational using the chip tester. It has been delivered to the clinic team.

The projects have involved a combination of effort from the freshmen, the lab assistant, clinic teams, and the advisor. The clinic teams act as a client, providing specifications and answering technical questions. This is a good learning experience for the clinic team members. The author as advisor has planned the overall chip architecture and divided it into blocks for the freshmen. The freshmen usually work in pairs on different components. In each project, a few have emerged as natural leaders who have taken responsibility for merging the components into larger units and one has stood out as exceptionally strong and has completed the overall chip assembly and verification. The freshmen also prepare written documentation for their chip.

CAD

VLSI CAD is a chronic headache, especially for smaller colleges. Cadence has aggressive university discounts and is a powerful industry standard, but requires nearly a full-time staff position to install and maintain. The author has little personal experience with the Mentor tools, but understands that there are similar challenges. The Tanner tools are easy to use but are less powerful than Cadence and cost more for academia. magic and sue are freely available under Unix and are thus widely used in academia; however their user interfaces leave much to be desired. The first class project successfully used magic and sue. As Harvey Mudd has explored moving toward Windows for CAD, the projects have switched to Electric, an open-source VLSI CAD system[5] developed by Dr. Steve Rubin available on Windows, Unix, and Macintosh. At first Electric had many limitations, but Dr. Rubin has been extremely proactive about improving the tool and has offered next day turnaround on showstopper bug reports. Now the tool is quite powerful and easy to learn; several chips have been successfully fabricated.

Assessment

This section seeks to assess the benefits and costs of the freshman advising seminar.

The seminar clearly strikes an untapped interest among freshmen, with more than a third of the incoming class applying for a handful of openings. In three years, only one student missed a seminar meeting, on account of illness. In the first year, the seminar was not evaluated with official course evaluation forms, but an unofficial survey of participants gave the class a 5/5 overall rating. In the second year the seminar received a 6.8/7 and in the third a 6.2/7. The college mean is 5.8/7 and 6.8/7 is the best teaching evaluation that the author has received. The drop in the third year probably is due to a greater amount of teaching by the lab assistant and a lower overall amount of time the instructor had available to spend on the class on account of a heavy teaching load.

Four of the first fourteen participants in the seminar have gone on to do VLSI research. At an undergraduate institution, it is very useful to have trained research students starting in the freshmen year so that they can grow into doing useful work before graduating. One has cofounded a company, One Hot Logic LLC, with the author.

The seminar was run as an experiment in the first year. Given its success, Harvey Mudd offered two other freshmen seminars each of the next two years on topics such as the Los Angeles River and Do-it-Yourself Nanotechnology.

The author got to know his freshman advisees much better than his major advisees, indicating that the seminar met its objectives in developing a relationship between faculty and students. It is not clear if the relationship led to tangible improvements in the success of the students at Harvey Mudd. Roughly half of the participants have gone on to become engineering majors; however, it may be just as valuable for freshmen to learn that they do not want to become engineers as to learn that they do. So far, one advisee has failed out and another has transferred; the remainder are on track to graduate in four years.

The direct financial cost of the seminar was $50/student for lab kits that each student keeps at the end of the semester, $450 in pay for the lab assistant, and $250 for meals, snacks, and the

orientation activity. The seminar met in the senior digital electronics lab and the engineering computational facility. A grant from the MOSIS Educational Program funded chip fabrication.

The greatest cost of the freshmen seminar program is faculty time. Now that the seminar is established, it takes about five hours of the author's time each week along with about ten hours before the semester starts to organize handouts and lab kits and another fifteen hours at the end of the semester to guide students through tapeout. More time was required during initial development. Although the Dean of Faculty has issued modest stipends to faculty advisors for organizing seminars, it is difficult to juggle the extra teaching load with an already busy schedule of teaching and research.

Clearly, there is great student demand for freshman advising seminars and the seminar has been extraordinarily successful in terms of teaching evaluations, research students, and even a startup company. In its present form, freshman advising seminars are essentially a labor of love. A strong and sustained institutional commitment is necessary to expand the seminars to reach their full potential. This is consistent with the author's observations at MIT, in which freshmen advising seminars bloomed in the early 1990's under the strong support of Travis Merritt, Dean of Undergraduate Education, then faded after his retirement.

Acknowledgments

The author thanks Sheldon Wettack, Lisa Sullivan, and Clive Dym at Harvey Mudd College for their moral and financial support of the freshman seminar experiment. Aaron Stratton has been an enthusiastic and dedicated lab assistant for two semesters. MOSIS arranged funding to support fabrication of two of the chips. The Sun Microsystems and Aerospace Corporation clinic teams and liaisons were instrumental to the success of the projects.

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Biographic Information

DAVID HARRIS has been an Assistant Professor of Engineering at Harvey Mudd College since 1999. He received his Ph.D. in Electrical Engineering from Stanford University and his M.Eng. and S.B. degrees from the Massachusetts Institute of Technology. He is the author of *Logical Effort*, *Skew-Tolerant Circuit Design*, six patents, and assorted papers on high speed digital VLSI design.