Design Flows and Collateral for the ASAP7 7nm FinFET Predictive Process Design Kit

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***Abstract*—Educators and researchers exploring integrated circuit design methods need models and design flows for advanced integrated circuit processes. As commercial processes have become highly proprietary, predictive technology models fill the gap. This work describes a design flow for ASAP7, the first 7 nm FinFET PDK, including schematic and layout entry, library characterization, synthesis, placement and routing, parasitic extraction, and HSPICE simulation.**

Keywords—design flow, predictive technology model, FinFETs

I. Introduction

Educators and researchers need credible and complete models and flows for advanced integrated circuit processes. Students should learn to design chips using the same tools and methods that they will employ in industry, and benefit from targeting contemporary processes to get a feel for the capabilities and challenges of these processes. For example, learning about contemporary memory design requires good simulation models. Researchers exploring functional blocks need to be able to characterize the performance, power, and area of these blocks in a modern process. Development and exploration of design methodologies requires realistic models to assess the effectiveness of the methods.

Ideally, academics could use industry-standard process design kits (PDKs) with the full set of collateral necessary for schematic entry, layout, design rule checking, parasitic extraction, transistor-level simulation, library generation, synthesis, and automatic placement and routing (APR) using tools from the leading electronic design automation companies. Unfortunately, the industry is highly proprietary and access to modern processes is difficult, especially when no fabrication is planned. Researchers have responded with a variety of predictive technology models (PTMs). This paper surveys the existing PTMs and PDKs, listing strengths and limitations of each. It then presents a complete design flow for the ASAP7 7 nm FinFET PTM. As conventional scaling slows, we expect that the 7 nm node will remain interesting for many years.

II. Survey of Process Design Kits

A process design kit requires predictive technology models for the transistors and design collateral including libraries and technology files required by CAD tools. Predictive technology models were popularized at Berkeley [1] and have evolved through many generations [2]. The models have attempted to track planar and multigate CMOS processes with varying success because predicting the future is an imperfect art [3].

At present, the major process design kits include FreePDK45 [4] and FreePDK15 [5], [6] from NCSU, 14 and 7 nm USC PDKs [7], [8], [9], [10], Synopsys 32 nm Generic Libraries [11], [12], and Cadence University Program 90 nm, 45 nm, and FinFET generic libraries [13]. Table I summarizes the types of data available in these PDKs. Synthesis and APR requires cell library Liberty (.lib) models consistent with HSPICE simulations of the extracted layouts, physical views (LEF/FRAM), and tool-dependent collateral including routing and interconnect parasitic extraction rules.

The NCSU FreePDK45 1.4 [14] is based on custom ASU Nano-CMOS PTMs tweaked to roughly match the Fujitsu 45 nm process [15] and has two cell libraries. The NanGate library [16] Liberty file delay and leakage models are inconsistent with the HSPICE models [3], so the library is not suitable for predictive research. The OSU library [17] has views for synthesis and Cadence Encounter APR. The Liberty delays are presently inconsistent with HSPICE but the libraries are being recharacterized. The NCSU FreePDK15 is based on the ASU 14 nm PTM-MG HP multigate transistor HSPICE models drawn at L = 20 nm (as compared to 18 nm nominal in the SPICE model file). The NanGate 15 nm Open Cell Library [18], [19] is presently incomplete, lacking views for APR. Both NanGate library release notes [16] prohibit "benchmarking of this library against any other library" and indicate the library is not optimized.

The Synopsys 32 nm generic library has serious mischaracterization problems at present [3]. The USC 7 nm library has a 10.5 nm fin pitch [9] corresponding to the ITRS definition of a 1 nm process [20], and hence has energy and FO4 delay much lower than industrial 7 nm expectations. The Cadence generic libraries use Spectre rather than HSPICE. The 45 nm generic library has fast and slow but no typical data. The FinFET library does not specify an intended process node and does not yet have APR views.

III. ASAP7 Process Design Kit

The ASAP7 7 nm FinFET PDK [22] was developed at Arizona State University in collaboration with ARM. The base kit contains Cadence Virtuoso technology files for schematic entry, layout, DRC, LVS, and parasitic extraction and HSPICE models for simulation. It supports four: SRAM, RVT, LVT, and SLVT classes with I_{OFF} leakages of less than 0.1, and about 1, 10, and 100 nA/µm, respectively. For RVT, LVT, and SLVT, nMOS ON currents are 1402, 1674, and 1881 µA/µm at 0.7 V, and FO4 inverter delays of 8.1, 6.8, and 6 ps, including extracted layout resistance and capacitance. The P/N ratio is 1.1. Subthreshold slope is about 62-64 mV/decade at room temperature, and DIBL is about 21-22 mV/V. Gate leakage is 0.33-1.48 nA/µm. The models are consistent with industry scaling trends and the International Technology Roadmap for Semiconductors forecast for high-performance logic devices, except that the inverter delay is greater and appears to be more realistic than the ITRS [3].

Table II summarizes the interconnect stack [23]. The PDK assumes a low-k dielectric of ε=2.9 and a thin (3.6 – 8 nm) hard mask of ε=42. The kit does not currently support antenna rules. Self-aligned via merging allows adjacent vias when they are aligned on the same grid. The ASAP7 design rules were developed using design/technology co-optimization (DTCO) of logic library and SRAM cells. The rules comprehend expected time dependent dielectric breakdown (TDDB) based on worst-case misalignments.

Table II. BEOL layers (metal aspect ratio is 2:1).

Metal / Via	Thickness / Pitch (nm)	Resistance
M1-M3	36	1.2 Ω /square
V1-V3	39.6 / 36(merged)	17.2 Ω
M4-M5	48	0.77 Ω /square
V4-V5	52.8 / 48(merged)	11.8 Ω
M6-M7	64	0.50 Ω /square
V6-V7	70.4 / 64(merged)	8.2 Ω
V8-M9	80	0.36 Ω /square
V8	88 / 80 (merged)	6.3 Ω

IV. Cell Libraries and APR Collateral

The PDK is also supported with a cell library for APR projects. The cell library includes LEF, LIB, FRAM, and .db views, as well as .cdl for LVS. All Cadence OA views, e.g., layout and schematic, are not supplied so that courses may include cell design as assignments. There are exemplary INVX1 and DFFX1 standard cells supplied with the kit. The presently available libraries were developed by VLSI course students at ASU and optimized and characterized by a graduate student. The cells use a horizontal alignment in line with the 54-nm CPP.

The basic libraries use the 7.5 track architecture outlined in [21] as shown in Fig. 1. The library can use 2-D M1, assuming EUV patterning. While the basic PDK assumes EUV M2 and M3, the library is compatible with self-aligned quadruple patterning (SAQP) M2 and M3. The library can support wide M2 power follow rails, consistent with SID SAQP M2 patterning, or narrow M2 power follow rails as expected by the EUV M2 assumption.

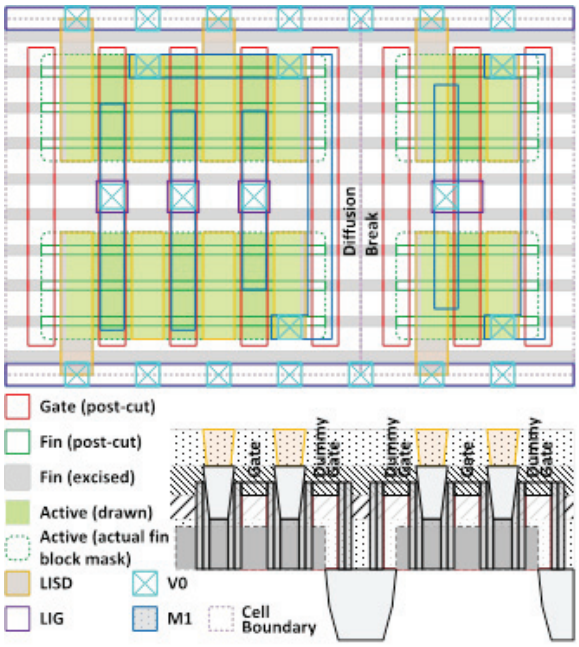

Fig. 1 7.5 M2 track ASAP7 standard cell layout and cross-section up to MOL. NAND3 (left) and inverter (right). Cross-section shows the double diffusion break required by fin cuts under gate (cut portion in grey). The cross section does not show LIG, V0, and M1.

M1 through M3 use a 36 nm pitch, based on recent literature that shows the ITRS roadmap assumption of 32 nm may not be supportable by 2-D EUV patterning in the near term [24][25][26]. Recent publications of commercial foundry 7 nm PDKs shows this assumption was correct [27]. The cell M1 layers allow routing to at least two M2 tracks for all inputs. Outputs are maximized to support all five possible 7.5 track M2 track connections in most cells.

Cells for decoupling capacitance are supplied. Various sizes are supported, with the expectation that insertion first uses the largest, most efficient and progresses towards the smallest. The two CPP pitch cells should be tap cells, with one CPP dummy cells used to complete the gate grid and well continuity.

Cadence Innovus has many sub-licenses required to support processes with sub-20 nm dimensions. These licenses are not readily available to University Program members. To work around this issue and to allow the widest possible utilization, the LEFs and QRC techfile provided with the library are 4x. The QRC techfile has been carefully calibrated to the Calibre PEX results, which are used as the standard. When bringing a design back into the OA environment, a 0.25 scale factor is used to bring an APR based design back to the real PDK scale. ICC appears to have no such check and can run unscaled FRAMs. Of course cell timing is unaffected by this scaled approach. Additionally, working with ARM, we have correlated an unscaled QRC techfile to Caliber PEX.

Fig. 2 illustrates a small APR design using the ASAP7 PDK and initial 7.5 track libraries. This is a level 2 cache error detection and correction block providing Hamming ECC for a

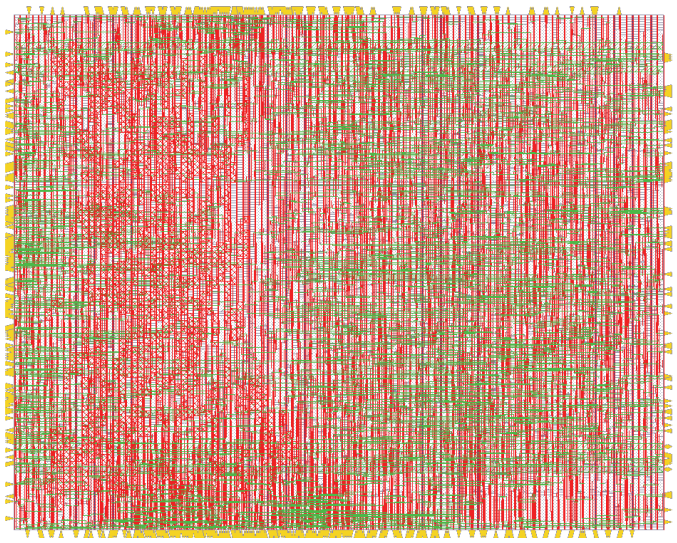

Fig. 2. APR example captured from Innovus. This design is routed only on M2 and M3. An optimized, iterative flow provides industry level cell density above 80%. This block is approximately 22 by 28 µm.

128-bit memory word. It has been used in the introductory VLSI course, providing a Verilog coding target using simple pipelining in the ECC generation and syndrome calculation as well as the correction directions. As mentioned, Innovus works with 4x dimensions, and the design is scaled when streamed into Cadence Virtuoso. The Calibre flows can generate the SADP metallization mandrel and block mask, as well as the intermediate spacer polygons. These have been used to ensure that the design rules, which do not require the designer to comprehend multi-patterning, are correct [23]. With minor modifications, the PDK can be used to study the impact of more modern fabrication/design interactions such as a pure/lines cuts flow [28].

V. ASAP7 Memories

Compact SRAM cells are key components in a modern fabrication process. While specific (tighter dimension) design rules allow these highly repeated cells to be smaller, they pose among the most complex DTCO challenges. Moreover, conventional planar processes provide more degrees of freedom in obtaining the necessary β ratios for write-ability and read stability, than the discretized fins in a FinFET process. In the ASAP7 PDK, four SRAM cells have been developed: 111, 112 122, and 123, describing the PMOS pullup, access, and pull down fin count, respectively [29]. The smallest 111 cells are within 10% of the recently published foundry 7 nm generation cell size [30]. The 112 and 122 cells require 10 fin pitches, and are thus the same size as the 7.5 track standard cells, but have different alignment. The alignment is dealt with by the requisite dummy cells at the array edges.

Variation modeling is not directly supported by the ASAP7 PDK, but is required for good SRAM design that comprehends yield over PVT variation. It is straightforward to

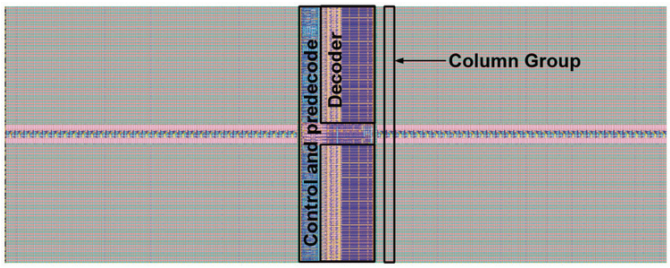

Fig. 3. 6-T cell 1k x 64-bit SRAM array using the ASAP7 PDK. Array efficiency is over 84%. The array is 74.8 by 30.3 µm

add the necessary mismatch, based on the expected AVT, using HSPICE. This is the approach used in the ASAP7 memory designs to determine read and write margins, as well as the differential sense amplifier input referred offsets. We use AVT = 1.2 mV-µm, based on the 1.07 and 1.23 for NMOS and PMOS, respectively, published by Intel for the 14 nm node [31]. This value is in line with expectations for a metal gate finFET process [32]. The same approaches should serve pure analog designs.

The SRAMs have densities, as measured by array efficiency (cell area/total area), in line with commercial designs. The largest array is illustrated in Fig. 3. Consequently, these will provide accurate power, performance, and area figures for studies ranging from the circuit to the architectural level. The standard cell library is used in the control logic (which is APR'd) but custom decoder cells are used for the requisite high density at the SRAM pitch. Write assist is essential given the discretized sizing—it is comprehended in the macros, but is not evident to the user in a design environment using them.

The SRAM cells provide the base for multi-port register file cells. These cells require a wider pitch and thus the array I/O uses custom designed cells, which are easily generated by stretching standard cells. Various register files have been designed in courses. The most commonly used two read and one write port 32x32 RF will be made available as a LEF and lib. These provide a considerable density advantage, but most modern designs synthesize such small arrays. The latter often have an access time advantage.

Synopsys has recently made small signal SRAM support an option rather than built-in feature of Nanotime. This is in contrast to past versions that did have rudimentary SRAM analysis. Unfortunately, the SRAM analysis option is not part of the standard academic licensing. Cadence has kindly provided ASU Liberate_MX licensing, not part of the standard academic releases, which are used to provide liberty files for the SRAMs. Nanotime is still used for register files, but we may change to Liberate_MX in future.

VI. Conclusions

Academics need PDKs supporting custom design, synthesis, and APR in advanced technologies. This paper has presented a process design kit for the ASAP7 7 nm FinFET

predictive technology models. It is the first predictive PDK with full collateral for transistor-level design, HSPICE simulation, synthesis, and APR in which the libraries match the HSPICE models and are consistent with industry trends.

In general, academic course and research work will become more difficult as PDK complexity increases. Until recently, generous vendor academic licensing has made most tools available for academic use, but the trend is worrisome below 20 nm. This will put increasing pressure on instructors as well as the CAD infrastructure.

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Table I. Comparison of Predictive PDKs

		Custom Design						APR		
PDK	**Library**	**Virtuoso Schematics**	**Virtuoso Layout**	**DRC**	**Parasitic Extraction**	**LVS**	**HSPICE**	**Liberty**	**Physical**	**Collateral**
FreePDK45	NanGate	Yes	Yes	Yes	Yes	Yes	Yes	Inconsistent	Yes	None
	OSU_SOC							Inconsistent	Yes	Encounter
FreePDK15	NanGate	Yes	Yes	Yes	No	No	Yes	Yes	Yes	None
USC 7nm		No	No	No	No	No	Too fast	Yes	No	None
Synopsys 32 nm		No	No	No	No	No	Inconsistent	Inconsistent	Yes	ICC
Cadence 45nm		Yes	Yes	Yes	Yes	Yes	Spectre ?	Yes	Yes	Encounter
Cadence FinFET		Yes	Yes	Yes	Yes	Yes	Spectre	No	No	No
ASAP7		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Innovus