Digital Design and Computer Architecture: RISC-V Edition

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Errata List as of 7 January 2022

Chapter	Page	Errata
4	199	HDL Example 4.24: "endmodule" should be left-aligned with "module sevenseg…" on the first line.
6	377	Exercise 6.16(a): "Use `t0` for `i`." → "Use `s0` for `i`."
6	381	Exercise 6.23: "`ori s3, s1, 0xABC`" → "`ori s3, s1, -1348`"
6	384	Exercise 6.33: "`for`… " and the line below it should each be indented by two spaces.
7	456	Figure 7.63: Signal RegSrc should be deleted from figure.
7	494	Exercise 7.39: "Assume the delay of an equality comparator is 23 ps."