Digital Design and Computer Architecture, 2nd Edition
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Errata List as of 15 April 2021

Chapter	Page	Errata
Front material		In Praise of Digital Design and Computer Architecture section: "…FGPAs…" → "…FPGAs…"
Preface	xxiii	End of 2nd paragraph: "…selection of designs on the DE2 Board using Cyclone II Web Edition." → "…selection of designs on the DE2 Board using Quartus II Web Edition."
Preface	xxiii	"Please send your bug reports to *ddcabugs@onehotlogic.com* ." → "Please send your bug reports to *ddcabugs@gmail.com* ."
1	23	Figure 1.22: Although logically equivalent, the columns should be labeled "*A B C D*" (instead of "*A C B D*")
2	65	1st paragraph: "…Figure 2.9: $Y = A'B' + AB'$. By Theorem T10, the equation simplifies to $Y = B'$. " → "…Figure 2.9: $Y = A'B + AB$. By Theorem T10, the equation simplifies to $Y = B$. "
2	76	3rd full paragraph: "...while 01 : 10 would change A from 1 to 0 and B from 0 to 1." → "...while 01 : 10 would change A from 0 to 1 and B from 1 to 0."
2	93	Figure 2.74: 85 ns → 85 ps, 100 ns → 100 ps, $t pd$_TRLSY → $t pd$_TRI_sy
4	204	HDL Example 4.26: SystemVerilog: the "<=" should be replaced with "=".
4	205	HDL Example 4.27: SystemVerilog: the "<=" should be replaced with "=".
4	210	HDL Example 4.30: SystemVerilog: the "<=" under case(state) should be replaced with "=".
4	210	HDL Example 4.30: "statetype [1:0] state, nextstate;" → "statetype state, nextstate;"
4		To use VHDL 2008 in ModelSim, you may need to set VHDL93 = 2008 in the modelsim.ini configuration file.
5	241	Last sentence: "…using the carry in to the block C_j." → "…using the carry in to the block C_{j-1}."
5	241	Equation 5.5 should be: $C_i = G_{i:j} + P_{i:j}C_{j-1}$
5	278	"However, in this case $Y = S_0$" → "However, in this case $Y = S_0'$."
5	278	Figure 5.61: in LE1, the input of the Y mux should connect to the output of the LUT.
6	319	Code Example 6.20: High-level code should include "int i;" as the second line.
6	320	Example 6.6: High-level code should include "int i;" as the second line.
6	327	5th paragraph: "In particular, it should not modify any registers besides the one containing the return value $v0." → "In particular, it should not modify any registers besides the one containing the return value $v0 (and $v1 for 64 bit results)."
6	331	Code Example 6.27: "iw" → "lw"
6	338	Code Example 6.30: "iw" → "lw"
6	340	Last line: "For example, the first store instruction…" → "For example, the second store instruction…"
6	346	Figure 6.35: "cop" → "fop"
6	346	3rd paragraph: "They require both a funct field and a cop (coprocessor) field to indicate…" → "They require both a funct field and a fop (floating point operation) field to indicate…"
6	346	3rd paragraph: "cop = 16 (10000_2) for single-precision…" → "fop = 16 (10000_2) for single-precision…
6	365	Exercise 6.30(d): "…can the jump instruction (j) jump backward?" → "…can the jump instruction (j) jump forward?"
7	395	First paragraph, last sentence: "The *RegDst* instruction selects..." → "The *RegDst* multiplexer selects…"
7	397	First line: "The main controller produces multiplexer select and register enable signals…" → "The main controller produces multiplexer select and enable signals…"
7	409	End of 3rd paragraph: "…the single-cycle processor has an instruction latency of 250 + 150 + 200 + 250 + 100 = 950 ps…" → "…the single-cycle processor has an instruction latency of 250 + 150 + 200 + 250 + 100 = 950 ps (where the final 100 ps is the time to write to the register file) …
7	428	Equation 7.5, Decode stage: "2(...T_mux +…)" → "2(...t_mux…)"
7	429	Figure 7.59, the Main Decoder should have a Jump signal that connects to the Datapath
7	449	First paragraph, last sentence: "for an IPC of 1.17." → "for an IPC of 1.2."
7	454	Figure 7.72: In the Bit position row, '32' should be '31'
7	470	Exercise 7.23: `addi $s0, $0, done` → `addi #s0, $0, 5`
7	471	Exercises 7.30 and 7.31: "iw" → "lw"
8	480	Last full paragraph: "If 50% of a program's instructions are loads and stores,…" → "If 50% of a program's performance is due to loads and stores…"
8	543	The top of the page should read: "The horizontal timing involves a front porch of 16 clocks, hsync pulse of 96 clocks, and back porch of 48 clocks. The vertical timing involves a front porch of 11 scan lines, vsync pulse of 2 lines, and back porch of 32 lines."
8	547	Last paragraph: "wireless phones" → "wireless routers"