Errata

CMOS VLSI Design
3rd Edition

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Send your corrections to bugs@cmosvlsi.com

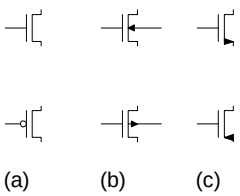
Errata in 2nd Printing

Page viii, Section 4.3: "SIzing" -> "Sizing" (N. Ho 8/16/06)

Page 39, Table 1.7: "PC <- PC+imm" -> "PC <- PC + 4 + imm*4" (E. Brunvand 11/7/05)

Page 41, Fig 1.52, beq: 0000000000000101 10600005 -> 0000000000000100 10600004 (E. Brunvand, 11/7/05)

Page 41, Fig 1.52, last line: encoding for sb should be 101000, not 110000 (E. Brunvand 11/7/05)

Page 67, Fig 2.1 should be: 

(D. Rancour, 8/5/05)

Page 67, Footnote: 2.4.5 -> 2.4.6 (J. Jung, 7/16/05)

Page 82, example: C_{jbs} -> C_{jbd}, C_{jbssw} -> C_{jbdsw}, C_{jbsswg} -> C_{jbdswg} (E. Martins 3/27/07)

Page 99, line 7: 0.34 -> 0.13 (D. Rancour 8/9/05)

Page 100, Section 2.5.4: Delete Optional (D. Rancour, 8/9/05)

Page 104, Fig 2.34: pMOS should swap "d" and "s" labels (K. Neilsen 6/1/05)

Page 144, bottom paragraph: "pitch is P = W+S" -> "pitch, in turns per meter, is P = 1/2(W+S)"

Page 190, Example line 2: 1:32 -> 5:32 (K.T. Lau, 1/26/06)

Page 199, line 1-2: "sheet resistance" -> "resistivity" (G. Venturini, 1/29/06)

Page 223, next to last paragraph, line 4: "thorough" -> "through" (G. Jedhe 9/11/05)

Page 282, Figure 5.9: line patterns for e and f should be reversed (M. Demming 1/12/09)

Page 308, Table 5.7: “gu” –> “gd” in Falling Logical Effort column (M. Awedh 12/10/07)

Page 326, Fig 6.11 (inverter efforts): $g_u = 1.14$, $g_d = 0.80$, $g_{avg} = 0.97$ (J. Liu 10/28/06)

Page 362, paragraph 4, line 9: ‘correct output Y” -> “correct output $\bar{Y}$ ”, (D. Rancour 9/1/05)

Page 407, 3rd paragraph, line 2, Figure 7.17(j) -> Figure 7.17(k) (DH 5/22/05)

Page 476, exercise 7.8. Add “Express the times relative to the rising edge of ϕ_1.” (R. Lethin 10/13/05)

Page 508, Fig 8.26: one of the transistors is missing a third contact and the blue stipple Lines should be behind contacts (Y. Dong 2/25/06)

Page 514: paragraph 3: generate_rom -> generate_rom_layout (J. Mao 9/24/06)

Page 515, pseudocode: y = y + yorigin -> y = y + rom_bit_height (J. Mao 9/24/06)

Page 617, Fig 9.31: Avoid line break on UpdateDR label (DH 10/15/06)

Page 644: “MINORTY” -> “MINORITY” (D. Gong 10/18/07)

Page 646, line below (10.5): “upper (most significant)” -> “upper (most significant) generates” (S. Khasawneh 11/22/07)

Page 699, 9th line: “y_i” -> “y_j”, “y_{i-1}” -> “y_{j-1}”

Page 701, paragraph 3, line 4: “$e_i = M_i$ xor y_{15}” -> “$e_i = PP_{iN}$ (e.g. the most significant bit of the *i*th partial product)” (G. Prasad 11/05)

Page 718, Fig 11.8 timing diagram: “bit_v1f” -> “bit_b_v1f” (S. Khasawneh 11/19/07)

Page 719, Figure 11.10(a): reverse inverter and data_s1 connection in write driver (S. Khasawneh 11/22/07)

Page 784: 150 Ω -> 109 Ω (S. Lin 4/12/07)

Page 795: Figure 12.36 caption: Itaniuim -> Itanium (S. Lin 4/16/07)

Page 803: 12.5.6.3 line 2: Itaniuim -> Itanium (S. Lin 4/16/07)

Page 880, 2nd line: “@(s)” -> “@(s, d0, d1)” (Viveka 7/23/08)

Page 829, Fig 12.75: “leat” -> “leads” (T. Carmel-Veilleux 9/6/09)

Page 851, line 2: add space after “input” to align with next row [(DH 9/24/05)

Page 853, Table A1: delete comma after >> (DH 9/24/05)

Page 856, module mul: add space after “input” to align [(DH 9/25/05)

Page 857, change two lines to delete illegal reversed range b[1:3] (DH 9/29/05)

```
assign y = {a[2:1], {3{b[0]}}, a[0], 3'b101};
y = a[2] a[1] b[0] b[0] b[0] a[0] 1 0 1
```

Page 900, Table B1: delete shading from “not” row (DH 9/24/05)
Delete row with =, = =, !=

Page 909: last paragraph, 1st line: @ stimulus -> sensitivity (DH 9/25/05)
@ -> sensitivity in two more places in same paragraph

Page 915: Output logic should be (H. Zhu 8/7/05)

```
-- output logic
x <= '1' when ((state = S1 or state = S2) and a = '0') or
              ((state = S3 or state = S4) and a = '1')
         else '0';
y <= '1' when ( state = S2 and a ='0') or (state = S4 and a = '1')
         else '0';
```

Page 942, [Naffziger 02]: implementnation -> implementation (DH 5/3/06)

Errata in 1st Printing (corrected in 2nd printing, Spring 2005)

Many figures have incorrect metal2 stipple (either blank or hashed) caused by a bug in the printer software. These include:

1.39, 1.44, 1.61, 1.62, 1.67, 3.8, 3.11, 3.18, 3.20, 4.31, 4.33, 8.27, 8.28, 8.29, 8.52, 8.53, 10.5,
10.65, 11.3, 11.5, 11.6, 11.38, 11.39, 11.50, 11.58, 12.6, 12.7, 12.23,
(DH 5/12/04)

Some figures have lines that don’t meet up properly caused by poor registration between blue and black by the printer. (DH 5/13/04)

3.21, 11.24, 11.25, 11.27, 11.28,

Back side of title page: (“David F.”) should be (“David M.”) (SH 5/16/04)

Fig 1.2 caption: (a) First transistor (Property of AT&T Archives. Reprinted with permission of AT&T.) and (b) first integrated circuit. (Courtesy of Texas Instruments.) Luiz Brunelli 1/8/05

Page 13, third line from bottom, last word: inversed <- inverted (Rosenberger 9/8/04)

Page 14, line 8: “multiplexer.” -> “inverting multiplexer.” A -> $\overline{A}$, D -> $\overline{D}$ (M. Kharashgeh 10/4/04)

Page 14, last paragraph: “2.3.2” -> 2.5.5 (V. Yadav 10/31/04)

Page 19, last line: add “In practice, both inverting and noninverting multiplexers are simply called multiplexers or muxes.” (C. Chu 1/13/05)

Page 24, fig. 1.34 Field oxide missing between NMOS and PMOS (J. Frenzel 2/6/05)

Page 26, Fig 1.35(a): Polysilicon should be black hash rather than solid blue (A. Rainer 1/27/05)

Page 35, Fig 1.47: A sixth vertical arrow is needed to indicate six tracks. J. Frenzel 1/20/05.

Page 63, Exercise 1.2: V_s. should be vs. (DH 5/29/04)

Page 64, Exercise 1.5(c): $\overline{AB}$ should read $\overline{A}\overline{B}$ (DH 5/29/04)

Page 64, Exercise 1.14(d): should read “layout your gate with a CAD tool using unit-sized transistors” (D. Harris 1/30/05)

Page 65, Exercise 1.15(d): should read “layout your gate with a CAD tool using unit-sized transistors” (D. Harris 1/30/05)

Page 65, Figure 1.73: missing black contact on Y output. J. Frenzel 1/20/05.

Page 96, line 6: -8 should be –oo (infinity symbol) (K. Popiolek, 10/13/04)

Page 102, 4th paragraph: 1.5.6 -> 1.4.6 (A. Parayandeh 11/18/04)

Page 109, Exercise 2.11: use n = 1.0 (DH 5/30/04)

Page 109, Exercise 2.13: give V_{DD} = 1.8 V (DH)

Page 110, Exercise 2.14: Before lasts sentence, add “Assume $\beta_n = \beta_p = \beta$ and $V_{tn} = |V_{tp}| = V_t$.” (DH)

Page 115, end of 3rd paragraph. Should read "... made thinner. This in turn makes them ..." (instead of "This is turn") (J. Frenzel 2/6/05)

Page 124, paragraph 3: "Pirhana solution" -> "Piranha solution" (S. Kabadayi 10/4/04)

Page 131 - last paragraph: "Section 1.6.5" should be "Section 1.5.5." (J. Frenzel 2/6/05)

Page 137, line 2: "leakge" -> "leakage" (S. Kabadayi 10/4/04)

Page 145, paragraph 4: “ground lane” -> “ground plane” (Sproull 6/1/04)

Page 161, Eq 4.1: “j=i” -> “j=1” (Sproull 6/1/04)

Page 191, Example, line 1: “page 99” -> “page 189” (J. Frenzel 2/28/05)

Page 213, last line of example: “writ-“” -> “writing.” (Jun Shi 11/11/04)

Page 243, Fig 4.66 Missing oxide on Y between metal1 and substrate. (J. Frenzel 2/6/05)

Page 266, Exercise 4.3: “AND-OR-INVERT” -> “unloaded AND-OR-INVERT” (DH)

Page 269, Exercise 4.25: 300 pF -> 300 fF (DH 10/27/04)

Page 277, table 5.2: mili -> milli (S. Carriere, 11/25/04)

Page 282, figure 4.9: e and f line patterns should be interchanged (S. Carriere, 11/24/04)

Page 284, paragraph 2: “and four inverters.” -> “and five inverters.” (S. Carriere, 11/24/04)

Page 284, paragraph 2: “inverter is subcircuit (X)” -> “inverter is a subcircuit (X)” (S. Carriere, 11/24/04)

Page 341, paragraph 3: "p = 2.76" => "ρ = 2.76" (Sproull 6/1/04)

Page 343, 2nd to last paragraph: “dynamic p-logic NOR” -> “dynamic p-logic NAND” (M. Abdeen, 2/18/05)

Page 346: DCVSPG and PPL schematics should reverse Y and Ybar (DH)

Page 372, line 3: “actually subthreshold” -> “actually have subthreshold” (Sproull 6/1/04)

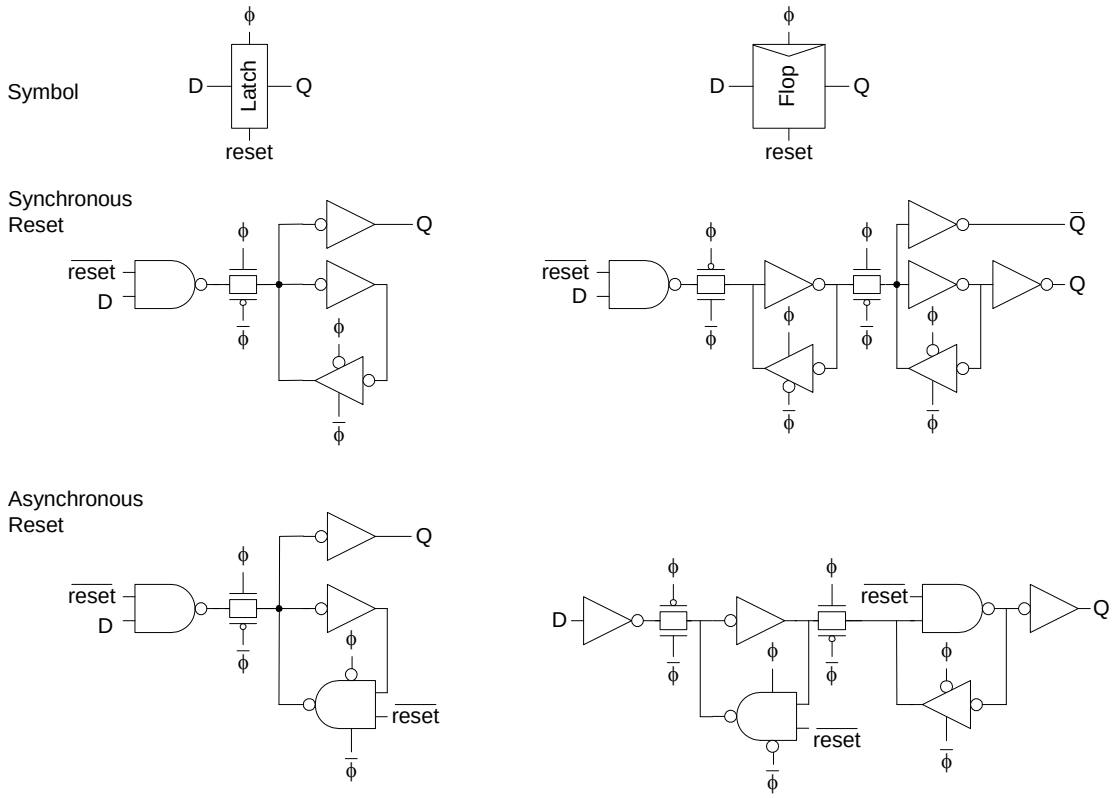
Page 380, Exercise 6.24: 2nd sentence: pull-up should be four times as strong as pull-down. Last sentence: compare to static CMOS 2-input NAND. (DH 6/27/04)

Page 381, Exercise 6.36: each input can drive 10 unit transistors (DH)

Page 400, fig 7.15: t_pdq should be t_pd (D. Ha 2/7/05)

Page 407, Fig 7.21: Exchange bubbles on phi2/phi2b (two places) (M. Senlik, 12/29/04)

Page 409, Fig 7.24: Asynchronously Resettable flip-flop should be redrawn as (A. Rainier 3/9/05):



Page 413, Fig 7.29: Delete funny box after text. (DH 4/04)

Page 423, Fig 7.39: 1.2, 1.4, and 1.6 labels on x axis are garbled and should be placed beneath tick marks. J. Frenzel 3/22/05.

Page 440, Figure 7. 58(a) the label for the fourth wave form: clkbddd -> clkddd (D. Ha 2/15/05)

Page 463, Fig 7.88(b): ack1 and ack2 should be swapped. J. Frenzel 4/4/05.

Page 473, Table 7.4: equation is missing from pulsed latch time borrowing: t_pw – (t_setup + t_skew) (DH)

Page 476, Exercise 7.5: Assume the cycle time is 500 ps. (DH)

Page 477, Exercise 7.19: Assume the hold time is 0. (DH)

Page 477, Exercise 7.21: Delete hyphen after “fast” (DH)

Page 565, Exercise 8.2: refer to Figure 8.8(b), not 8.5(b) (DH)

Page 566, Exercise 8.15: refer to Figure 8.56, not 8.57. (DH)

Page 566, Exercise 8.16: Delete last sentence about electrical efforts. (DH)

Page 641, Figure 10.4(b): Add a ground symbol in the same place as 10.4(c). (S Carriere 10/31/04)

Page 642, Fig 10.5(b): Use the same dotted metal2 stipple on the GND wire as on VDD. (DH 5/12/04)

Page 644, Figure 10.9: Swap the labels S_h and S_l (S Carriere 10/31/04)

Page 645, 4th paragraph, 3rd line: "symmetric function" -> "self-dual function" J. Frenzel 4/7/05.

Page 648, 2nd line of text: (i-1) -> (i+1) J. Frenzel 4/19/05

Page 649, first line: 10.18 -> 10.17 (D. Ha, 4/4/05)

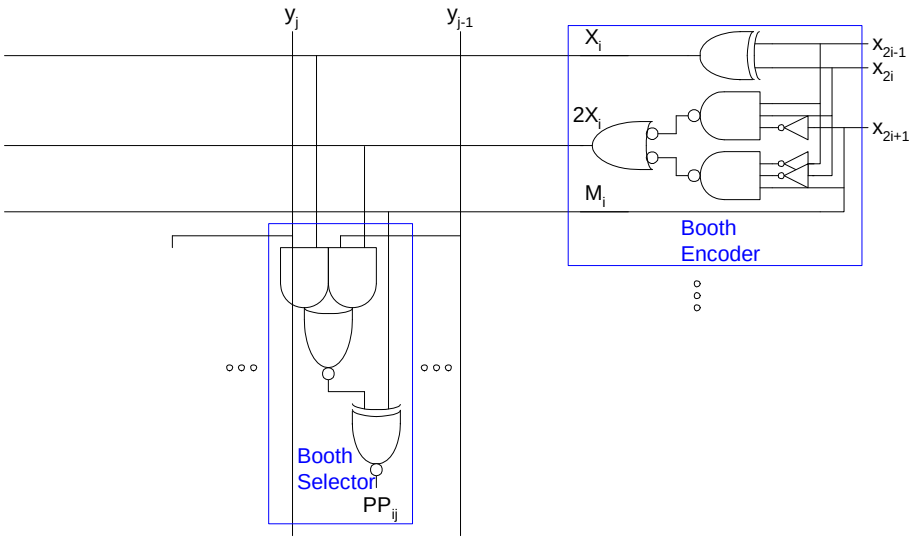
Page 653, EQ 10.14: 2(n-1)+(k-1) -> [2(n-1)+(k-1)] (R. Chaddha, 10/30/04)

Page 662, Figure 10.34(c): the gray cell labeled 8:1 should be a black cell (A. Kesiraju, 10/7/04)

Page 666, Figure 10.36: rightmost carry chains should use gray rather than black cells in first row of (d) and first two rows of (a). (DH)

Page 673-676: numerous errors in subscripts and formulas on Naffziger adder. *Caveat emptor*. (J. Ziser, 12/16/06)

Page 699, Figure 10.75. Booth encoder is incorrect. Replace with:



(E. Brunvand 2/16/05)

Page 710, Exercise 10.2: Change last sentence to "… function of the most significant bits of the two inputs and the output." (DH)

Page 710, Exercise 10.3: Change last sentence to "…function of the sub signal and the most significant bits of the two inputs and the output." (DH)

Page 710, Figure 10.87: Delete (b) (DH)

Page 710, Exercise 10.6: Change to "The carry increment adder in Figure 10.31(b)…" (DH)

Page 723, Fig 11.14: Switch inverted and noninverted inputs A2, A1, A0. (DH)

Page 727, Figure 11.19: swap bars on A1/A1bar and A2/A2bar (R. DiGiacomo, 12/19/04)

Page 732, 3rd to last line: 2^N should be $2N$ (DH)

Page 792, Fig. 12.32: Upper left transistor in charge pump should be tied to bias voltage, not to VDD. T. Saito 1/05

Page 810, EQ 12.16: r_0 should be r_o (DH)

Page 815, EQ (12.23): R_1 should be R DH 10/21/04

Page 865, priority_if figure: the output should be y[3:0] instead of a[3:0]. A. Rainier 1/27/05

Page 866, priority_assign figure: the output should be y[3:0] instead of a[3:0]. A. Rainier 1/27/05

Page 866, ram figure: the input should be addr[5:0] instead of adr[5:0]. A. Rainier 1/27/05

Page 873, first paragraph: "tempted so" -> "tempted to" A. Rainier, 1/27/05

Page 886, mipstest assembly. "Machine Code" and 8-digit opcodes should be aligned in a column. DH 1/18/05

Page 929, [Chern92]: P. Yang," Multimetal -> P. Yang, "Multimetal (D. Suarez, 3/16/05)

Index: entries from page 136-154 are misnumbered (S. Carriere, 11/25/04)
p. 138 (should be 136)
Multiple threshold voltages

Threshold voltage
Subthreshold
Gate oxide
Silicon on Insulator
SOI
P 139 (should be 137)
Sapphire
Buried oxide
Dielectric
Subthreshold
Finfet
p. 140 (should be 138)
mobility
SiGe
p. 141 (should be 139)
strained silicon
plastic transistors
transistor; plastic
p. 142 (should be 140)
copper
damascene process
dual damascene
p. 142 (should be 141)
low-k dielectric
fluorosilicate glass
p. 143 (should be 141)
SiLK
Capacitor
MOS capacitor
p. 144 (should be 142)
poly-insulator-poly capacitor
metal-insulator-metal capacitor
MIM capacitor
Fringe capacitor
Fractal capacitor
Resistor
Silicide block
Nichrome
p. 144 (should be 143)
Dummy resistor
Finger
p. 146 (should be 144)
temperature coefficient
spiral inductor
inductor
Q

p. 147 (should be 145)
permeability
transmission line
microstrip
coplanar waveguide
nonvolatile memory
NVM
One-time programmable memory
Fuse
p. 147 (should be 146)
Electrically erasable programmable ROM
Flash memory
Floating gate
p. 148 (should be 146)
bipolar transistor
transistor; bipolar
npn transistor
pnp transistor
BiCMOS
p. 148 (should be 147)
collector
base
emitter
p. 149 (should be 147)
fuse
antifuse
accelerometer
p. 149 (should be 148)
MEMS
p. 150 (should be 148)
carbon nanotube
nanotubes
p. 150 (should be 149)
run set
p. 151 (should be 149)
Dracula
Nwell
Active
P-select
n-select
poly
contact
metal
p. 153 (should be 151)
breakdown voltage
p. 154 (should be 152)

diode
p. 155 (should be 153)
resolution enhancement