

Digital Electronics & Computer Engineering (E85)

Harris

Fall 2010

Midterm

This is a closed-book take-home exam. You are permitted a calculator and one 8.5x11" sheet of paper with notes. You may not communicate about the exam with anyone except the instructor before you have turned in the exam.

Record the time that you start and end working on the exam. You must complete all of your work no later than 2 hours after you began.

You are bound by the Harvey Mudd College Honor Code while taking this exam.

Along side each question, the number of points is written in brackets. The entire exam is worth 35 points. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Write neatly; illegible answers will be marked wrong. Show your work for partial credit.

Name: _____

Time Started: _____

Time Ended: _____

Do Not Write Below This Point

Page 2: _____ /5

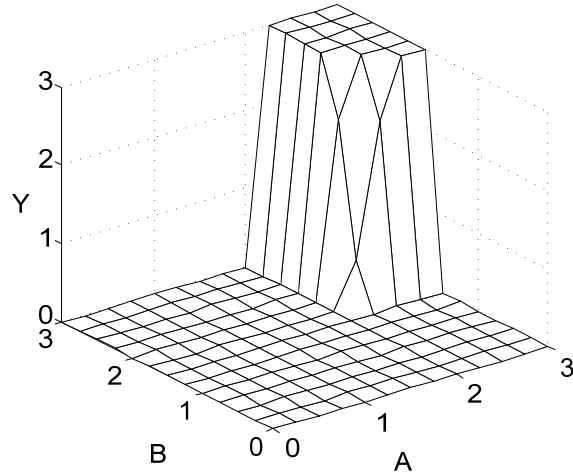
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Total: _____ /35

You have discovered an unlabeled 2-input logic gate in the lab. By meticulously varying the input voltage to terminals A and B and measuring the output voltage at Y, you discover that the gate has the following characteristics.



1. [1] What kind of logic gate did you find?

Gate type _____

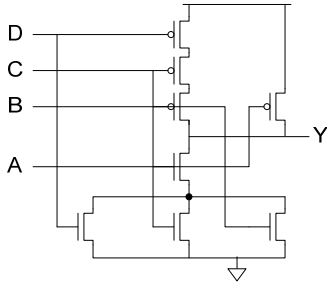
2. [2] What are the input and output logic levels?

V_{IL} _____ V_{IH} _____ V_{OL} _____ V_{OH} _____

3. [2] What is the worst-case noise margin?

Noise Margin _____

4) [3] While walking down a dark alley, you encounter the following shady logic gate. Scare it off by writing its Boolean equation.



Logic Function: Y = _____

5) [2] Write -100 as an 8-bit 2's complement number.

Number: _____

6) [3] Write the simplest Boolean equation equivalent to the following Verilog code:

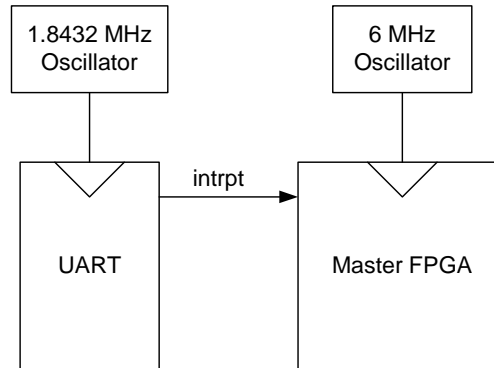
```

module midterm(input logic a, b, c, d, e,
               output logic y);
    assign y = a & b & ~c | a & c & e | a & d & ~b & ~c |
              a & b & c & d | a & c & ~e;
endmodule

```

Simplified Function: Y = _____

7. [5] The 1999-2000 Sun Microsystem Clinic Team built a finite state machine on a Xilinx Spartan S20 Field Programmable Gate Array. It ran a loop in which it read 32 bytes from a Universal Asynchronous Receiver/Transmitter (UART). The UART generated an *intrpt* signal whenever a new byte was available to read. The FPGA ran on a 6 MHz clock and the UART used a 1.8432 MHz clock.



The FSM would run through the loop several times receiving several interrupts and reading the bytes, then crash by transitioning to an invalid state not listed in the state transition table (neither S39 nor S38). The invalid transition took place out of the following loop:

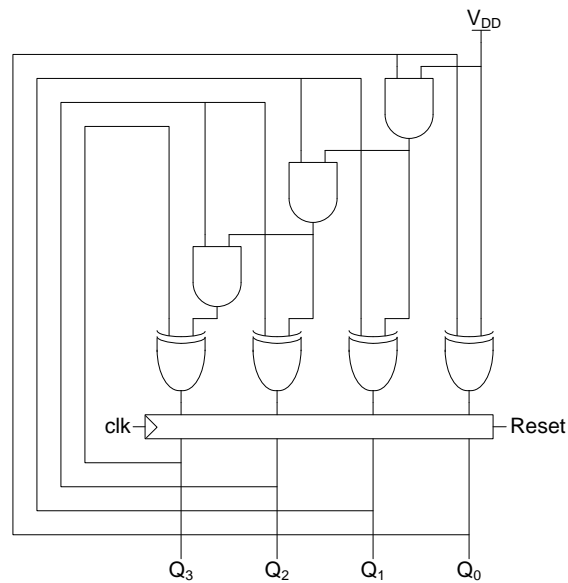
```

always @ (CurrState or Datain or intrpt or count)
begin
  case (CurrState)
  ...
  S38: // waiting for interrupt indicating next byte arrived
  begin
    if (intrpt)
    begin
      NextState <= S39;
    end
    else
    begin
      NextState <= S38;
    end
  end
end
...

```

There were no errors in portions of the code not shown. Explain why the system malfunctioned and how you could fix the problem.

Your firm, Spaced Out Circuits, designs digital systems for NASA interplanetary missions. An engineer from Caltech spent three months designing the following circuit before being fired. Your boss says that it doesn't run fast enough, costs too much to produce, and that the engineer left no documentation of what it is supposed to do.



The space-qualified digital components available to you have the following specs:

Component	Unit cost	Propagation Delay (ps)	Contamination Delay (ps)
Inverter	\$3	20	15
Buffer	\$4	30	25
AND2 / OR2	\$15	35	25
AND3 / OR3 / XOR2	\$20	40	30
Resettable Flip-Flop	\$30	32	15

The flip-flop also has a setup time of 22 ps and a hold time of 28 ps. The current design costs $\$30 \times 4 + \$20 \times 4 + \$15 \times 3 = \245 .

8. [2] Explain to your boss what the circuit does as clearly and concisely as possible.

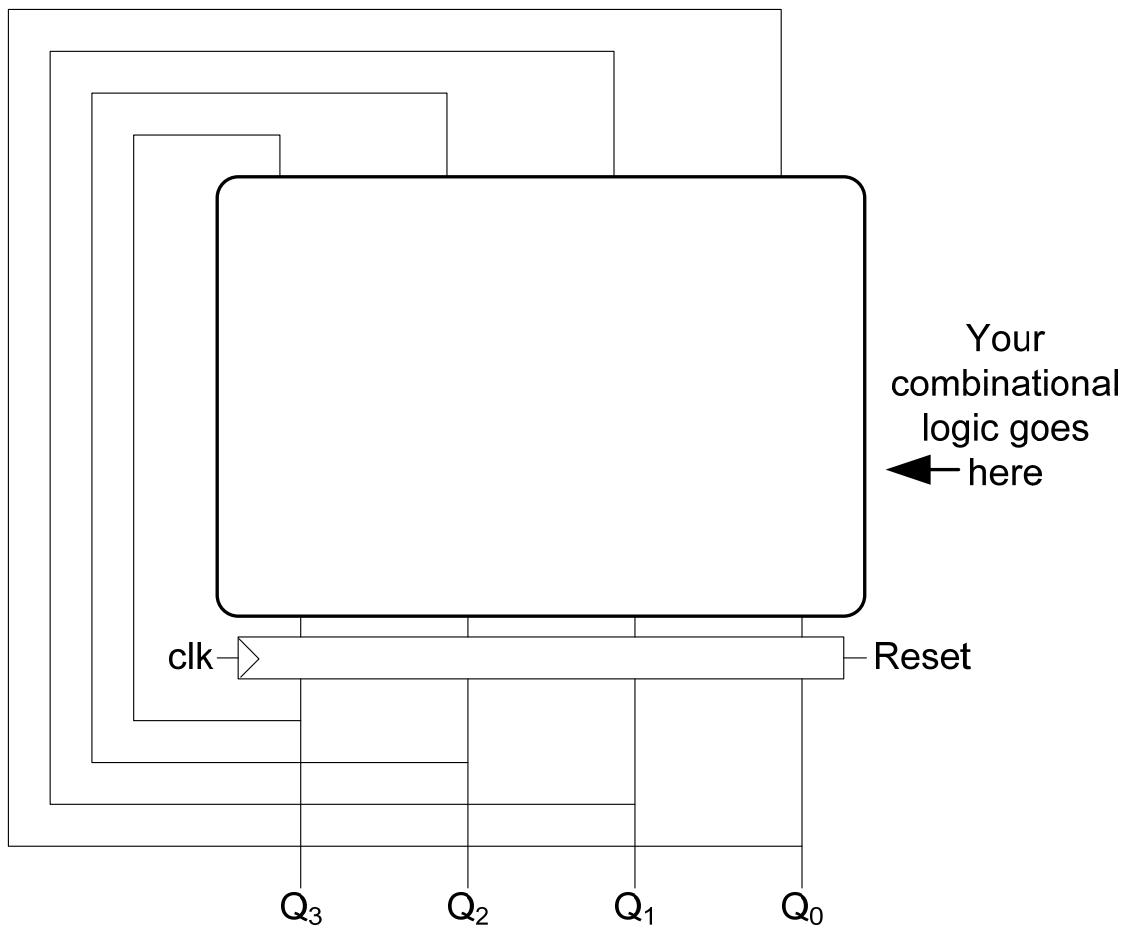
9. [1] What is the minimum clock period at which the circuit will operate correctly if there is no clock skew?

Clock Period _____

10. [2] How much clock skew can the circuit withstand and still operate correctly if the clock period is 500 ps?

Maximum Skew _____

11. [4] Suppose the actual clock skew may be up to 20 ps. Redesign the combinational logic to run as fast as possible. Choose the lowest-cost solution that achieves this speed and works reliably. Sketch your design below.



12. [3] What is the clock period at which your improved circuit will operate correctly if the clock skew may be up to 20 ps?

Clock Period _____

13. [1] What is the cost of your improved circuit?

Cost _____

14. [3] Write the shortest and simplest Verilog code that you can to describe the circuit.

```
module mystery(input logic clk, reset,  
               output logic [3:0] Q);
```

```
endmodule
```